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Short communication

Design optimization guidelines for a class of RF switched-capacitor power amplifiers

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ABSTRACT

An optimization methodology for a popular class of differential RF switched-capacitor power amplifiers exhibiting high efficiency, output power and linearity is presented. Analytical maximization of the output power with respect to component values provides explicit formulas and design guidelines for the amplifier's core and the tuning of the matching network, that can be used as a starting point for the design and trimming of the power amplifier circuit in an IC design environment.

1. Introduction

Power amplifiers (PA) are often considered to be the most challenging block to implement in a RF transmitter; the need for spectrally efficient modulation schemes has led to signals with high peak-to-average power ratio (PAPR). Thus, related research has been focused on the improvement of the trade-off between linearity and efficiency. In this direction, various techniques have been proposed.

Envelope elimination and restoration (EER) [1–7] is one viable candidate for efficiently amplifying RF signals with amplitude modulation (AM). In most polar modulators, the phase-modulated signal is fed to an efficient switched-mode PA. The reconstruction of the AM signal is done by modulating the power supply voltage of the PA. This approach, however, has several drawbacks degrading the performance of the transmitter; the efficiency-bandwidth trade-off of the power supply modulator, and the reduced efficiency of the transmitter at power back-off levels are the most challenging ones to address.

The outphasing architecture [8–10] has been a promising solution, achieving impressive results. Its principle of operation is the decomposition of the RF signal into two constant-amplitude signals, with the amplitude modulation information encoded in their relative phase. This makes possible the use of switched-mode PAs. The reconstruction of the amplified signal can be achieved using a power combiner.

Pulse-width modulation (PWM) [11–13] is another proposed technique. Here, the amplitude information is encoded in the pulse width resulting in the generation of a constant-amplitude signal, but with varying duty cycle driving a switched-mode PA. The main drawback of this technique is the pulse-swallowing effect due to the minimum pulse duration.

Most of the aforementioned problems are addressed effectively by digitally-modulated power amplifiers (DPAs) consisting of multiple unit PA cells [14–17]. A subset of unit cells are selected to be switched at the carrier frequency, based on the digital amplitude codeword that eventually controls the output amplitude. In order to achieve high efficiency, a switched-mode PA can be used for each unit cell.

The class of switched-capacitor PA (SCPA) examined in this work was introduced in [18]; it is a case of a DPA offering numerous advantages [19,20], such as high accuracy due to precise capacitor ratios achieved in CMOS technology [18,21,22], as well as flexibility of scaling for higher resolution applications (e.g. for WLAN to WiMAX), and has been employed in various PA designs [23–27]. The SCPA's core consists of an array of N capacitors; depending on the input code, n of the capacitors switch between V_{dd} and ground at the RF carrier frequency, while the rest $N-n$ of them are grounded. In the simplest case, all capacitors and switches are of the same size as shown in Fig. 1. Modeling of the SCPA family has been presented in [28,29] with emphasis on the state-space and the mathematical details, in [30] focusing on mismatch, in [31] on dealing with losses, and in [32,33] regarding nonlinearity and

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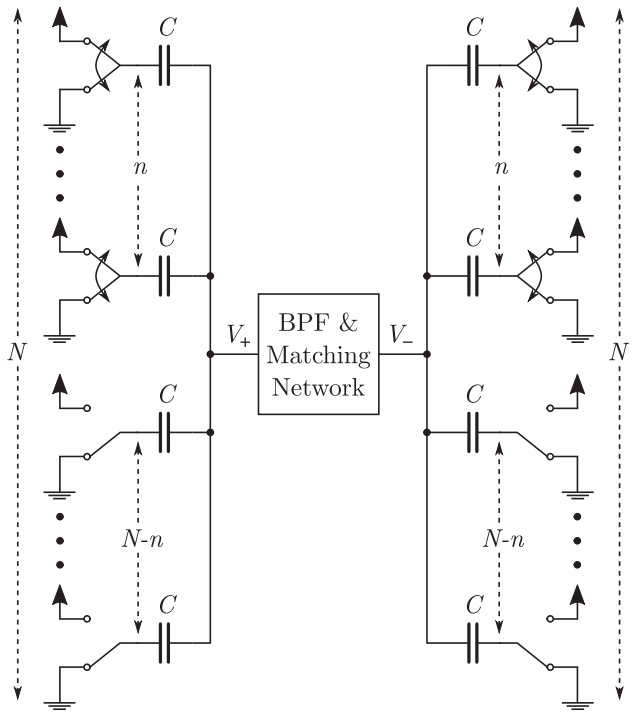

Fig. 1. Architecture of the differential SCPA [28,29].

its reduction.

This work is motivated by the SCPA mathematical modeling in [28,29] and provides design optimization guidelines along with closed-form expressions for the optimal component values. These values can be used as a starting point for the design and trimming of the SCPA circuit in an IC design environment (e.g. Cadence), speeding-up its general optimization, while further help with the initial area estimation of the design. Along with the work presented in [28,29], a complete framework for initial parameterization and optimization of the particular SCPA family design procedure is provided. The detailed steps of the presented framework could allow its adaptation to other classes of switching power amplifiers, based on the same methodology principles and steps.

The remainder of this article is organized as follows: Section 2 briefly discusses the operation of the examined SCPA class, and Section 3 presents the power optimization of the SCPA. Simulation results and additional remarks are given in Section 4, while Section 5 concludes the article.

2. SCPA operation

The SCPA of Fig. 1 is formed of N identical unit cells, like the one seen in Fig. 2. The first n ($n = 0,1,\ldots,N$) of the unit cells are active and operate in parallel, switching their capacitors C simultaneously between V_{dd} and ground at the RF carrier frequency, ω_c, by means of complementary clocks ϕ and $\widetilde{\phi}$. In the remaining $\widetilde{n} = N - n$ grounded unit cells, the capacitors C are kept grounded with the PMOS being continuously off and the NMOS being in triode. The model of the unit PA cells includes the on resistance of the MOSFETs in triode, represented by conductances g_n and g_p, for the NMOS and the PMOS, respectively. It does not include MOSFETs' capacitances C_{db} and C_{gd} nor the fringing parasitics of C, assuming they are significantly smaller[1] than C; conditions desirable for achieving high power efficiency.

[1] And their impedance at ω_c is much larger than that of the corresponding cell's load.

The switches' network of the N unit cells is followed by the tuning and matching network as shown in Fig. 1. The detailed structure of the tuning and matching network we consider is shown in Fig. 3. Here, inductor L_1 is used to tune the total capacitance $NC = (n+\widetilde{n})C$ at the carrier frequency, i.e.

$$L_1 = \frac{1}{NC\omega_c^2}, \tag{1}$$

while L_2 and capacitor C_m comprise the low-pass matching network employed for the impedance transformation and the suppression of harmonics. Resistors R_1 and R_2 model the finite quality factors Q_1 and Q_2 of the inductors L_1 and L_2, respectively. Supply bondwire inductance is assumed to be much smaller than L_1, L_2, and thus to have a negligible effect at the operating frequency; so, it is ignored in the analysis to follow. The load of the antenna is denoted by R_L and it is transformed to the termination resistance r_x by L_2, and C_m; r_x is considered as an optimization parameter to maximize output power.

3. Power optimization

We start the optimization process from the output load R_L and proceed towards the switches. First we establish a value for the intermediate resistance r_x transformed via the $L_2 - C_m$ pair as shown in Fig. 3. Because of the differential structure we can use the half-circuit of Fig. 3, with an equivalent load of $R_L/2$. The values of L_2 and C_m are derived by requiring that the resistance $R_L/2$ transformed by $L_2 - C_m$ equals r_x at ω_c. Starting from

$$\begin{aligned} r_x &= j\omega_c L_2 + \frac{R_L}{2 + j\omega_c R_L C_m} \\ &= \frac{2R_L}{4 + \omega_c^2 R_L^2 C_m^2} + j\left(\omega_c L_2 - \frac{\omega_c R_L^2 C_m}{4 + \omega_c^2 R_L^2 C_m^2}\right) \end{aligned} \tag{2}$$

we solve for C_m and L_2 to get

$$\begin{aligned} C_m &= \frac{1}{\omega_c R_L}\sqrt{\frac{2R_L}{r_x} - 4} \\ L_2 &= \frac{r_x R_L C_m}{2} \end{aligned} \tag{3}$$

where it must be $0 < r_x < R_L/2$. The limit $r_x = R_L/2$ practically means no presence of a transformation network and thus, no harmonic suppression at the output.

Now we derive the optimal value of r_x^{opt}, maximizing output power, P_{out}. We do so by making the simplifying assumptions that $g_n = g_p\ (= g)$, and that the pulses driving the CMOS switches are steep with 50% duty cycle. In this case the single-side linear model of the SCPA is as in Fig. 4; it models the whole set of the N unit cells, combining in parallel, the group of n active cells, and the group of the remaining $\widetilde{n} = N - n$ grounded cells. The source, V_S, provides a 50% duty cycle square-wave from 0 to V_{dd}. The values of the unit cell capacitor C and the load resistance R_L are specified from the beginning of the design and are considered given, while L_1 is given by (1) and $R_i = \omega_c L_i/Q_i, i = 1,2$.

The equivalent circuit of Fig. 5 has been obtained from Fig. 4 through Thévenin transformation implying the following expressions, where (1) has been used,

$$\begin{aligned} Z_{th} &= A + jB \\ A &= \frac{R_1 C + gL_1}{C(1 + NgR_1)} \\ B &= \frac{\omega_c L_1 (1 - NgR_1)}{(1 + NgR_1)} \\ V_{th} &= \gamma_{th} V_{dd} \\ \gamma_{th} &= \frac{ng(R_1 + j\omega_c L_1)}{1 + NgR_1}. \end{aligned} \tag{4}$$

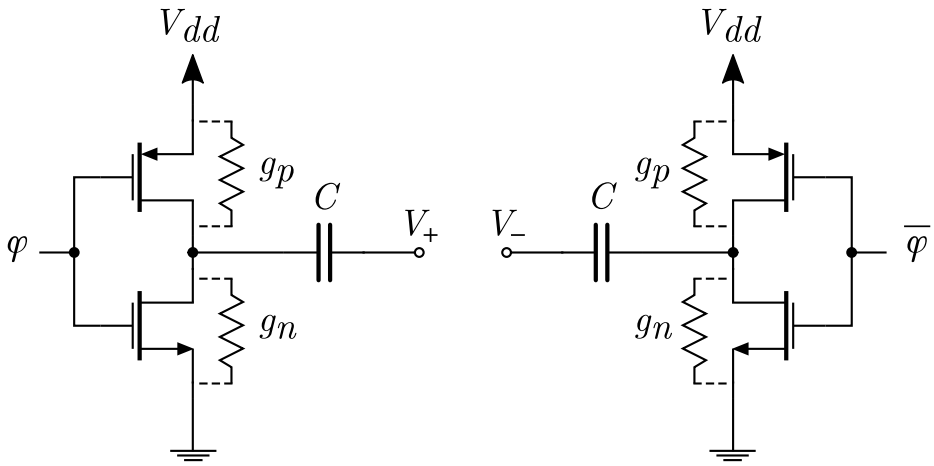

Fig. 2. Unit PA cell of the differential SCPA [28,29].

The 0 to V_{th} square-wave source signal, V_{Sth}, has Fourier decomposition

$$V_{Sth} = \frac{2V_{th}}{\pi}\left(\sin\left(\omega_c t\right) + \frac{1}{3}\sin\left(3\omega_c t\right) + \frac{1}{5}\sin\left(5\omega_c t\right) + \ldots\right),$$

and the fundamental frequency component amplitude of the output u_x is

$$\left|u_x\right| = \frac{r_x}{\left|r_x + R_2 + Z_{th}\right|}\cdot\frac{2}{\pi}\left|V_{th}\right|. \tag{5}$$

The RMS output power of the fundamental frequency component for the differential structure is given by $P_{out} = 2\cdot\left|u_x\right|^2/(2r_x)$; using (4)–(5) we get

$$P_{out} = \frac{r_x}{\left(r_x + R_2 + A\right)^2 + B^2}\cdot\frac{4}{\pi^2}\left|\gamma_{th}\right|^2 V_{dd}^2. \tag{6}$$

Note that P_{out} is an implicit function of g via A, B and γ_{th}. As expected

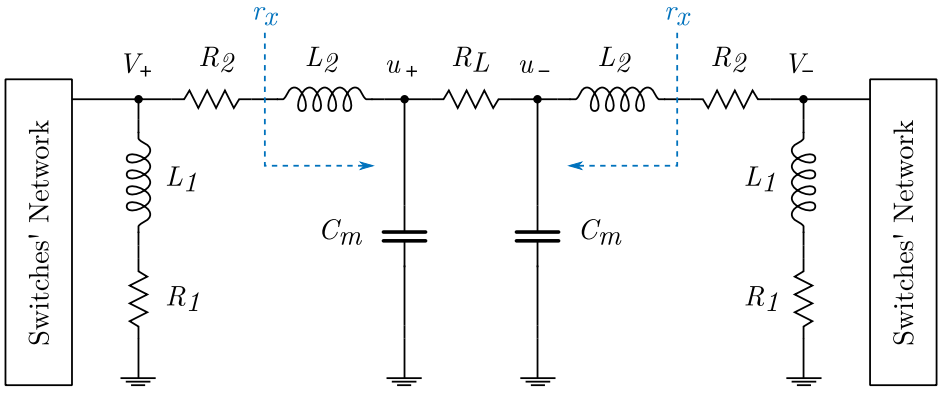

Fig. 3. The differential SCPA with the matching network and differential load [29].

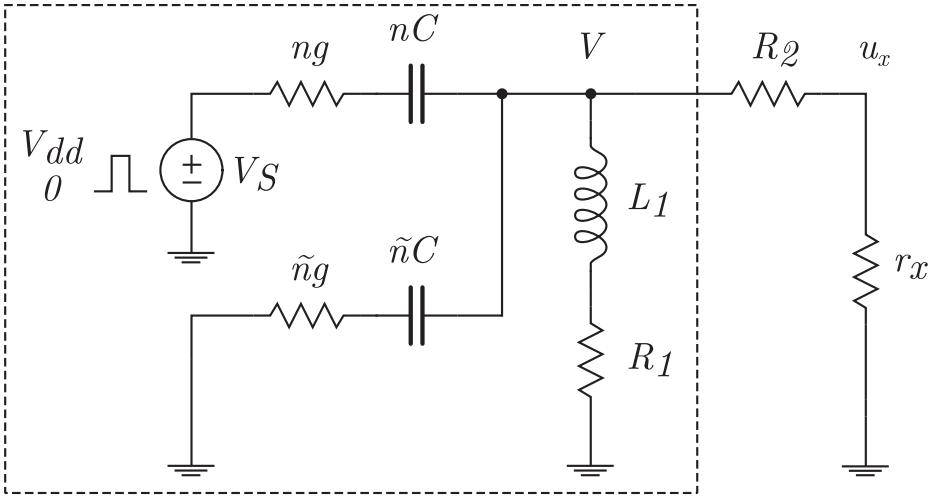

Fig. 4. Equivalent half-circuit at ω_c for the derivation of r_x^{opt}.

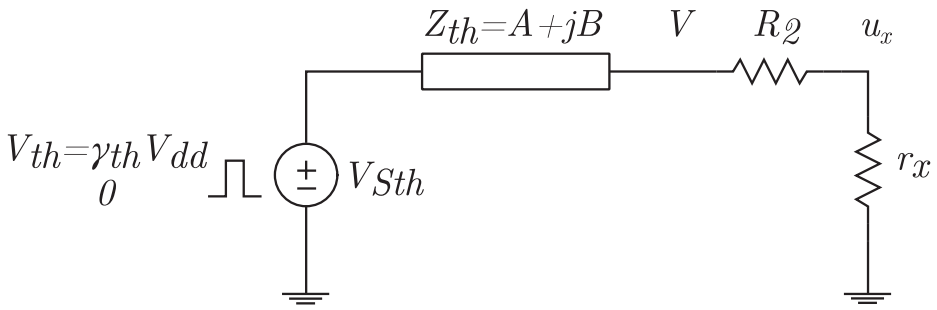

Fig. 5. The equivalent of Fig. 4 at ω_c with the dashed block transformed.

intuitively, it can be verified through lengthy calculations that P_{out} is strictly increasing with g. Since $g = 1/r_{on} = \mu C_{ox}(W/L)V_{eff}$, it is advised to select the W/L ratios of the PMOS and NMOS transistors as large as possible, keeping in mind however, that large areas WL result in undesirable large parasitic capacitances.

To derive the optimal value of r_x, we observe first that in (6), none of A, B or γ_{th} depends on r_x explicitly or implicitly. Moreover, combining (3) with $R_2 = \omega_c L_2/Q_2$ we get

$$R_2 = \frac{1}{Q_2}\sqrt{r_x\left(\frac{R_L}{2} - r_x\right)} \tag{7}$$

and, therefore, R_2 is a function of r_x. Taking $dP_{out}/dr_x = 0$ then gives

$$(r_x + R_2 + A)^2 + B^2 - 2r_x(r_x + R_2 + A)\left(1 + \frac{dR_2}{dr_x}\right) = 0. \tag{8}$$

Replacing (7) into (8) results in a complicated algebraic equation of r_x. To simplify things and yet achieve good accuracy in our analytical approach, we note that dR_2/dr_x is not very sensitive to r_x, when r_x is away of the limits 0 and $R_L/2$ (this can be verified easily by the second derivative of R_2). So, we approximate dR_2/dr_x with its numerical value for $r_x = R_L/4$ (the center value of the allowed range for r_x). This results in $dR_2/dr_x = 0$, simplifying (8) to

$$r_x^2 = (R_2 + A)^2 + B^2. \tag{9}$$

Replacing (7) into (9) gives a fourth-order algebraic equation with a complicated solution. Instead, we use the same approximation as before, i.e. in (9) we replace R_2 with $R_L/(4Q_2)$ which is the value of R_2 corresponding to $r_x = R_L/4$. Thus

$$r_x^{opt} = \sqrt{\left(\frac{R_L}{4Q_2} + A\right)^2 + B^2}. \tag{10}$$

Eq. (10) gives us an analytical and handy way for the initial selection of r_x and so the transformation impedance ratio that leads to maximum output power. As shown from (10), r_x^{opt} is independent of the input code, n.

4. Simulation results

The findings of the previous section are evaluated in a differential SCPA implemented in TSMC 40 nm technology and simulated in Cadence Spectre, where all results are derived by parametric periodic steady-state (PSS) analysis in shooting mode.

The SCPA operates under a supply voltage of V_{dd}=1 V, with N=64, C = 300fF, and drives a load of $R_L = 100\Omega$. The carrier frequency, f_c, is set at 5.9 GHz, resulting in $L_1 = 0.038$ nH. Parameter D (the ratio of the time-length during which the NMOS or PMOS switch is on, to the length of half a period [29]) is chosen to be 80%. The transistors of each unit PA cell are sized with $L_n = L_p = 40$ nm, $W_n = 40$ μm, and $W_p = 54$ μm, giving $r_{on,n} = 7.75\Omega$, and $r_{on,p} = 7.80\Omega$. The clock signals reach the unit PA cells via appropriate drivers (inverters), while power supply and ground bondwire parasitic inductances, as well as internal decoupling capacitances are taken into account in the simulation setup.

Assuming $r_{on} = (r_{on,n} + r_{on,p})/2$, and $Q_1 = Q_2 = 10$, Eq. (10) gives

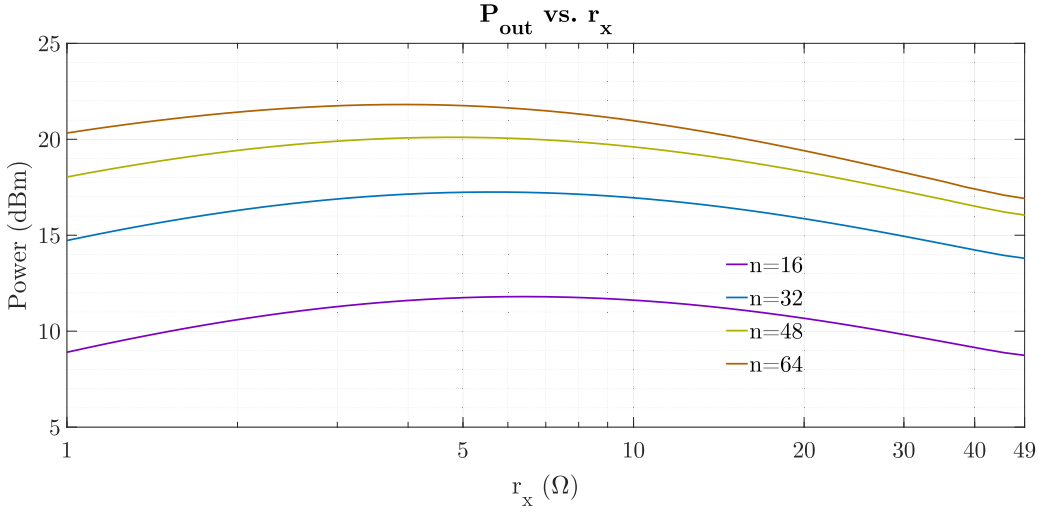

Fig. 6. P_{out} as a function of r_x.

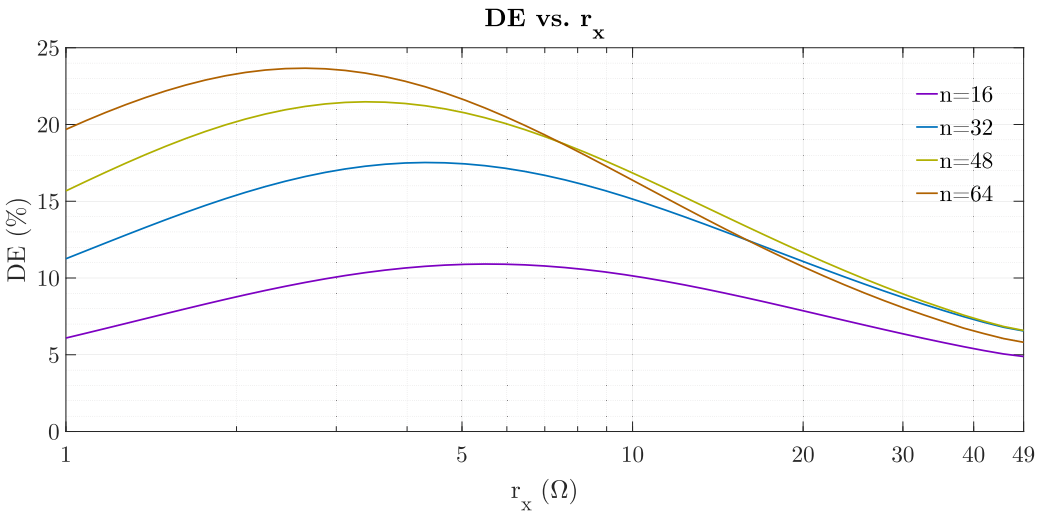

Fig. 7. DE as a function of r_x.

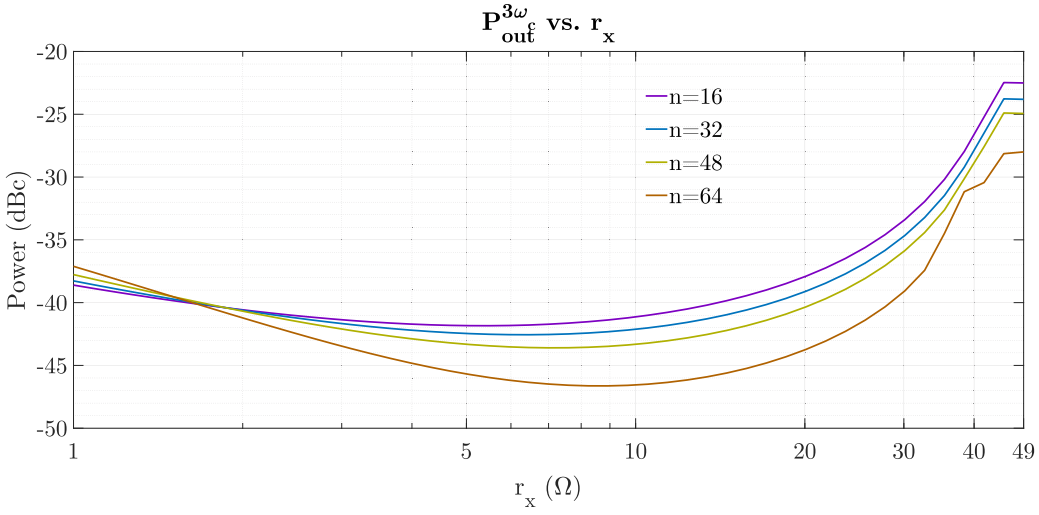

Fig. 8. Third harmonic suppression as a function of r_x.

$r_x^{opt} = 10.1\Omega$. Fig. 6 depicts the SCPA's output power with respect to r_x (in logarithmic scale) for various input code values. It is seen that the value of r_x for which P_{out} is maximized is very close to the value derived by (10). A slow variation in the maximization of P_{out} for decaying values of r_x as n increases can be observed, as a result of the bondwire parasitics.

The proposed optimization of the output power can be further evaluated with respect to an efficiency metric. Fig. 7 presents the drain efficiency (DE) of the complete SCPA[2]. Contrary to the output power, maximization of the DE depends on the input code, n. As such, a DE-oriented optimization of the SCPA would rely on the statistical properties of n, and thus, on the modulation scheme used [28].

The impact of r_x (and thus, r_x^{opt}) in the suppression of the harmonics at the output of the SCPA can be seen in Figs. 8 and 9, where the power of the third and the fifth harmonic is presented (in dBc), respectively. It can be seen that the derived value of r_x^{opt} results in very good harmonic rejection levels. The harmonic suppression deteriorates as r_x increases and approaches the value of $R_L/2$ (which makes the low-pass filter $L_2 - C_m$ disappear).

As a final remark, the dependence of r_x^{opt} with respect to different sets of carrier frequency and C values (where L_1 is always calculated by (1)) can be seen in Figs. 10 and 11; f_c ranges in GHz, while C ranges in fF. The two graphs depict similar behavior and indicate that there may be combinations of f_c and C that result in r_x^{opt} values out of its allowed range of $(0, R_L/2)$. In such cases, either the C value should be reconsidered, or a different topology for the transformation network can be selected.

5. Conclusion

This paper presented an optimization methodology for a popular class of RF switched-capacitor power amplifiers. Handy formulas were provided for the selection of the elements' values in the load-transformation network in order to achieve maximum output power; these values are to be used as a starting point in the initial design phase of the PA to help with the speed-up of its optimization.

[2] Please note that the supply power calculation in [29] takes into account the unit PA cells without their drives; as such, an estimation of the DE with the analysis presented in [29] would differ from the results in Fig. 7.

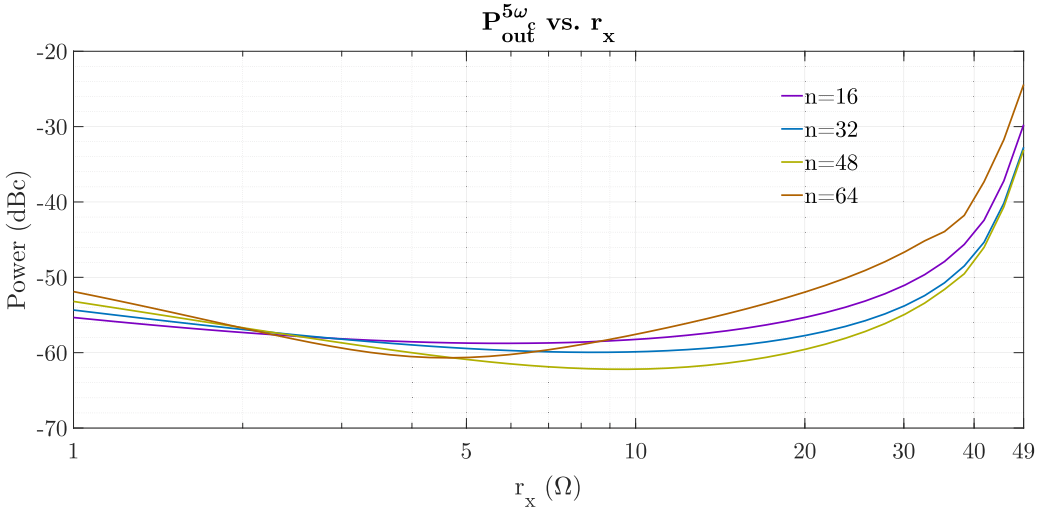

Fig. 9. Fifth harmonic suppression as a function of r_x.

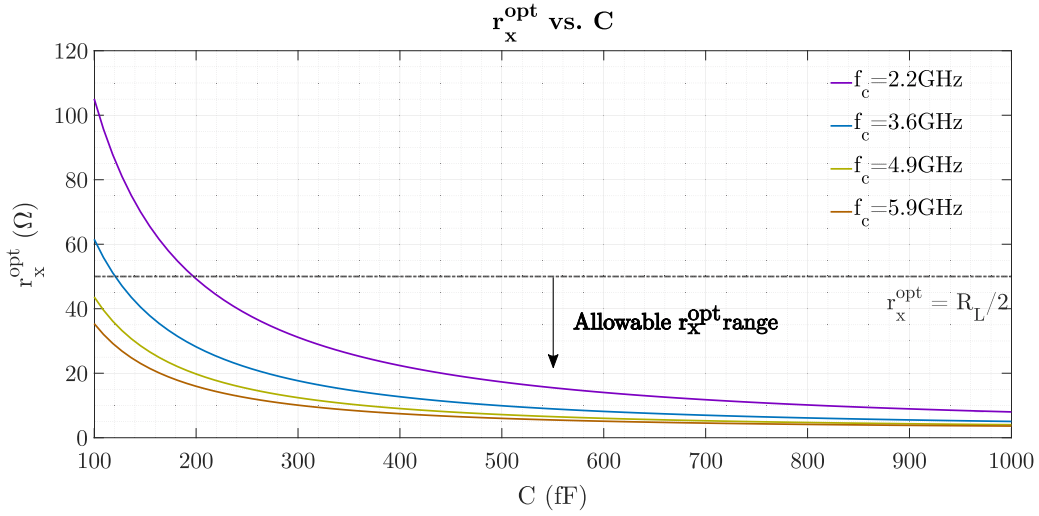

Fig. 10. r_x^{opt} as a function of C.

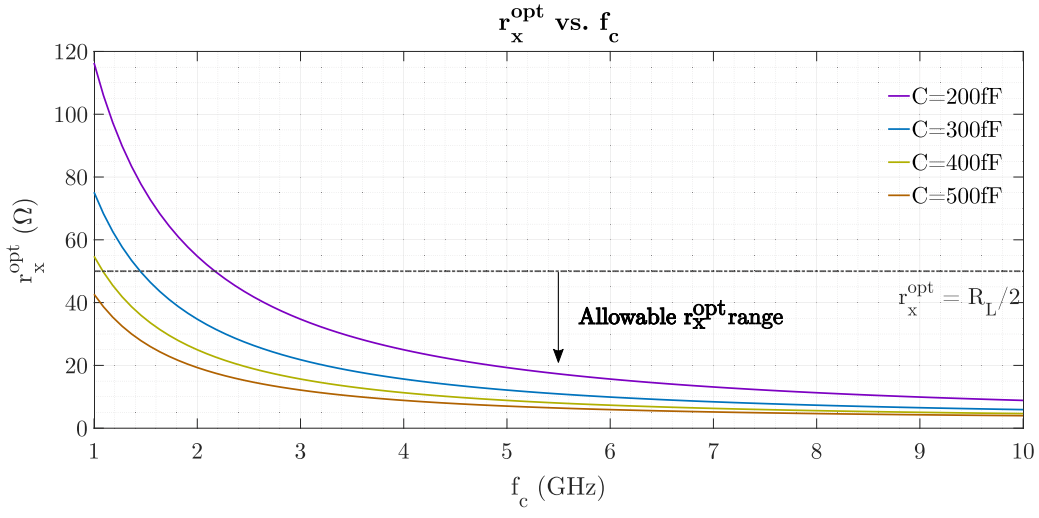

Fig. 11. r_x^{opt} as a function of f_c.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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