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Design of a sub-1V CMOS reference voltage generator

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ABSTRACT

In this paper a low complexity, sub-1V, reference voltage generator with low voltage sensitivity over PVT variation and high power supply rejection ratio (PSRR) is proposed. It consists of a traditional bandgap reference core where resistors are used for generating both the PTAT and CTAT currents, which are then added forming a temperature-independent current. A new 1 V modified folded cascode operational amplifier is proposed and used in the main bandgap's loop resulting in low offset, high loop gain and adequate loop phase margin of 58.9°. The loop consists of only two inverting stages and the circuit can be integrated entirely without the need of external large capacitors for frequency compensation. A regulated cascode current source is employed for accurately mirroring of the core temperature-independent current to a resistive load, where the reference voltage is generated. The proposed circuit was simulated in SPECTRE achieving an output reference voltage variation of 3.62%, without trimming, over process variation corners with ±10% variation of the 1 V power supply voltage and within the industrial temperature range, from −40 °C to 125 °C. The temperature coefficient from −40 °C to 125 °C is 6.81 ppm/°C at 1 V at the typical process corner. The PSRR at 1 Hz and the output RMS noise within a bandwidth of 100 MHz are −69.85 dB and 279 μV RMS, respectively, at the typical process corner, at a supply voltage of 1 V and temperature of 27 °C. Typical power consumption is 452 μA at 1 V.

1. Introduction

Reference voltage generators are fundamental analog circuits included in most analog, digital and mixed signal systems on chip (SoCs) in applications such as mobile, radar, biomedical, automotive, consumer and others. They are employed to provide a stable bias operation point to other blocks such as operational amplifiers, analog to digital converters, digital to analog converters, flash memories, regulators, clock and data recovery circuits, phase-locked loops, etc.. Thus, the reference voltage generators directly impact the performance of all of them in terms of accuracy and noise [1,31].

The main requirements for a voltage reference generator are: low sensitivity of the output voltage on temperature, supply and process variations; low noise, wide temperature range of operation, high accuracy, stability, high PSRR, small die area and low power consumption. In addition, over the past decade technology downscaling has been pushing for low supply-voltage circuit architectures operating at 1 V or below.

In conventional CMOS 1 V voltage reference architectures, parasitic bipolar PNP transistors' base-emitter voltage and thermal voltage are transformed to currents, which are added to generate a stable-over-temperature current, which is converted to a reference voltage on a resistor [2]. Banba's sub-1V design approach [2] paved the way for current-mode voltage-reference designs, using either bipolar devices [3–14] or CMOS devices in the subthreshold regime [15–23], for reference voltage generation. This approach suffers from the bipolar transistor's base-emitter voltage non-linear temperature dependence, the offset error of the core operational transconductance amplifier (OTA), the error of the mirroring of the temperature-constant current generated and the higher order non-linearity over temperature of the resistor converting the temperature-constant current to voltage.

The bipolar transistor's base-emitter voltage non-linear temperature dependence can be reduced by applying curvature compensation techniques [3], which requires additional resistors and thus higher power consumption and larger area. There is also room for improvement and discussion concerning the mirroring of the temperature-constant current to the output resistor since a current mirror contributes to the voltage reference inaccuracy [4,5]. In Refs. [6,7], 1 V supply bandgap reference (BGR) circuits designed in BiCMOS processes are reported demonstrating low temperature coefficients of 20 ppm/°C and 11 ppm/°C, respectively, in the temperature range of −40 °C to 125 °C. In Ref. [14], the proportional-to-absolute-temperature (PTAT) and the complementary-to-absolute-temperature (CTAT) currents are produced

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using vertical PNP bipolar transistors and the PMOS current mirrors are biased in the subthreshold regime to allow operation with 1 V supply.

In Ref. [24], the threshold voltages of NMOS and PMOS operating in saturation are used to form a temperature-insensitive reference voltage which makes this design approach sensitive to process variations [25]. In Refs. [26–28] CMOS devices operating in weak inversion are employed for the generation of PTAT and CTAT voltages by appropriately adding linear functions of the gate-source voltages. In Refs. [29,30], a pico-watt voltage reference circuit is proposed for low power applications, such as biomedical implantable sensing systems, with a temperature coefficient of 16.9 ppm/°C. In Ref. [30], circuit techniques for the design of BiCMOS voltage references are discussed in detail.

In Refs. [15–23], PTAT current is generated by subtracting the gate-source voltages of two differently sized CMOS devices, biased in the subthreshold region, and applying the difference on a resistor. CTAT current is formed via a CMOS device gate-source voltage which is also applied on a resistor. The addition of the PTAT and the CTAT currents forms a relatively temperature-independent reference current or voltage via a resistor. This approach however results in limited accuracy over a wide temperature range due to the fact that CMOS devices have higher non-linearity (with respect to temperature) compared to bipolar ones. In Refs. [15–17], the threshold-voltage temperature dependence is used for gate-source CTAT voltage generation, resulting in relatively low linearity with respect to temperature.

In Refs. [22,23], fully CMOS, low-voltage, low-power voltage references are reported operating in the weak inversion regime, without bipolar devices or diodes, covering a wide temperature range of 180 °C and 190 °C, respectively. Furthermore, a series combination of high Ohmic and medium Ohmic resistors are used in the PTAT and CTAT current generation loops so that high-order curvature compensation is applied. Despite its advantages, this approach results in high line-sensitivity (6.19%) while resistors' trimming is required for a good performance at the typical corner.

In Refs. [12,13], low-voltage, ultra-low-power voltage references are presented exhibiting a temperature coefficient of 58 ppm/°C, after trimming, in a temperature range of 110 °C; and, 28 ppm/°C with curvature compensation in a range of 165 °C, respectively. In Refs. [19–21, 28], subthreshold low-power voltage references are shown with sub-1V operation and temperature coefficients higher than 12.8 ppm/°C, in a temperature range of less than 125 °C. In Refs. [15,18,26,27], low-power, subthreshold voltage references at sub-1V and 1 V supply voltages are reported. They achieve temperature coefficients of 135 ppm/°C, 19 ppm/°C, 105.4 ppm/°C and 18.5 ppm/°C, respectively, in a temperature range of less than 165 °C.

In Refs. [4,8], an effort was made to decrease the required number of high Ohmic voltage reference resistors using OTA while achieving acceptable accuracy at a supply voltage of 0.9 V. In Ref. [8], the voltage reference performance is measured only from 0 °C to 125 °C. In Ref. [4], the temperature range of acceptable performance, with process and supply voltage variation, is 161 °C; however, two external RC networks are needed to ensure the stability of the circuit's two loops with two 25 pF capacitors. In Ref. [9], the voltage reference proposed in Ref. [4] was adopted and was redesigned in a different CMOS process at 1.2 V with a useful temperature range of 165 °C. It achieved a simulated overall output reference voltage variation of 2.4% over PVT, thus a 4.2% improvement in accuracy compared to the original design.

In Ref. [10], a low-power curvature-corrected CMOS bandgap voltage reference is presented demonstrating a low temperature coefficient of 5.5 ppm/°C from −40 °C to 125 °C with a PSRR of −38.9 dB at 1 KHz and with supply voltage of 1.8 V, using bipolar devices. In Ref. [11], a sub-1V voltage reference is proposed where the PTAT voltage is generated in a traditional BGR core with bipolar devices and its multiplication is done by a self-clocked switched capacitor network. It can operate from −50 °C to 150 °C with a temperature coefficient of 41 ppm/^{0}C. Finally, in Ref. [5], a sub-1V voltage reference is presented based on the sampled reverse bandgap principle and the achieved temperature coefficient is 40 ppm/^{0}C from −20 °C to 85 °C.

This paper presents the design of a low-complexity sub-1V CMOS reference voltage generator, with low output reference voltage sensitivity over PVT across a temperature range of 165 °C, high PSRR and moderate power consumption. The use of external capacitors for filtering or stability, large resistors and trimming requirement is avoided. So, it can be fully co-integrated with high frequency PLLs, in sub-1V processes, for transceiver applications where the BGR current consumption is not the system's bottleneck. A new sub-1V modified folded cascode operational amplifier is imbedded in the conventional bandgap loop which ensures low offset, high loop gain and sufficient loop phase margin. Finally, a regulated cascode current source is also used for the precise mirroring of the bandgap's reference core temperature-independent current to a resistive load.

2. Design

The proposed sub-1V voltage reference generator is shown in Fig. 1. It consists of a variation of Banda's [1,2] bandgap core where a PTAT current is generated via Q1, Q2 and R1. V_{EB} of Q2 is applied on R2 and R3 (R2 = R3) by the operational amplifier OA1 along with MP4 and MP5 completing the loop. This generates the CTAT current. The PTAT and CTAT currents are added forming a temperature-constant current which flows through MP4 and MP5, and, it is replicated via MP3 on R4 to generate Vref.

A simple current mirror would probably fail to replicate accurately the temperature-constant current when the supply voltage is 0.9 V and the temperature is low, e.g. −40 °C, because at low temperatures V_{EB} of Q2 rises even to 800 mV, leaving no more than 100 mV headroom for the current mirror. E.g., if the current mirror was realized using a single MOSFET with 60 mV saturation voltage, the V_{DS} margin left before entering the triode region would be limited to 40 mV; this would reduce the mirror's output resistance which would limit the current mirroring quality and worsen the PSRR.

Furthermore, 1 V MOSFET devices exhibit wider spread of their parameters (g_m, V_{TH}, etc.), over process variation and mismatch, compared to 1.2 V ones, due to their thinner structure. Under these conditions, the error of the reference voltage due to the well-known non-linearity of the V_{EB} of Q2 is less important than that of the current mirror. For these reasons, the design of a sub-1V reference voltage generator using 1 V MOSFET devices can be tedious and demanding. To improve the sub-1V performance of the bandgap and reduce the current mirror's error, a regulated cascode current source is used, as shown in Fig. 1, composed of the operational amplifier OA2, and MP6, MP3 and MP4.

The loops with the two operational amplifiers enforce the same drain-source voltage to MP3, MP4 and MP5, under all conditions, significantly improving the current mirroring accuracy, especially at low supply voltages and low temperatures. Furthermore, OA2 regulates the gate voltage of MP6, providing a very high output impedance, thus high PSRR. Capacitors C4 and C5 provide adequate PSRR at higher frequencies. Capacitor C5 also helps during start-up to obtain smooth transition of the bandgap's core bias currents without ringing. Resistor R6 in series with capacitor C3 provides the frequency compensation of the feedback loop.

In our implementation, all PMOS devices are identical and R2 = R3. Therefore the output reference voltage Vref can be expressed as $V_{ref} = V_T \cdot \frac{R_4}{R_1} \cdot \ln\left(\frac{A_{Q1}}{A_{Q2}}\right) + \frac{R_4}{R_3} \cdot V_{EB(Q2)}$ where A_{Q1} and A_{Q2} are the Emitter sizes of Q1 and Q2, respectively [1]. It was selected that $A_{Q1} / A_{Q2} = 24$ and by appropriately choosing the ratios R_4/R_1 and R_4/R_3 the output reference voltage is set to 290 mV so that MP3 can be properly stacked up with MP6 and resistor R4.

The start-up circuit is formed of NM1 and CMOS inverter INV1. The constant current is mirrored via MP1 to R5 to generate a 500 mV voltage and to drive INV1 since the typical NMOS threshold voltage is about 280 mV. Finally, MP2 is used for the biasing of the operational amplifier

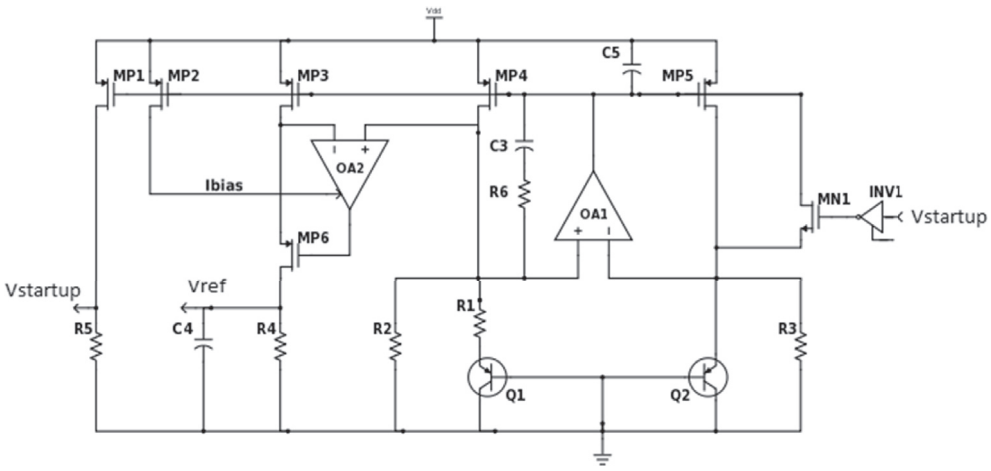

Fig. 1. The proposed sub-1V CMOS reference voltage generator.

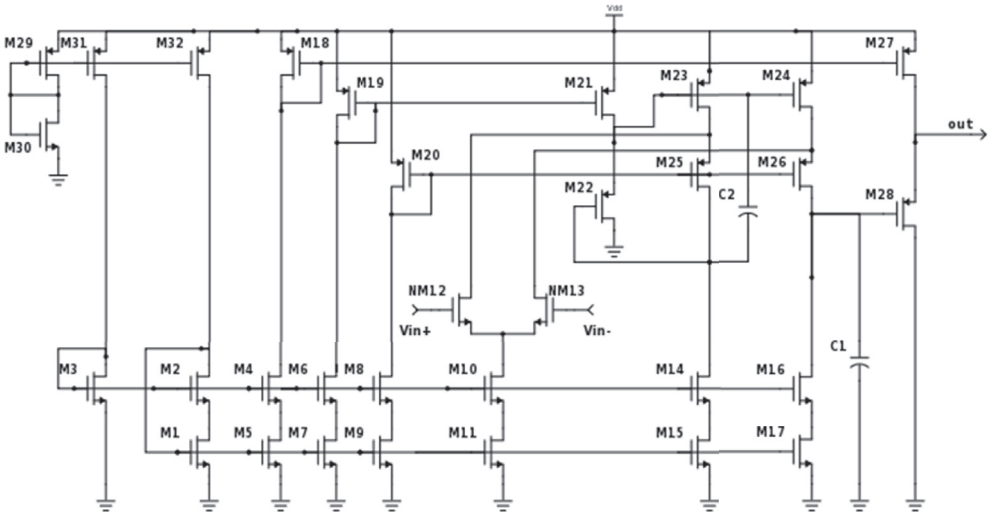

Fig. 2. The proposed 1 V, modified folded cascode operational amplifier with an output buffer stage (OA1).

OA2.

The proposed 1 V, modified folded cascode operational amplifier with output buffer stage (OA1) is shown in Fig. 2. It has a single gain stage, the folded cascode one, and along with the common source amplifier MP4 in Fig. 1, it forms a two-stage loop which can be frequency compensated using a relatively small capacitor achieving adequate gain and phase margin over PVT variation. If a two stage topology had been selected for OA1 instead, frequency compensation would have been more challenging and it would probably require significantly larger compensation capacitors for similar stability performance. OA1 is biased through the current mirror formed by M29-M32, and not via the PMOS devices of the bandgap's core, so that it has available its full gain during the start-up period.

The proposed architecture extends the traditional folded cascode structure, consisting of NM12, NM13, M23-M26 and M14-M17, by adding the extra pair of M21-M22 which forms a DC level shifter. This enables setting the voltage at the drain of M25 so that M23 and M25 remain in saturation over PVT variation. This would have not been possible without the level shifter, i.e. for the traditional low voltage cascode where the gate of M23 is connected directly to the drain of M25, especially for supply voltage of 0.9 V and low temperature e.g. −40 °C. Consequently, if M22 was not included in the design then the gate-source voltage of M23 would have set the drain voltage of M25 to a higher level, putting at risk the operation of M25 in the saturation regime, especially in process corners at

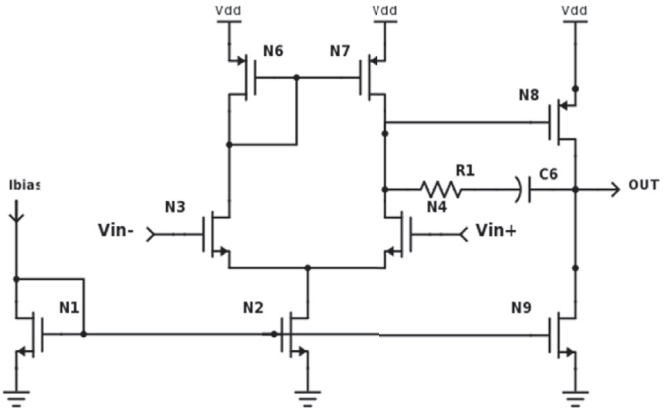

Fig. 3. The two-stages operational amplifier (OA2) used in the regulated cascode current source.

supply voltage of 0.9 V and at low temperatures, e.g. −40 °C.

When the gate bias voltage of the cascode devices M25-M26 is increased by increasing the W/L ratio of M20, the drain-source voltage of M23-M24 is decreased, reducing the folded cascode stage's output impedance and its gain; yet adequate headroom is left for M25 to avoid

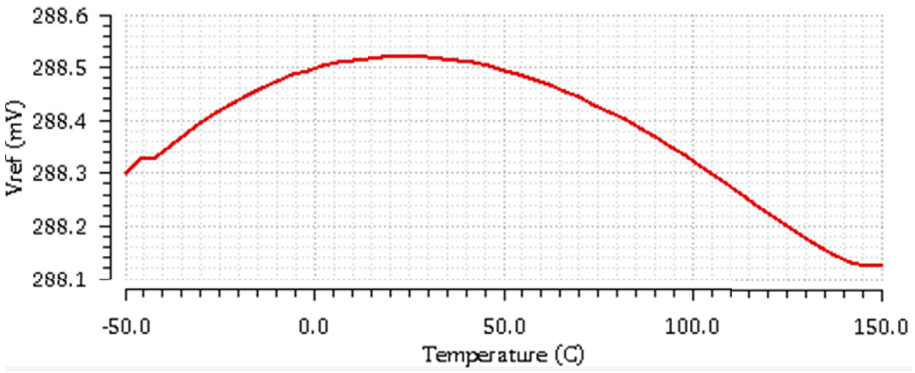

Fig. 4. Output voltage of the proposed Sub-1V CMOS reference voltage generator over the extended temperature range from −50 °C to 150 °C, at the typical corner and with supply voltage of 1 V.

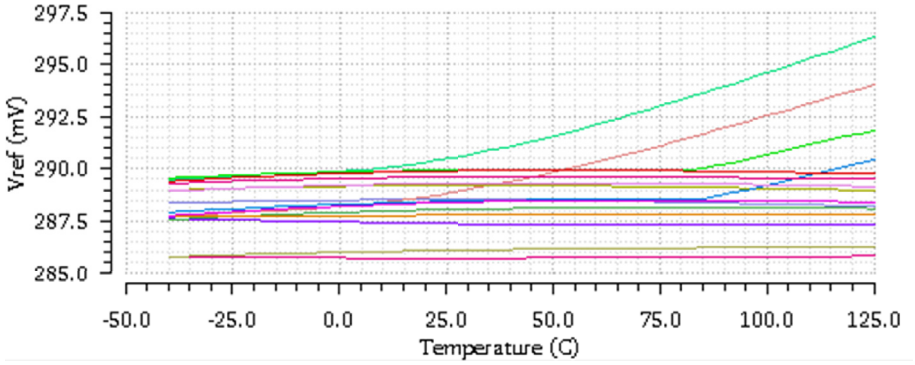

Fig. 5. Output voltage over 32 process corners with 1 V supply voltage varying by ±10% and temperature ranging within the entire industrial range from −40 °C to 125 °C.

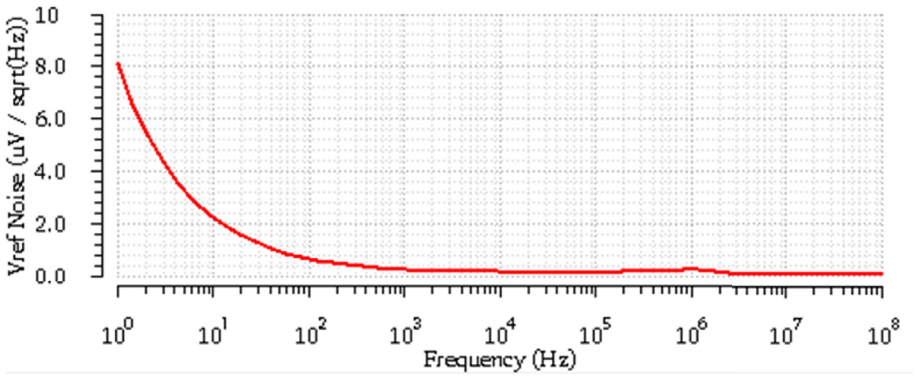

Fig. 6. Noise of the output reference voltage in μV $(RMS)/\sqrt{Hz}$, for 1 V supply voltage and at room temperature.

entering the triode regime. In the opposite case, where the gate bias voltage of the cascode devices M25-M26 is decreased, the folded cascode stage's output impedance and gain are increased; however, less headroom is available for M25, which may enter the triode regime at certain corners and worsen the offset of the folded cascode stage. As it is typical in sub-1V power supply design, the MOSFET devices are sized for minimum drain-source saturation voltage and gate-source voltage close to the threshold. This is also the case for NM12, NM13, M23-M26 and M14-M17.

Capacitor C2 provides frequency compensation of the local loop formed by M22, M23 and M25. The local loop unity gain frequency should be higher than the unity gain frequency of the operational amplifier. Capacitor C1 is used for the frequency compensation of the modified folded cascode structure in Fig. 1.

Finally, M28 is biased via M27 and provides a DC level shift-up of the OA1 output close to the half of the rail. This ensures the operation of M24-M26 in saturation, resulting in high output impedance of the cascode stage and high gain for OA1. High gain is important under all PVT conditions to achieve acceptable bandgap performance especially at low supply voltage of 0.9 V.

The two-stage operational amplifier (OA2) used in the regulated cascode current source is shown in Fig. 3. C6 and R1 are used for the frequency compensation of the entire loop, formed by OA2, MP6 and the load R4. This loop consists of only two inverting stages and a common drain stage thus the Miller frequency compensation technique can be easily applied.

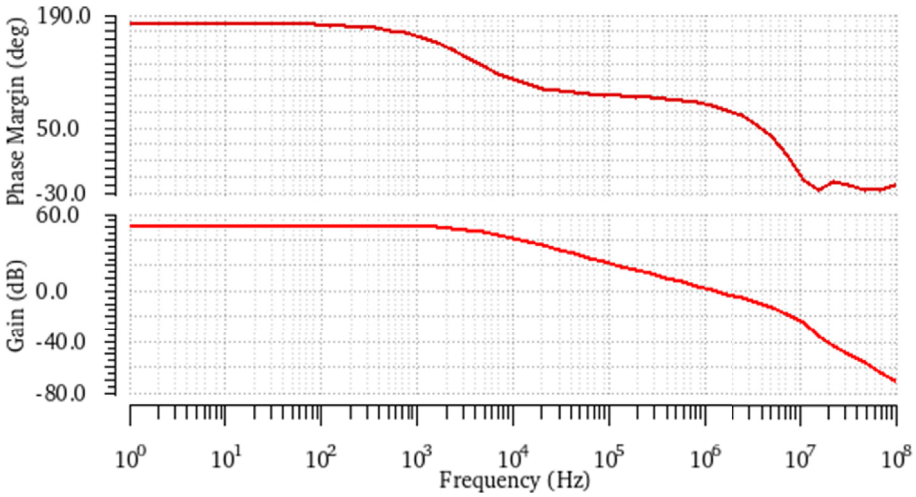

Fig. 7. Phase and gain of the proposed operational amplifier OA1.

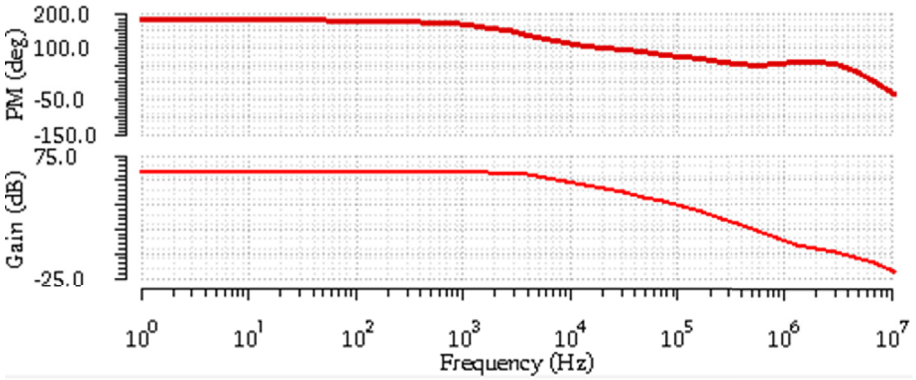

Fig. 8. Phase and gain of the bandgap's main loop formed by OA1 and MP4 loaded with $(\boldsymbol{R}_1 + \boldsymbol{r}_e)//\boldsymbol{R}_2$.

3. Simulations results

Fig. 4 shows the output voltage, V_{ref}, over the extended industrial temperature range, from −50 °C to 150 °C, at the typical corner and with supply voltage of 1 V. The temperature coefficient within the standard industrial temperature range, from −40 °C to 125 °C, is 6.81 ppm/°C.

Fig. 5 shows V_{ref} simulated over 32 process corners, with 1 V supply voltage varying by ±10% and temperature varying within the industrial range from −40 °C to 125 °C. It can be seen that the total variation of V_{ref} is 3.62% without any trimming. Monte Carlo simulation results are shown in Figs. 12 and 13 for room temperature of 27 °C and for supply voltages of 1 V and 0.9 V, respectively.

Fig. 6 shows the noise of the output reference voltage in μV $(RMS)/\sqrt{Hz}$, for 1 V supply voltage and at room temperature. The RMS noise power at the bandwidth of 1 Hz to 100 MHz is 279 μV RMS.

Fig. 7 shows the phase and the gain of the proposed operational amplifier OA1. The DC gain is about 51 dB, the phase margin is 77° (at 1.39 MHz) and the gain margin equals 18.72 dB (at 8.36 MHz) when OA1 is loaded with a capacitive load of C3//C5, all at the typical process corner.

The phase and the gain of the bandgap's core main loop, formed by OA1 and MP4 which is loaded with $(R_1 + r_e)//R_2$, are shown in Fig. 8. The phase margin is 58.94° and the gain margin is 13.74 dB. Fig. 9 shows the phase and gain of the bandgap's second loop, formed by OA2 and

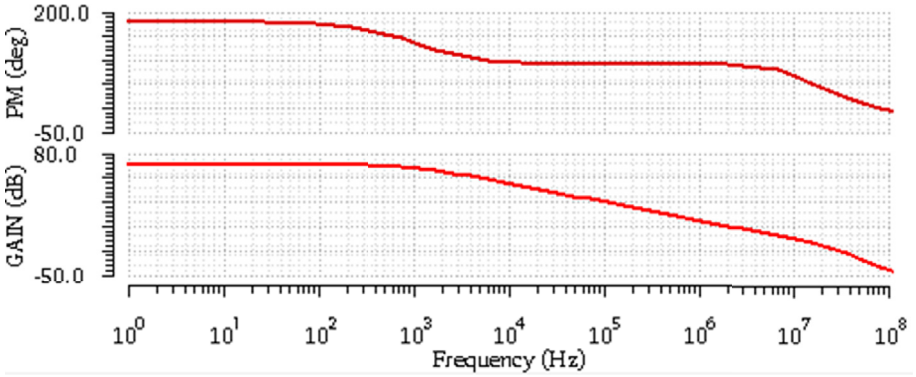

Fig. 9. Phase and gain of the bandgap's second loop, formed by OA2 and MP6 loaded with $\boldsymbol{R}_4//\boldsymbol{C}_4$.

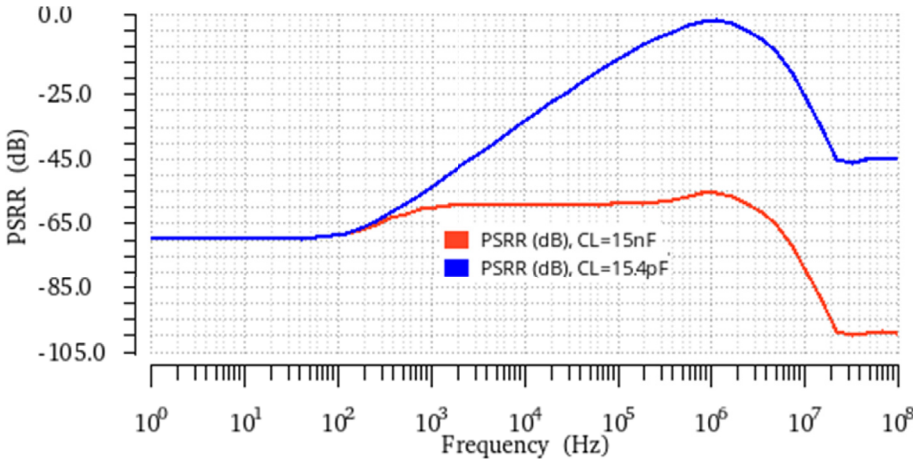

Fig. 10. PSRR of the output voltage for 1 V supply and at room temperature.

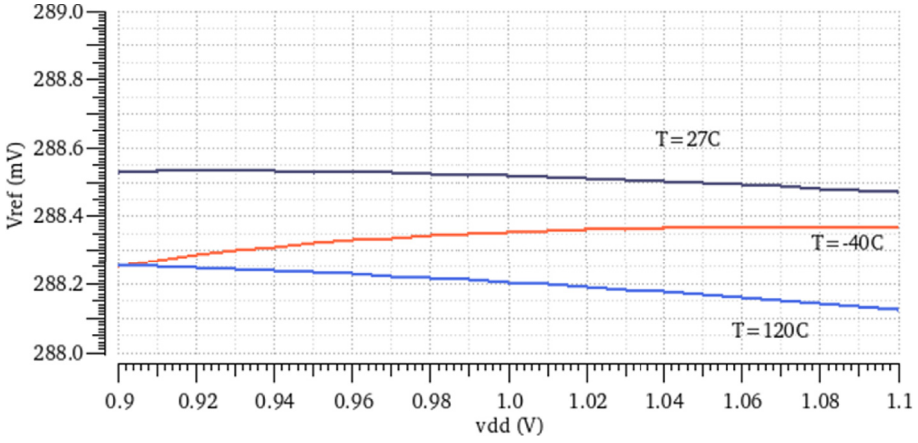

Fig. 11. Line sensitivity of the proposed voltage reference at 27 °C, −40 °C and 120 °C.

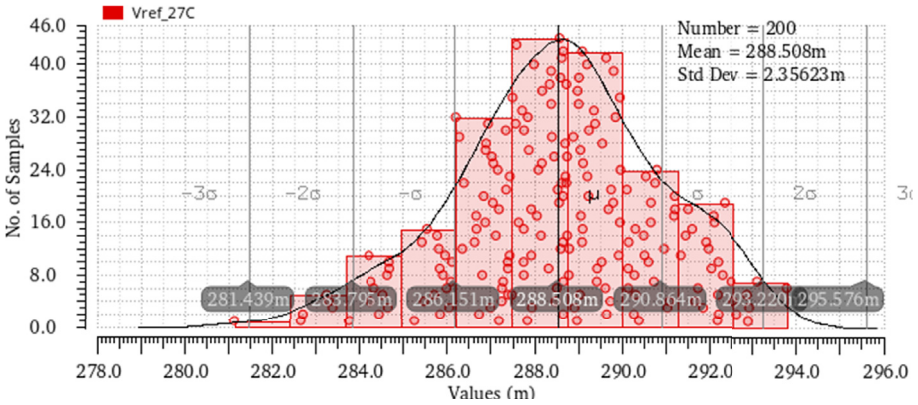

Fig. 12. Monte Carlo simulation results at 27 °C at the supply voltage of 1 V.

MP6 loaded with R_4 //C_4. The phase margin is 89.39° and the gain margin is 41.51 dB.

Fig. 10 shows the PSRR of the output voltage. At 1 Hz the PSRR is −69.85 dB. An external shunt capacitor would raise PSRR at high frequencies drastically and reduce the RMS noise, e.g., for a 10 nF capacitor the PSRR is −55.1 dB at 1 MHz and the RMS noise drops to 17.96 μV from 1 Hz to 100 MHz. For a 15 nF (C_4=C_L) capacitor, PSRR is also shown in Fig. 10. The line sensitivity of the output is depicted in Fig. 11, where the supply voltage varies from 0.9 V to 1.1 V, and it equals 0.03% at 27 °C, 0.056% at −40 °C and 0.064% at 120 °C.

Table 1 summarizes the overall SPECTRE simulated performance of the proposed sub-1V CMOS reference voltage generator. Table 2 compares it with the performance of other works in the literature.

From Table 2 it can be seen that the proposed topology has comparable temperature coefficient with that in Ref. [17], yet in Ref. [17] the temperature range is limited to 80 °C. The proposed topology exhibits the second best temperature coefficient, after that in Ref. [9], both operating within a temperature range of 165 °C. The proposed work however can

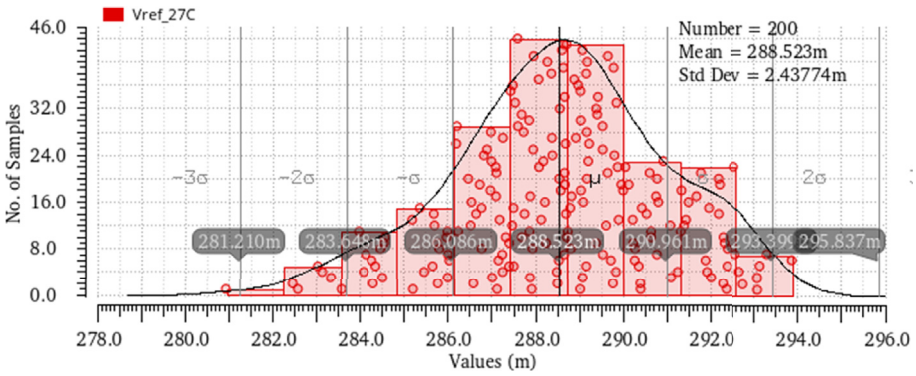

Fig. 13. Monte Carlo simulation results at 27 °C at the supply voltage of 0.9 V.

Table 1
Performance summary of the proposed sub-1V CMOS reference voltage generator.

Schematic Simulations Results	
CMOS Process	Standard 90 nm CMOS
Devices	Standard 1 V MOSFET
Nominal Supply Voltage (V_{dd})	1 V
Power Consumption (μW)	452
Output Reference Voltage (mV)	288.52
Temperature Range (°C)	−40 to 125
Temperature Coefficient, TC (ppm/°C)	6.81
PSRR at 1 Hz (dB) at 27 °C	−69.85
Line Sensitivity at 27 °C	0.03%
Total reference voltage variation, $\Delta V_{ref}/V_{ref}$ over 32 process corners: supply voltage varies from 0.9 V to 1.1 V in the temperature ranges from −40 °C to 125 °C	3.62%
$3\sigma/V_{ref}$ at 1 V at 27 °C	2.45%
$3\sigma/V_{ref}$ at 0.9 V at 27 °C	2.53%
Output reference voltage RMS Noise within the bandwidth 1 Hz to 100 MHz, at 27 °C (μV)	279

operate with a minimum supply voltage of 0.9 V versus 1.08 V of that in Ref. [9]. The presented work demonstrates a low temperature coefficient of 6.93 ppm/°C within the extended range from −50 °C to 150 °C and exhibits a PSRR at DC of −69.85 dB, which is better than that of [9]. Compared to Ref. [9] the proposed BGR attains an overall reference voltage variation of 3.62%, over PVT, versus 2.4%, over PVT, of that in Ref. [9]. In comparison with the work in Ref. [4], the proposed topology achieves better reference voltage output accuracy over PVT, 3.62% versus 6.6%, within the same supply voltage range, 0.9 V–1.1 V, and within the same temperature range from −40 °C to 125 °C, while no external components are used for stability or filtering.

4. Conclusions

In this paper a low complexity sub-1V CMOS reference voltage generator circuit was presented achieving an overall output reference voltage sensitivity of 3.62% over process, supply and temperature variation within a temperature range of 165 °C when the supply voltage varies from 0.9 V to 1.1 V.

It has low output voltage sensitivity with a temperature coefficient of 6.81 ppm/°C, within the range from −40 °C to 125 °C, and, 6.93 ppm/°C within the extended range from −50 °C to 150 °C. It exhibits a PSRR equal to −69.85 dB at 1 Hz and moderate power consumption without the requirement of external large capacitors for filtering or stability, large resistors or trimming.

Table 2
Performance comparison of the proposed sub-1V CMOS reference voltage generator with others in the literature.

Ref.	Tech.	$V_{dd,min}$ (Volts)	V_{dd} (Volts)	TC (ppm/^{0}C)	ΔT (^{0}C)	I_{dd}/P_{dc} (μA)/(μW)	PSRR (dB)	LNR (%)	$3\sigma/V_{ref}$ (%)	Area (mm)^2
[2]	0.4 μm	0.84	2.2–4	–	27 to 125	2.2	–	–	2.9	0.1
[4]	90 nm CMOS	0.9	0.9–1.5	23.66	−40 to 125	208	−52.78 @ DC	0.74	2.64	0.066
[6]	0.5 μm BiCMOS	0.85[b], 1[c]	1–5	14	−40 to 125	20	–	0.0048	0.56	0.4
[7]	0.5 μm BiCMOS	1	1–5	11	−40 to 125	20	–	–	1	0.4
[9]	65 nm CMOS	1.08	1.08–1.32	2.42	−40 to 125	155	−54	–	0.129	0.04
[12]	0.18 μm CMOS	0.5–0.9	0.5–0.9	33.3	−25 to 80	-/0.04	−62@100 Hz	0.059	2.28	0.058
[13]	0.18 μm CMOS	0.55–1	0.55–1	29.2	−45 to 140	-/0.083	−62@100 Hz	0.11	2.4	0.061
[14]	0.5 μm CMOS	0.95	3.3	17	−40 to 125	10	–	–	–	0.109
[15]	0.18 μm CMOS	–	1–2.4	18.5	−45 to 90	0.83	–	1	–	0.008
[16]	90 nm CMOS	1	1.05–1.35	–	−20 to 90	1.3	–	–	–	–
[17]	0.18 μm CMOS	–	1–2.2	6.6	−10 to 70	160	–	0.16	–	–
[19]	0.18μm CMOS	>0.65	>0.65	–	0 to 120	0.6/0.39	−52.5@100 Hz	–	0.81	0.08
[20]	0.13 μm CMOS	1–3.3	1–3.3	48	−40 to 85	1/-	−44@100 Hz	0.19	–	0.02
[21]	0.13 μm CMOS	0.6–1.8	0.6–1.8	7.90476	−25 to 80	0.622/0.373	−80@100 Hz	0.015	4.14	0.036
[22]	0.18 μm CMOS	0.7–1.8	0.7–1.8	14.649	−32 to 125	-/2.7	−28@l00 Hz	–	–	0.023
[23]	0.18 μm CMOS	0.65–1.8	0.65–1.8	47.894	−60 to 130	5.33/4	–	0.503[a]	–	0.039
This work	90 nm CMOS	0.9	0.9–1.1	6.81 6.93	−40 to 125 −50 to 150	452	−69.85@1 Hz	0.03	2.45@1 V 2.5@0.9 V	–

[a] mu from Monte Carlo simulation.
[b] 0.85 @ 20 °C.
[c] 1 @ −40 °C.

Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mejo.2019.05.023.

References

[1] R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, 3nd edition, John Wiley & Sons, IEEE Press, New Jersey, 2010.
[2] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, K. Sakui, A CMOS bandgap reference circuit with sub-1-V operation, IEEE J. Solid State Circ. 34 (1999) 670–674.
[3] P. Malcovati, F. Maloberti, M. Pruzzi, C. Fiocchi, Curvature compensated BiCMOS bandgap with 1V supply voltage, in: ESSCIRC, 2000, pp. 7–10.
[4] A. Tsitouras, F. Plessas, M. Birbas, J. Kikidis, G. Kalivas, A sub-1V supply CMOS voltage reference generator, Int. J. Circ. Theor. Appl. 40 (8) (2012) 745–758.
[5] V. Ivanov, R. Brederlow, J. Gerber, An ultra low power bandgap operational at supply from 0.75V, IEEE J. Solid State Circ. 47 (2012) 1515–1523.
[6] V.V. Ivanov, K.E. Sanborn, I.M. Filanovfsky, Bandgap voltage references with 1V supply, in: ESSCIRC, 2006, pp. 311–314.
[7] K.E. Sanborn, Dongsheng Ma, V.V. Ivanov, A sub-1-V Low noise Bandgap voltage reference, IEEE J. Solid State Circ. 42 (2007) 2466–2481.
[8] A.J. Annema, P. Veldhorst, G. Doornbos, B. Nauta, A sub-1V bandgap voltage reference in 32nm FinFET technology, in: IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 2009, pp. 332–333.
[9] G. Souliotis, F. Plessas, S. Vlassis, A high accuracy voltage reference generator, Microelectron. J. 75 (2018), 61-47.
[10] J. Geng, Y. Zhao, H. Zhao, A high-order curvature-corrected CMOS bandgap voltage reference with constant current technique, Int. J. Circ. Theor. Appl. (2012), https://doi.org/10.1002/cta.1836.
[11] M. Wiessflecker, G. Hofer, G. Holweg, H. Reinisch, W. Pribyl, A sub 1V self clocked switched capacitor bandgap reference with a current consumption of 180nA, in: IEEE International Symposium on Circuits and Systems (ISCAS), 2012.
[12] J. Mu, L. Liu, Z. Zhu, Y. Yang, A 58-ppm/◦C 40-nW BGR at supply from 0.5V for energy harvesting IoT devices, IEEE Trans. Circ. Systems II: Expr. Briefs 64 (2017) 752–756.
[13] L. Liu, J. Mu, Z. Zhu, A 0.55-V, 28-ppm/°C, 83-nW CMOS sub-BGR with ultra low power curvature compensation, IEEE Trans. Circ. Syst. Regular Pap. 65 (2018) 95–106.
[14] J. Doyle, J.L. Young, B.K. Yong, H. Wilsch, F. Lombardi, A CMOS subbandgap reference circuit with 1-V power supply voltage, IEEE J. Solid State Circ. 39 (2004) 252–255.
[15] Jirong Ma, Yongming Li, Chun Zhang, Zhihua Wang, A 1V ultra-low power high precision CMOS voltage reference, in: EDSSC, 2007, pp. 847–850.
[16] G. di Naro, G. Lombardo, C. Paolino, G. Lullo, A low-power fully-Mosfet voltage reference generator for 90-nm CMOS technology, in: International Conference on IC Design & Technology, ICICDT, 2006, pp. 1–4.
[17] I. Nissinen, J. Kostamovaara, A low voltage CMOS constant current-voltage reference circuit, in: International Symposium on Circuits and Systems, 2004, ISCAS, vol. 1, 2004, pp. 381–384.
[18] Rohit Singh, Kumar Singh Amit, Sonal Singhal, Feedback driven temperature and supply compensated sub-0.5 V reference generator, in: 9th International Conference on Industrial and Information Systems (ICIIS), 2014.
[19] P.B. Basyurt, E. Bonizzoni, D.Y. Aksin, F. Maloberti, Voltage reference architectures for low-supply-voltage low-power applications, Microelectron. J. 46 (2015) 1012–1019.
[20] A. Parisia, A. Finocchiarob, G. Palmisano, An accurate 1-V threshold voltage reference for ultra-low power applications, Microelectron. J. 63 (2017) 155–159.
[21] L. Liu, Y. Song, J. Mu, W. Guo, Z. Zhu, Y. Yang, A high accuracy CMOS subthreshold voltage reference with offset cancellation and thermal compensation, Microelectron. J. 60 (2017) 102–108.
[22] C.M. Andreou, J. Georgiou, A 0.7 V, 2.7 μW, 12.9 ppm/◦C over 180◦C CMOS subthreshold voltage reference, Int. J. Circ. Theor. Appl. 45 (2017) 1349–1368. https://doi.org/10.1002/cta.2292.
[23] C.M. Andreou, J. Georgiou, A 0.75-V, 4-μW, 15-ppm/◦C, 190◦C temperature range, voltage reference, Int. J. Circ. Theor. Appl. 44 (2016) 1029–1038. https://doi.org/10.1002/cta.2122.
[24] Y. Dai, D.T. Comer, D.J. Comer, C.S. Petrie, Threshold voltage based CMOS voltage reference, IEE Proc. Circ. Dev. Syst. 151 (2004) 58–62.
[25] P.K.T. Mok, K.N. Leung, Design Considerations of Recent Advanced Low-Voltage Low-Temperature-Coefficient CMOS Bandgap Voltage Reference, CICC, 2004, pp. 635–642.
[26] A. Anvesha, M.S. Baghini, A sub-1V 32nA process, voltage and temperature invariant voltage reference circuit, in: 26th International Conference on VLSI Design and the 12th International Conference on Embedded Systems, 2013, pp. 136–141.
[27] D. Albano, F. Crupi, F. Cucchi, G. Iannaccone, A picopower temperature-compensated, subthreshold CMOS voltage reference, Int. J. Circ. Theor. Appl. (2013), https://doi.org/10.1002/cta.1925.
[28] Y. Zeng, Y. Huang, Y. Luo, H.Z. Tan, An ultra-low-power CMOS voltage reference generator based on body bias technique, Microelectron. J. 44 (2013) 1145–1153.
[29] Seok, Kim, Sylvester, Blaauw, A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V, IEEE J. Solid State Circ. 47 (10) (2012) 2534–2545.
[30] M. Seok, G. Kim, D. Sylvester, D. Blaauw, A 0.5V 2.2pW 2-transistor voltage reference, in: IEEE Custom Integrated Circuits Conference, 2009, pp. 577–580.
[31] R.L. Geiger, P.E. Allen, N.R. Strader (Eds.), VLSI Design Techniques for Analog and Digital Circuits, McGraw-Hill College, March 1, 1989.