A Class of 1-Bit Multi-Step Look-Ahead Σ-Δ Modulators

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***Abstract*— Digital Multi-Step Look-Ahead (MSLA) 1-bit Σ-Δ modulators are introduced. They improve upon the stability and noise shaping characteristics of conventional 1-bit Σ-Δ modulators by minimizing quantization error metrics of the current and future output samples. The mathematical model of the proposed MSLA modulators is analyzed. It is shown that the MSLA modulators are equivalent to a system of conventional Σ-Δ modulators in parallel, but with a common multi-input 1-bit quantizer instead of a typical one. The properties of this multi-input quantizer are studied and the transfer functions of the MSLA modulators are derived. Simulation results are presented demonstrating the advantages of the MSLA modulators over conventional 1-bit Σ-Δ ones in a number of applications. A parametric hardware architecture of the MSLA modulators is presented offering an adjustable trade-off between performance and hardware complexity based on the number of look-ahead steps. Finally, a FPGA implementation of a MSLA modulator is presented along with simulation results.**

***Index Terms*— 1-bit quantization, all-digital, DAC, look-ahead, modulator, noise shaping, optimization algorithm, sigma-delta.**

I. Introduction

THE noise shaping characteristics and simplicity of Σ-Δ modulators have led to their widespread usage in high-resolution Digital-to-Analog Converters (DAC), Analog-to-Digital Converters (ADC) and time-to-digital converters. Initially, Σ-Δ modulators were designed as purely analog or mixed-signal circuits [1]. Because digital circuits are unaffected by process, voltage and temperature variations, and are becoming faster, more energy-efficient and smaller with the scaling of IC process technologies, there has been an increasing interest in all-digital Σ-Δ modulators [2]. These modulators are used as components in a variety of applications ranging from traditional data converters to all-digital transmitters [3], [4], frequency synthesizers [5], [6] and PLLs [7]. Moreover, a Σ-Δ DAC is the combination of an all-digital Σ-Δ modulator followed by a 1-bit or few-bit DAC, which is much easier to design than a multi-bit one.

Since Σ-Δ modulation is based on a feedback loop, stability requirements are crucial for a successful design. These requirements pose restrictions to the noise transfer function (NTF) design space and limit the allowable input signal range [1], [8]. The quantizer resolution of the Σ-Δ modulator also affects its stability [9]. Single-bit modulators are more susceptible to instability than multi-bit ones, but the tendency towards DAC-less all-digital architectures necessitates the use of 1-bit Σ-Δ modulators. Furthermore, 1-bit quantization is inherently linear since there are only two signal levels and thus the matching requirements between different components are significantly relaxed.

Many works have dealt with the stability analysis of Σ-Δ modulators. Parallel decomposition of high-order modulators [10], limit cycle investigation [11] and quasi-linear modeling using the describing function method [12] are some of the proposed stability analysis techniques, while in [13] the stability of band-pass Σ-Δ modulators is considered.

This work proposes an all-digital Multi-Step Look-Ahead (MSLA) 1-bit modulation scheme which improves on the stability of conventional Σ-Δ modulators. This is achieved by taking into account future input samples for the determination of the current output. The number of look-ahead steps is a design parameter which is selected in order to obtain the desired balance between complexity and stability improvement. The enhanced stability offers more flexibility in the selection of the NTF, allowing for NTFs with increased pass-band bandwidth and out-of-band gain. This results in higher in-band noise attenuation and thus higher signal-to-noise-ratio (SNR).

In section II the process of 1-bit quantization is viewed as an optimization algorithm and the MSLA algorithm is introduced. The mathematical analysis of the MSLA modulator follows in section III, where its relation to conventional Σ-Δ and other look-ahead modulators is investigated. In section IV simulation results for a variety of applications are presented and the stability improvement offered by the MSLA modulator is quantified. Section V introduces a digital hardware architecture for the implementation of the MSLA modulator and a test-case FPGA implementation is presented. Finally, section VI concludes the discussion.

II. 1-Bit Quantization as an Optimization Algorithm

The process of 1-bit quantization is viewed as an optimization problem. The high resolution input sequence is passed through a band-selective filter. The filter is chosen to have a profile similar to the information spectrum of the input sequence. This maintains the information while pushing the

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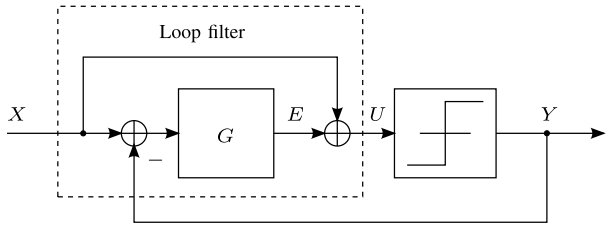

Fig. 1. The 1-bit error-feedback Σ-Δ modulator.

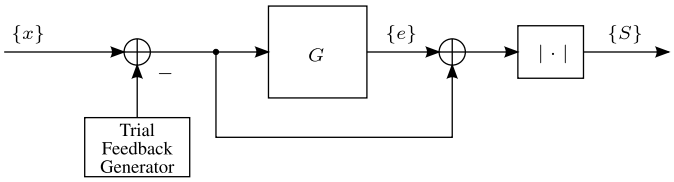

Fig. 2. Cost function calculation block diagram.

Minimizing variables:					v	
0	1	...	$n-2$	$n-1$	n	**Cost**
y_0	y_1	...	y_{n-2}	y_{n-1}	−1	$S_{0,n}(-1)$
y_0	y_1	...	y_{n-2}	y_{n-1}	1	$S_{0,n}(1)$

Previous outputs; Trial FB seq.

Fig. 3. Overview of the EF SDM optimization algorithm.

1-bit quantization error power outside the information spectrum minimizing the total in-band quantization error.

In [14] it is shown that the error-feedback Σ-Δ modulator (EF SDM) produces a 1-bit output sequence with the minimum quantization error power when a first-order loop filter is used. This Σ-Δ modulator forms the basis for the development of the MSLA modulator. In the following analysis it is shown that the EF SDM depicted in Fig. 1 may be viewed as an optimization algorithm. The MSLA modulator is then introduced as an extension of the EF SDM, where future input values are used as part of the optimization process.

For the reader's convenience, an overview of the notation used in this and the next sections is presented in Appendix A.

A. The 1-Bit Error-Feedback Σ-Δ Modulator

From inspection of the system in Fig. 1 it is

$$U(z) = X(z) + G(z)\big(X(z) - Y(z)\big) \tag{1}$$

where $X(z)$, $Y(z)$ and $U(z)$ are the z-transforms of the input, output and quantizer input respectively and $G(z)$ is the transfer function of filter G. The quantization error is $N(z) = Y(z) - U(z)$, which combined with (1) and eliminating $U(z)$ gives $Y(z) = X(z) + 1/(1+G(z))N(z)$. Thus, the signal and noise transfer functions are $STF(z) \equiv Y(z)/X(z)|_{N(z)=0} = 1$ and $NTF(z) \equiv Y(z)/N(z)|_{X(z)=0} = 1/\big(1+G(z)\big)$ respectively. A realizable EF SDM requires at least a single sample delay in filter G, which also translates to $NTF(\infty) = 1$ [1]. So, the general form of $G(z)$ is

$$G(z) = \frac{1 - NTF(z)}{NTF(z)} = \frac{\sum_{i=1}^{\ell} b_i z^{-i}}{1 + \sum_{i=1}^{m} a_i z^{-i}} \tag{2}$$

where ℓ, m are the orders of the numerator and the denominator polynomials respectively. Filter G is also known as the comparison filter.

In [15] it is shown that the EF SDM is equivalent to an optimization algorithm and its output is determined by minimizing the cost function[1]

$$S_{0,n}(v) = |x_n + e_n - v|. \tag{3}$$

Here, x_n is the current input, e_n is the current comparison filter output and $v \in \{\pm 1\}$ is the minimizing variable. The output y_n is the value of v minimizing the cost function $S_{0,n}$, i.e.

$$y_n = \underset{v\in\{\pm 1\}}{\arg\min}\, S_{0,n}(v). \tag{4}$$

[1]The first subscript 0 indicates that the cost function takes into account 0 look-ahead steps, while the second subscript n denotes that it is calculated at time index n.

The solution of (4) is $y_n = \operatorname{sgn}(e_n + x_n)$ and is implemented by the 1-bit quantizer in the EF SDM of Fig. 1. From (3) and (4) we note that the output of the 1-bit EF SDM is determined by minimizing *only* the *instantaneous* quantization error.

A block diagram of the cost function calculation of (3) is shown in Fig. 2. The negative feedback loop from the output to the input has been replaced by the trial feedback generator. At each iteration of the algorithm it generates all the possible values of v, namely -1 and 1 here. The quantization error which is the difference between the input sequence and the trial feedback generator sequence[2], i.e., $(x_0 - y_0, x_1 - y_1, \ldots, x_{n-1} - y_{n-1}, x_n - v)$, is filtered by $1 + G(z) = 1/NTF(z)$. The absolute value of the filter output is the cost function. The square of the cost function is thus equal to the filtered quantization error power.

The output selection procedure of the EF SDM by utilizing the optimization algorithm is illustrated in Fig. 3. The output sequence with the least cost is chosen and the corresponding y_n output value is appended to the output sequence. This process gives the same output sequence $\{y\}$ as the 1-bit EF SDM with the same comparison filter G.

B. The MSLA Modulator Algorithm (k Look-Ahead Steps)

A generalization of the 1-bit quantization optimization problem is possible if the minimization of the filtered quantization error is not restricted to the current input sample x_n, but incorporates the next k future input samples as well, which are also called *look-ahead* samples. It should be noted that the future input samples are not in any way predicted; they are already available and the term "future" refers to a time delay of the output sequence by k samples.

The key idea is to "search" among all the 2^{k+1} possible output sequences $\big\{(v_0, v_1, \ldots, v_k)|v_i \in \{\pm 1\}\big\}$, also known as *paths*. The MSLA algorithm assesses the 2^{k+1} paths and selects the one with the minimum total quantization error power. Then, the first element of this path is selected as the

[2]Throughout the paper we assume zero initial conditions of the filters and all signals being zero for negative time index.

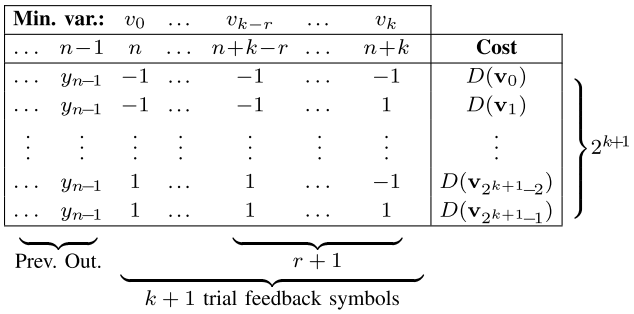

Fig. 4. Overview of the MSLA optimization algorithm.

current output. Finally, time index n is increased by one and the algorithm proceeds. This process is captured in Fig. 2 where the feedback generator outputs the 2^{k+1} possible paths generating the input to comparison filter G:

$$(x_0 - y_0, x_1 - y_1, \ldots, x_{n-1} - y_{n-1}, x_n - v_0, x_{n+1} - v_1, \ldots, x_{n+k} - v_k). \quad (5)$$

The associated costs are $\sum_{j=0}^{k} S_{j,n}(v_0, v_1, \ldots, v_j)$, where the *partial costs* $S_{j,n}$ are defined as

$$S_{j,n}(v_0, v_1, \ldots, v_j) = \left| x_{n+j} + e_{n+j} - v_j \right|^2. \quad (6)$$

Extensive simulation suggests that taking into account only the partial costs associated with the last few look-ahead samples, i.e., $j = k-r, k-r+1, \ldots, k$, as shown in Fig. 4, may result in superior stability and lower complexity at the cost of reduced SNR. In this case, the total cost of a path is given by (7) where we have set $\mathbf{v} = (v_0, v_1, \ldots, v_k)$.

$$D_n(\mathbf{v}) = \sum_{j=k-r}^{k} S_{j,n}(v_0, v_1, \ldots, v_j) \quad (7)$$

The MSLA modulator output is the value of v_0, which along with the values of $v_1, v_2, \ldots, v_k$ minimize $D_n(\mathbf{v})$, i.e.,

$$y_n = \underset{v_0 \in \{\pm 1\}}{\arg\min} \left(\min_{v_1, v_2, \ldots, v_k \in \{\pm 1\}} D_n(\mathbf{v}) \right). \quad (8)$$

Since filter G in Fig. 2 is in general an infinite impulse response (IIR) one, and thus its output depends on all previous and current input samples, the comparison filter output e_{n+j} is an implicit function of $v_0, v_1, \ldots, v_{j-1}$. Assuming G is as in (2) and since its input is given by (5), its output for $0 \le j \le k$ is

$$e_{n+j} = \sum_{i=1}^{\ell} b_i x_{n+j-i} - \sum_{i=1}^{j} b_i v_{j-i} - \sum_{i=j+1}^{\ell} b_i y_{n+j-i} - \sum_{i=1}^{m} a_i e_{n+j-i} \quad (9)$$

Instead of using the square of the absolute value for the partial cost in (6), an alternative is to use the absolute value. In this case the output of the MSLA modulator is given again by (8) and (7), but (6) is replaced by

$$S_{j,n}(v_0, v_1, \ldots, v_j) = \left| x_{n+j} + e_{n+j} - v_j \right|. \quad (10)$$

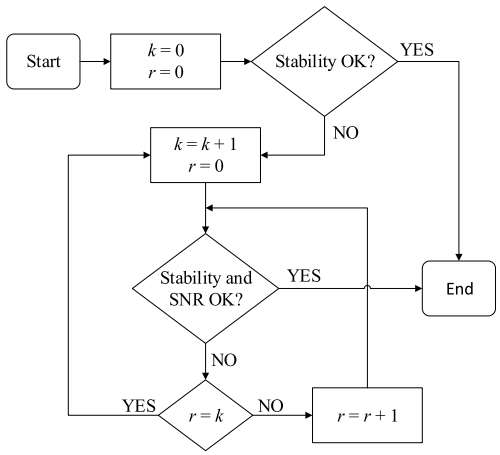

Fig. 5. r, k selection flowchart.

Using the absolute value can result in more efficient quantizer designs as it is shown later. Because of this, the focus of our analysis considers partial costs as in (10). Moreover, simulation results in subsequent sections indicate that the output spectrum does not depend significantly on either choice.

The number of partial costs used in (7) is determined by r and reflects to the complexity of the modulator. The choice of look-ahead steps k and r for a given filter G, and therefore a given NTF and STF, can be made as shown in Fig. 5.

The assessment of stability is done via simulation as with a conventional Σ-Δ modulator. This is because of the lack, to our knowledge, of an accurate theoretical model predicting stability in look-ahead modulators. A range of simulation runs with varying DC and sinusoidal input amplitudes and frequencies is typically used to provide a trustworthy estimate. The reader is referred to [1, Chapter 8] for details on the simulation procedure.

C. The Optimal Solution to the 1-Bit Quantization Problem

Let us consider the case of an input sequence of finite yet arbitrary length N. Then the optimal solution to the 1-bit quantization optimization problem in terms of SNR is obtained by solving the minimization problem

$$(y_0, y_1, \ldots, y_{N-1}) = \underset{v_0, v_1, \ldots, v_{N-1} \in \{\pm 1\}}{\arg\min} D_n(\mathbf{v}) \quad (11)$$

where $D_n(\mathbf{v}) = \sum_{j=0}^{N-1} |x_j + e_j - v_j|^2$. In this case the trial feedback generator of Fig. 2 outputs all the 2^N possible trial sequences just like the MSLA modulator. However, this time, the whole trial feedback sequence $(v_0, v_1, \ldots, v_{N-1})$ resulting in the minimum total quantization power is chosen as the output sequence $(y_0, y_1, \ldots, y_{N-1})$.

A more efficient solution to the aforementioned problem is Viterbi decoding [14], [16]. However, Viterbi decoding is only possible for filters G with a finite state machine representation, which rules out most IIR filters G with poles on the unit circle such as the ones based on a Σ-Δ modulator NTF. Note that the complexity of both approaches is prohibiting for input signals with a significant length, while they are inapplicable to real-time streaming signals. Reduced complexity techniques such

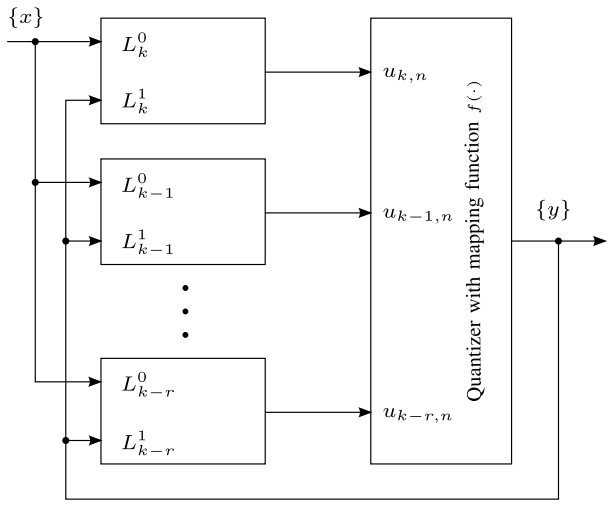

Fig. 6. The MSLA modulator efficient form system diagram.

as list decoding or M-algorithm [17] have been introduced, but their complexity remains too high. Therefore, even lower complexity look-ahead algorithms are needed, such as the MSLA.

III. MSLA Modulator Efficient Form

Brute force solution of the MSLA optimization problem in (8) via (7) and (10) requires the computation of 2^{k+1} cost values in every time step. Note also that the total cost function D_n depends on time n. A more efficient approach instead is to convert the optimization-form of the MSLA modulator into the equivalent nonlinear feedback system form in Fig. 6. The system is comprised of $r+1$ two-input filters and a multivariable nonlinear function $f(\cdot) : \Re^{r+1} \to \{\pm 1\}$. Function f can be considered as the equivalent to the 1-bit quantizer of the conventional Σ-Δ modulator.

Following some algebraic manipulation in Appendix B an equivalent expression of (10) for $k-r \le j \le k$ is

$$S_{j,n}(v_0, v_1, \ldots, v_j) = \left| u_{j,n} - \sum_{i=0}^{j} c_{j,i} v_{j-i} \right| \tag{12}$$

which is a function of a linear combination of $v_0, v_1, \ldots, v_j$, parameterized on $u_{j,n}$, where

$$u_{j,n} = \sum_{i=0}^{j} c_{j,i} x_{n+j-i} + \sum_{i=j+1}^{j+\ell-1} c_{j,i} \left(x_{n+j-i} - y_{n+j-i} \right) + \sum_{i=0}^{m-1} d_{j,i} e_{n-i}. \tag{13}$$

Constant coefficients $c_{j,i}$ and $d_{j,i}$ result from the comparison filter G and are derived in Appendix B. Also note that $u_{j,n}$ is independent of $v_0, v_1, \ldots, v_j$. For the special case of $j=0$, $u_{0,n} = x_n + e_n$ and $S_{0,n}(v_0) = |u_{0,n} - v_0|$.

Substituting (12) into (7) and using (8) gives the following expression for the MSLA modulator output

$$y_n = f\left(u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n}\right) \tag{14}$$

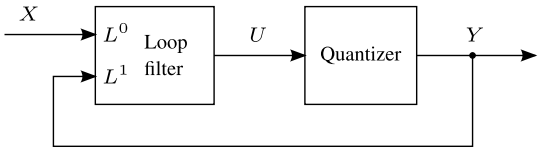

Fig. 7. The general Σ-Δ modulator system diagram.

where function f is defined as the solution of the time-invariant (i.e., f does *not* depend on n) combinatorial problem

$$f\left(u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n}\right) = \arg\min_{v_0 \in \{\pm 1\}} \left(\min_{\substack{v_1, v_2, \ldots, v_k \\ \in \{\pm 1\}}} \sum_{j=k-r}^{k} \left| u_{j,n} - \sum_{i=0}^{j} c_{j,i} v_{j-i} \right| \right). \tag{15}$$

This equation forms the foundation of the proposed methodology. The behavior of function $f(\cdot)$ is investigated in Section III-B.

Having function f we now derive filters $L_j^{0,1}(z)$, $k-r \le j \le k$ to complete the MSLA modulator equivalent in Fig. 6. For $j=0$ (9) gives $e_n = \sum_{i=1}^{\ell} b_i (x_{n-i} - y_{n-i}) - \sum_{i=1}^{m} a_i e_{n-i}$. Its z-transform is

$$E(z) = G(z)\big(X(z) - Y(z)\big) \tag{16}$$

where $G(z)$ is defined in (2).

Taking the z-transform of (13) with respect to n and combining it with (16) yields

$$U_j(z) = L_j^0(z) X(z) + L_j^1(z) Y(z) \tag{17}$$

where $U_j(z)$ is the z-transform of the j-th filter output (Fig. 6) and

$$L_j^0(z) = \sum_{i=0}^{j+\ell-1} c_{j,i} z^{j-i} + G(z) \sum_{i=0}^{m-1} d_{j,i} z^{-i} \tag{18}$$

$$L_j^1(z) = -\sum_{i=j+1}^{j+\ell-1} c_{j,i} z^{j-i} - G(z) \sum_{i=0}^{m-1} d_{j,i} z^{-i} \tag{19}$$

with $k-r \le j \le k$.

Equations (14) and (17) establish the equivalence of the MSLA modulator system in Fig. 6 with that in Fig. 2. The form in Fig. 6 may be considered as an extension of the general Σ-Δ modulator system shown in Fig. 7 [1].

A. MSLA Modulator Transfer Functions

As a first-order approximation, the multi-input quantizer function f in Fig. 6 is replaced by $r+1$ correlated additive noise sources and loop gains K_j, $k-r \le j \le k$ as shown in Fig. 8. In the $r+1$ resulting loops the noise sources are such that added to their corresponding filter output produce the same output y. This means that the transfer functions may be derived using any of the $r+1$ simple loops.

To proceed we choose to define the NTF based on the first (top) of the $r+1$ loops. The reasoning for this is that the first filter (L_k^0, L_k^1) incorporates the highest look-ahead order and therefore captures most of the MSLA modulator dynamics.

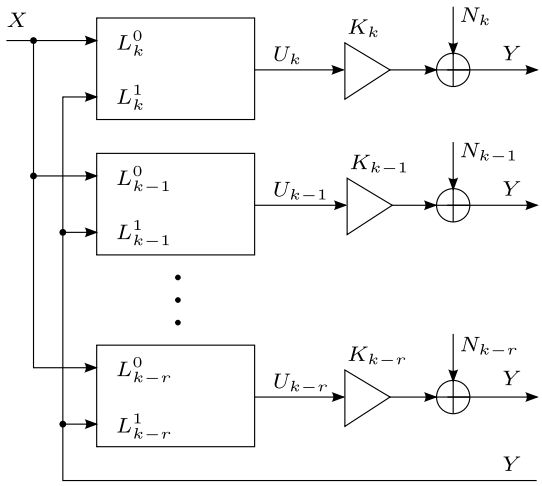

Fig. 8. The MSLA modulator efficient form system diagram with the quantizer replaced by noise sources.

To derive the NTF we set $X(z) = 0$ and we define $N_k(z)$ as the z-transform of the noise source added to the filter output $K_k U_k(z)$. Then

$$Y(z) = N_k + K_k L_k^1(z) Y(z). \tag{20}$$

So, the NTF is

$$NTF_{\text{MSLA}} \equiv \left.\frac{Y}{N_k}\right|_{X=0} = \frac{1}{1 - K_k L_k^1}. \tag{21}$$

The STF is

$$STF_{\text{MSLA}} \equiv \left.\frac{Y}{X}\right|_{N_i=0} = \frac{K_k L_k^0}{1 - K_k L_k^1}. \tag{22}$$

Following the analysis in [1, Section 2.1], K_k is calculated by minimizing the average power of the quantizer's linear model error $y_n - K_k u_{k,n}$. This leads to

$$K_k = \frac{\langle y, u_k \rangle}{\langle u_k, u_k \rangle} = \frac{\langle f(\mathbf{u}), u_k \rangle}{\sigma_{u_k}^2} \tag{23}$$

where $\langle a, b \rangle$ is defined either stochastically as $E[ab]$ or deterministically as the time average $\lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N} a_n b_n$ of the sequences a_n and b_n. The impact of the other loop filters is included in the quantizer gain K_k, and therefore in the NTF and STF, via the inner product of $f(\mathbf{u})$ with u_k. The value of K_k can be derived via simulation. The expressions for the NTF and STF of the MSLA modulator are comparable to the ones obtained for the conventional Σ-Δ modulator depicted in Fig. 7 [1].

To avoid confusion, please note that in the remainder of the paper the NTF of the MSLA modulator is denoted as NTF_{MSLA}. The notation NTF is reserved for the initial EF SDM NTF used as the basis for the MSLA modulator comparison filter G defined in (2).

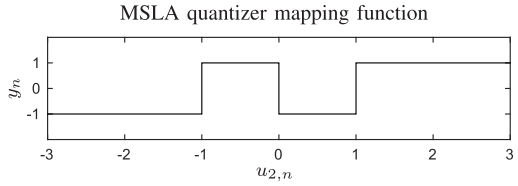

Fig. 9. The MSLA modulator quantizer function f for $NTF = (1 - 2\cos(2\pi \cdot 0.365)z^{-1} + z^{-2})^2$, $k = 2$ and $r = 0$.

B. MSLA Modulator Quantizer Aspects

An alternative expression for the MSLA modulator quantizer function $f(\cdot)$ can be derived by defining

$$\tilde{D}(\mathbf{u}, \mathbf{v}) = \sum_{j=k-r}^{k} \left| u_{j,n} - \sum_{i=0}^{j} c_{j,i} v_{j-i} \right| \tag{24}$$

where $\mathbf{u} = (u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n})$ and $\mathbf{v} = (v_0, v_1, \ldots, v_k)$. Since the output of the modulator is determined solely by the value of v_0 (see (15)), we can distinguish between two sets of values of $\tilde{D}(\mathbf{u}, \mathbf{v})$, i.e.,

$$A(\mathbf{u}) = \left\{ \tilde{D}(\mathbf{u}, \mathbf{v}) : \mathbf{v} = (1, v_1, v_2, \ldots, v_k) \mid v_i \in \{\pm 1\} \right\} \text{ and}$$
$$B(\mathbf{u}) = \left\{ \tilde{D}(\mathbf{u}, \mathbf{v}) : \mathbf{v} = (-1, v_1, v_2, \ldots, v_k) \mid v_i \in \{\pm 1\} \right\}$$

with each set containing 2^k elements. Given the input vector $\mathbf{u}$, the modulator output is

$$f(\mathbf{u}) = \begin{cases} 1 & \text{if} \quad \min A(\mathbf{u}) \le \min B(\mathbf{u}) \\ -1 & \text{otherwise.} \end{cases} \tag{25}$$

Thus, the domain space $\Re^{r+1}$ of f is partitioned into the two subsets $f^{-1}(\{+1\})$ and $f^{-1}(\{-1\})$. Note that the minimization process is independent of time index n and thus f is a static function.

The following examples illustrate the form of f as given by (25) for different NTFs and values of k and r:

Example 1: The quantizer function $f(\cdot)$ of a MSLA modulator with $NTF = (1 - 2\cos(2\pi \cdot 0.365)z^{-1} + z^{-2})^2$, $k = 2$ and $r = 0$ is

$$f(u_{2,n}) = \begin{cases} 1, & u_{2,n} \in [-1, 0) \cup [1, \infty) \\ -1, & u_{2,n} \in (-\infty, -1) \cup [0, 1). \end{cases} \tag{26}$$

It can also be expressed using signum functions as

$$f(u_{2,n}) = \text{sgn}\left(u_{2,n} + 1\right) \cdot \text{sgn}\left(u_{2,n}\right) \cdot \text{sgn}\left(u_{2,n} - 1\right). \tag{27}$$

In this case, the effect of the MSLA modulator is the inversion of the quantizer output in the interval $[-1, 1]$ compared to a conventional Σ-Δ modulator 1-bit quantizer (Fig. 9).

Example 2: Let $NTF = (1 - z^{-1})^3$, $k = 2$ and $r = 0$. The resulting quantizer function is the same as that of a conventional Σ-Δ quantizer, i.e., $f(u_{2,n}) = \text{sgn}(u_{2,n})$. This is generally true in the case that $|c_{k,k}| > \sum_{i=0}^{k-1} |c_{k,i}|$ and $r = 0$.

Example 3: The previous examples dealt only with $r = 0$, so y_n was a function of $u_{k,n}$ only. If $r = 1$, then $y_n = f(u_{k-1,n}, u_{k,n})$ and the mapping from $\mathbf{u} = (u_{k-1,n}, u_{k,n})$ to y_n is formed by regions on a plane. This is seen in Fig. 10(a),

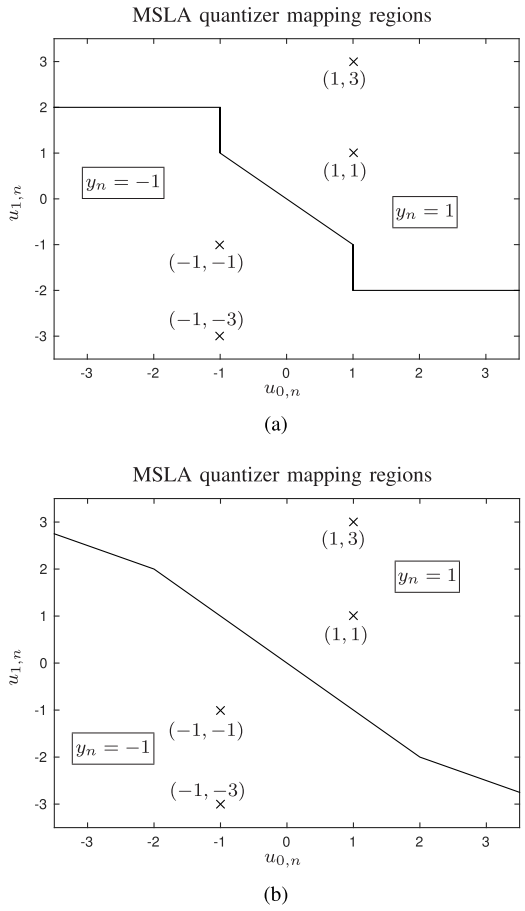

Fig. 10. Mapping regions from $u_{0,n}$, $u_{1,n}$ to y_n for the MSLA modulator with $NTF = (1 - z^{-1})^2$, $k = 1$, $r = 1$ and a total cost function employing (a) Manhattan or (b) Euclidean distance.

where the MSLA modulator is configured with $(1 - z^{-1})^2$ as the comparison filter NTF, $k = 1$ and $r = 1$.

Fig. 10(a) depicts a Voronoi diagram [18] in two-dimensional space. The output of the modulator is determined by the least Manhattan distance of the quantizer input vector $\mathbf{u}$ from a set of points which depend on the coefficients $c_{j,i}$. These points are also shown in Fig. 10(a). The coordinates of these points in u_j axes are given by $\sum_{i=0}^{j} c_{j,i} v_{j-i}$ for all possible values of $\mathbf{v} = (v_0, v_1, \ldots, v_k)$, resulting in a total of 2^{k+1} points in $(r + 1)$-dimensional space.

Example 4: In the previous example, if Euclidean distance is used, i.e., $S_{j,n}$ are given by (6) instead of (10), the corresponding Voronoi diagram is shown in Fig. 10(b). In this case the output of the modulator is determined by the least Euclidean distance of the quantizer input vector $\mathbf{u}$ from the same set of points as in the previous example.

Voronoi diagrams employing Manhattan distance, and thus the corresponding MSLA modulator quantizer mapping regions, consist only of horizontal, vertical and ±45° dividing lines (planes) [18]. The dividing lines (planes) of Euclidean distance Voronoi diagrams on the other hand are not subject to this restriction. The hardware implementation of the MSLA quantizer is either based on a LUT or on a number of comparisons involving its inputs. So, apart from some special cases, using the Manhattan distance results in a simpler hardware implementation of the quantizer. This is another reason why this work deals mostly with the Manhattan distance case.

TABLE I
1-BIT LOOK-AHEAD Σ -Δ COMPLEXITY COMPARISON

Description	Filter output calc.	Memory	Other
Full LA	$N \cdot 2^N$	–	Select min.
LA with re-use of results	$2^{N+1} - 2$	$2^N - 1$	Select min.
LA with select & cont.	2^N	2^N	Select min.
LA with linear decomp.	2^{N-1}	2^N	Select min.
Basic pruned LA	$N \cdot 2^N$	$N \cdot L$	Path sorting
Pruned LA with re-use of results	$2^{N+1} - 2$	$N \cdot L + 2^N - 1$	Path sorting
Efficient trellis Σ-Δ modulation	$2 \cdot M$	$M \cdot L$	Uniqueness of last N symbols + path sorting
Pruned tree Σ-Δ modulation (M-algorithm)	$2 \cdot M$	$M \cdot L$	Path sorting
MSLA Σ-Δ modulation	$r+1$	–	$(r+1)$-input 1-bit quantizer logic

As a test-case, the mapping functions of Fig. 10 were synthesized for a Xilinx Kintex-7 target device assuming two 7-bit inputs. After logical optimization the Manhattan distance quantizer was comprised of one 5-input LUT, three 6-input LUTs and one D flip-flop, whereas the Euclidean distance one had in addition one 3-input LUT, one 6-input LUT and one 2:1 multiplexer. The difference in hardware complexity becomes even more pronounced as the bit width or the number of quantizer inputs is increased.

In the previous examples we considered only $r = 0$ or $r = 1$. The results are similar when $r > 1$, but the mapping regions are formed in a $(r + 1)$-dimensional space and are not convenient for demonstration.

C. Complexity Comparison

In the previous sections it was shown that the MSLA modulator is composed of $r+1$ loop filters and an $(r+1)$-input quantizer. This setup offers significantly lower computational complexity than other look-ahead Σ-Δ implementations. Table I summarizes the complexity of a variety of look-ahead algorithms. These results are not bound to any specific hardware implementation, but they are based on the computational complexity of each algorithm. All of these algorithms are discussed thoroughly in [19], while the M-algorithm is also used in [17]. The first four algorithms of Table I are based on the full-look ahead algorithm and the next four ones are variations of the M-algorithm.

The full look-ahead algorithm is derived from the MSLA one if we use Euclidean distance and let $r = k = N$, where N is the number of look-ahead samples. As it can be seen in the first four rows of Table I its complexity remains exponential and therefore its use becomes prohibiting for large values of N. Typical values are $N = 10$.

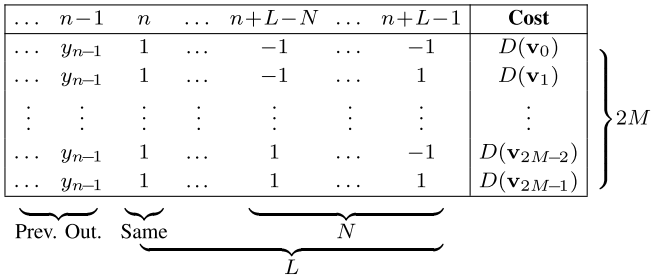

Fig. 11. Overview of the M-algorithm optimization algorithm.

Reduced complexity techniques such as list decoding or M-algorithm [17] have been suggested for use in all-digital transmitters. M-algorithm does not assess 2^{k+1} paths of length $k+1$, as is the case with the full look-ahead and the MSLA algorithms. Instead, there are $2M$ paths of length L under investigation, with the restriction that their last $N = \log_2(2M)$ symbols are different. Fig. 11 illustrates this approach.

At each iteration the M paths with the highest cost are discarded and $2M$ new paths are generated by appending either -1 or 1 to the remaining M paths. The cost associated with each path is $D_n(\mathbf{v}_i) = \sum_{j=0}^{L} \left| x_{n+j} + e_{n+j} - v_j \right|^2$. L should be sufficiently large so that all path samples at time index n are identical and their value is passed to the output. This is another significant difference between the MSLA and the M-algorithm. Typical values of the parameters are $M = 16$ and $L = 1500$. Moreover, the path updating process poses a significant overhead. Therefore the M-algorithm remains too complex for real-time signal conversion. In [20] it was proposed that the precalculated optimal output sequences for a given symbol are stored and then they are played-back during transmission to address hardware realization issues.

Assuming a typical value of $r = 8$, the reduction of complexity offered by the MSLA modulator is substantial, while its performance is comparable to that of the other implementations. The only overhead apart from the $r+1$ loop filter output calculations, is the realization of the $(r+1)$-input quantizer. A LUT approach is possible for moderate values of r, offering minimal delay at the cost of increased area. On the other hand a comparator-based approach would require less area at the cost of increased delay. The latter solution would require approximately the same resources as the path sorting algorithm needed by the other reduced complexity implementations.

D. Stability Analysis Considerations

A critical aspect of all 1-bit Σ-Δ modulators is their stability and stability limits. Because of their strongly nonlinear nature, the notion of stability relates to their desirable performance, and can accept a variety of definitions depending on the application and the mathematical tools used to analyze it. Simulations indicate that it is appropriate to treat the 1-bit Σ-Δ modulators as nonlinear dynamical systems and adopt the classical Describing-Function methodology using a quasi-linear model of the quantizer, as it was presented in [12].

Using the methodology developed in [12], the stability limits of the MSLA modulator can be analyzed, but such an analysis is beyond the scope of this manuscript. Instead, we have relied on a large number of simulations in order to illustrate the stability limits. The results are presented in the next section.

TABLE II
NOISE TRANSFER FUNCTIONS OF FIG. 12

	Transfer function
NTF 1	$\frac{1-3.99646z^{-1}+5.993z^{-2}-3.99646z^{-3}+1.000000433z^{-4}}{1-3.131z^{-1}+3.7237z^{-2}-1.99z^{-3}+0.4029z^{-4}+3.5\cdot10^{-5}z^{-5}}$
NTF 2	$\frac{(1-z^{-1})(1-1.994z^{-1}+z^{-2})}{(1-0.5995z^{-1})(1-1.384z^{-1}+0.5892z^{-2})}$
NTF 3	$\frac{(1-z^{-1})(1-2z^{-1}+z^{-2})}{(1-0.6694z^{-1})(1-1.531z^{-1}+0.6639z^{-2})}$
NTF 4	$(1-z^{-1})^3$
NTF 5	$\left(1-2\cos(2\pi\cdot0.365)z^{-1}+z^{-2}\right)^2$

IV. SIMULATION RESULTS

In the following subsections NTF is defined based on the transfer function $G(z)$ as in (2), i.e., $NTF(z) = 1/(1+G(z))$. It should be distinguished from NTF_{MSLA} given in (21).

A. The Effect of Look-Ahead Steps in Stability

Simulation of several different comparison filters and associated NTFs indicates the stability improvement of the modulator as the number of look-ahead steps k is increasing. In the following comparative simulation results, the maximum sinusoidal input amplitude resulting in stable operation is chosen as the stability measure. Manhattan distances are used for the simulations.

Two kinds of NTFs were chosen; NTFs resulting in stable conventional Σ-Δ modulators and NTFs resulting in unstable ones. The selection of stable NTFs (NTFs 1-3 in Table II) was based on design guidelines in [1], [21], [22]. The unstable NTFs (4-5 in Table II) have their zeros on the unit circle with poles at $z = 0$. Typically NTFs stable in conventional Σ-Δ modulators are also stable in MSLA ones. Moreover, as k is increased they remain stable for higher input amplitudes, while unstable NTFs in conventional Σ-Δ modulators may become stable. The main advantage of resorting to a look-ahead Σ-Δ modulator instead of a conventional one is the possibility to use more aggressive NTFs in terms of out-of-band gain and thus achieve higher in-band noise attenuation and SNDR (Signal-to-Noise and Distortion Ratio).

The attained stability simulation results are shown in Fig. 12 and the corresponding filters are shown in Table II. The MATLAB simulation uses $2\cdot10^6$ input samples. For the low-pass filters 1-4 $x_n = A\sin(2\pi\cdot0.0041482n)$ was used as the input and for the band-pass filter 5 it was $x_n = A\sin(2\pi\cdot0.365n)$. The effect of the look-ahead steps k in increasing the maximum sinusoidal input amplitude for stable operation is evident. Especially, NTFs 4 and 5, unstable when used in a conventional Σ-Δ modulator loop, i.e., $k = 0$, result in stable operation for $k \geq 1$ and $k \geq 2$ respectively.

In Fig. 13 more simulation results for NTF 5 are presented, demonstrating the impact of k and r on the SNDR (Signal-to-Noise and Distortion Ratio). Here, the input is fixed to

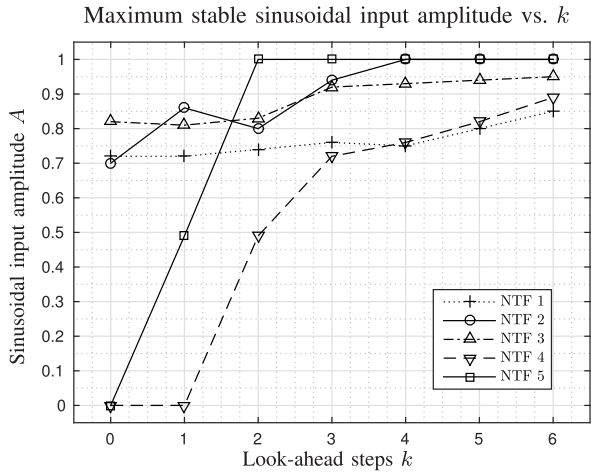

Fig. 12. Maximum stable sinusoidal input amplitude for the Manhattan distance MSLA modulator with different look-ahead steps k and NTFs (shown in Table II). Various values for r are used.

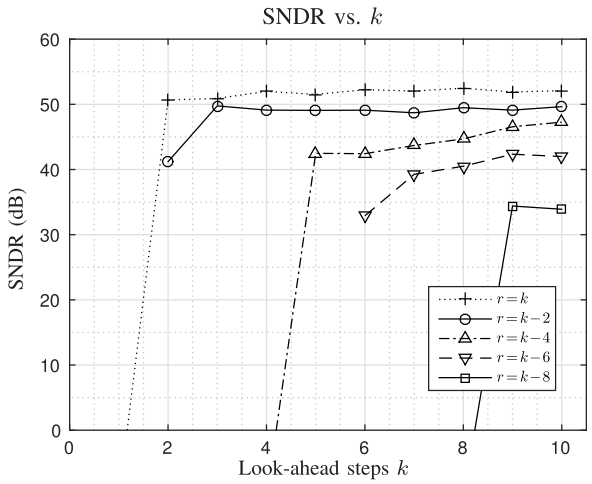

Fig. 13. SNDR vs. look-ahead steps k for NTF 5 with r as a parameter.

$x_n = 0.4\sin(2\pi \cdot 0.365n)$ and OSR $= 64$ is used for the calculation of the SNDR. The low OSR value is responsible for the relatively low SNDR values. The SNDR is in general increasing with k, while reducing the value of r from its maximum value of $r = k$ results in less hardware complexity, but with a SNDR penalty. The results are similar for other loop filter selections. For the case of $r = 0$ it should be noted that the MSLA modulator is reduced to a conventional Σ-Δ one with a modified loop filter transfer function given by (18) and (19). As it can be seen in Fig. 13, in many cases this loop filter transformation results in stable loop filter transfer functions derived from NTF 5, which is unstable when used in a conventional Σ-Δ modulator.

The performance of the MSLA modulator for NTF 2 in terms of SNDR vs. sinusoidal input amplitude A with k as a parameter and $r = k$ is depicted in Fig. 14. The input is $x_n = A\sin(2\pi \cdot 0.0041482n)$ and OSR $= 32$ is used for the calculation of the SNDR. As expected, the performance and stability are enhanced as the value of k is increased. Similar results are obtained for different comparison filters.

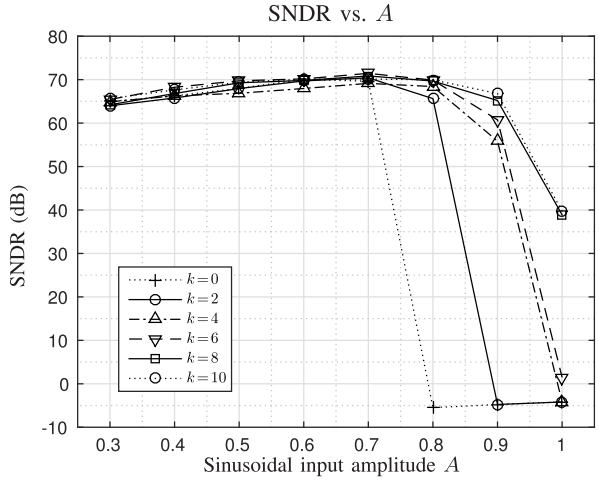

Fig. 14. SNDR vs. sinusoidal input amplitude A for NTF 2 with k as a parameter and $r = k$.

The first consideration for the selection of the NTF poles in a conventional Σ-Δ modulator is its stability. NTFs 4-5 have no poles for the reduction of the out-of-band gain and are unstable when used in a conventional Σ-Δ modulator [1]. The obtained simulation results demonstrate that such NTFs used in a MSLA modulator can offer stable operation for a wide range of input amplitudes provided that k is sufficiently large (≥ 2). Thus, the design space of the NTF is greatly increased allowing for the selection of the zeros and poles of the NTF based on other design criteria apart from stability. One such criterion is the possibility to have convenient filter coefficients such as powers of 2 (or a sum of two or three of them). This filter coefficient selection reduces multiplications and thus increases the speed and the efficiency of the MSLA modulator, leading also to less chip area compared to a MSLA modulator with a loop filter requiring a significant amount of multiplications.

In conclusion, the MSLA modulator offers higher input dynamic range than a conventional Σ-Δ modulator with the same NTF. Furthermore, a more aggressive NTF providing higher SNDR may be used. Finally, the trade-off between the performance improvement and hardware complexity may be tuned by appropriately selecting the values of k and r.

B. Manhattan vs. Euclidean Distance Comparison

As stated in previous sections, the use of Manhattan distance results in lower complexity quantizer implementations in comparison with using Euclidean distance at minimal performance and stability cost. This behavior is typical and is illustrated in Table III, where the SNDR of the MSLA modulators using Manhattan and Euclidean distances are compared. NTF 2 is chosen with various values of k, r and sinusoidal input amplitude A. The input is $x_n = A\sin(2\pi \cdot 0.0041482n)$ and OSR $= 32$.

The conclusion is that choosing Manhattan distance over Euclidean usually has a minor SNDR impact of 1-2 dB. The differences become more pronounced when the input amplitude is close to the stability limit. In this marginal

TABLE III
SNDR COMPARISON OF MANHATTAN AND EUCLIDEAN DISTANCES

k	r	A	SNDR (dB)	
			Manhattan	**Euclidean**
6	6	0.5	69.73	71.96
6	6	0.7	71.45	71.98
6	6	0.9	60.74	61.44
6	4	0.5	58.28	58.17
6	4	0.7	62.81	62.17
6	4	0.9	53.39	58.52
2	2	0.5	67.95	69.86
2	2	0.7	70.41	71.48
2	2	0.9	65.63	Unstable

case, Manhattan distance might offer increased stability as it is evident in the last row of Table III, i.e., the MSLA modulator employing Euclidean distance is unstable whereas the Manhattan distance one maintains stability.

C. Comparison With Other Look-Ahead Algorithms

The benefits of using look-ahead techniques are found mainly in their increased stability characteristics, therefore allowing for higher order loop filters, higher SNDR and increased maximum input amplitudes. Other benefits include their lower THD (total harmonic distortion) and noise modulation [19]. The observed SNDR of look-ahead modulators with *the same* comparison filter (and thus NTF) as a conventional Σ-Δ modulator is typically 1-2 dB lower than that of a conventional one for input values in the stable range of both modulators. However, this is mitigated by exploiting the increased stability of look-ahead modulators e.g. use of a higher order NTF or a NTF with a higher out-of-band gain.

In Section III-C a complexity comparison between various look-ahead implementations and the MSLA modulator was presented, showcasing the reduced relative complexity of the MSLA modulator. Here, we compare the performance of these modulators in terms of SNDR and maximum sinusoidal input amplitude A. The results are summarized in Table IV. The simulation results of the various look-ahead implementations, i.e., pruned look-ahead, efficient trellis and pruned tree (M-algorithm), are taken from [19]. In order to have a fair comparison we have used the same conditions for our simulations. A 5th (or 3rd) order feed-forward loop filter with resonators is used with the configuration SDM2 (or SDM4) as described in Appendix B of [19]. For the SNDR calculations a -6 dB 1 KHz sine wave is used as the input and $OSR = 64$ is assumed with a sampling frequency of $64 \cdot 44.1$ KHz. In all circumstances 10^6 output samples are generated. The parameters of the algorithms were chosen so that their hardware complexity is comparable. This is the reason why the number of filter output calculations (NoFC) is included in the last column of Table IV. NoFC is calculated according to Table I.

The MSLA modulator displays similar or better performance than other look-ahead algorithms for comparable complexity. More specifically, for SDM2 the MSLA modulator with $r = k = 7$ or higher outperforms the other implementations in terms of SNDR, while for SDM4 the selection of $r = k = 3$ is sufficient to give the MSLA modulator the performance advantage. A value of $r = k = 12$ is needed for the MSLA modulator in order to exhibit the same maximum stable sinusoidal amplitude as the pruned tree algorithm with $M = 4$ and only the pruned tree algorithm with $M = 8$ outperforms it, but with the cost of higher complexity.

TABLE IV
COMPARISON OF LOOK-AHEAD ALGORITHMS

Look-Ahead Algorithm	**SDM2**		**SDM4**		**NoFC**
	SNDR	**Max.** A	**SNDR**	**Max.** A	
Pruned LA ($N = 2$)	114	0.69	83	0.83	6
Pruned LA ($N = 3$)	114	0.71	83	0.85	14
Eff. trellis ($M = 32$, $N = 4$, $L = 4096$)	114	0.74	-	-	64
Pruned tree ($M = 2$, $L = 4096$)	113	0.68	-	-	4
Pruned tree ($M = 4$, $L = 4096$)	114	0.74	-	-	8
Pruned tree ($M = 8$, $L = 4096$)	114	0.78	-	-	16
MSLA ($r = k = 3$)	111	0.66	86	0.79	4
MSLA ($r = k = 5$)	113	0.70	89	0.81	6
MSLA ($r = k = 7$)	115	0.69	89	0.84	8
MSLA ($r = k = 11$)	115	0.73	90	0.89	12
MSLA ($r = k = 12$)	115	0.74	91	0.90	13

D. Output Power Spectra and Applications

In the following test cases MSLA modulators with Manhattan distance as the cost function are used for the reasons discussed in Section III-B.

1) Low-Pass Modulator With DC Input: A popular application of Σ-Δ modulators with DC input is the generation of the divider control in fractional-N frequency synthesizers. The most common structure used is the 1-1-1 MASH modulator [23]. The drawback of MASH is its multi-bit output, which complicates the design of the divider. The MSLA modulator with a simple 3rd order low-pass filter offers comparable noise shaping and stability with 1-bit output.

As a test-case the $NTF = (1 - z^{-1})^3$ is used with a DC input. An advantage of this NTF is the simplicity of its coefficients, resulting in a multiplier-less, and therefore fast and power efficient, hardware implementation. The power spectrum obtained from $2 \cdot 10^6$ output samples of the MSLA modulator with $k = 2$ and a DC input of 0.0025 is shown Fig. 15. There are some frequency spurs starting at $f = 0.0025 f_s$ as it is expected from a DC input value which is a small rational fraction, namely $1/400$. However, they can be eliminated when a small random dither is added to the input [24]. Simulation results also back this claim. The frequency and severity of these spurs depend on the DC input amplitude and on the modulator order. High-order modulators exhibit fewer or no spurs due to signal mixing in the higher order loop filter [1].

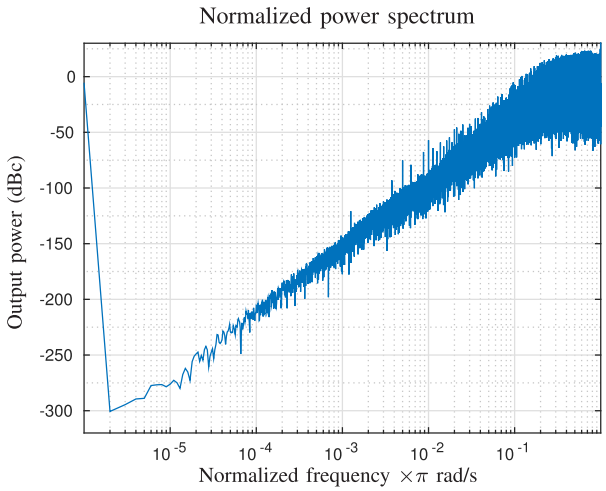

Fig. 15. Power spectrum relative to the carrier of $2 \cdot 10^6$ output samples of the low-pass MSLA modulator with $k = 2$, $NTF = (1 - z^{-1})^3$ and a DC input with amplitude 0.0025.

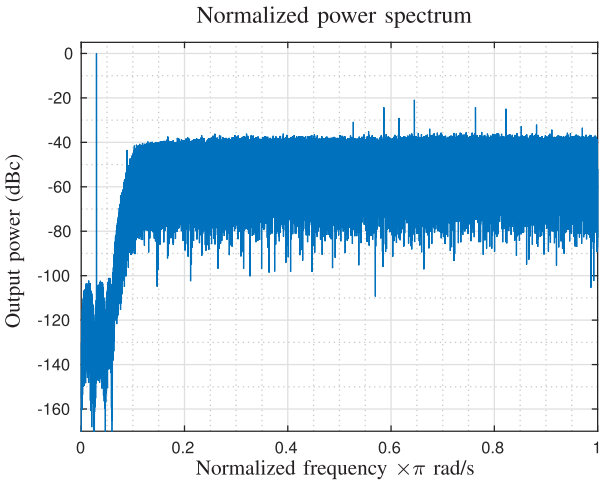

Fig. 16. Power spectrum relative to the carrier of $2 \cdot 10^6$ output samples of the wide-band low-pass MSLA modulator with $r = k = 10$ and a sinusoidal input with amplitude 0.43.

2) Low-Pass Modulator With Sinusoidal Input: The low-pass Σ-Δ modulator is used in a multitude of applications, with audio being a major one [25], [26]. A purely digital-to-digital Σ-Δ converter is used to generate the 1-bit SA-CD (Super Audio CD) bitstream from explicit PCM input data [19]. Recently, 1-bit low-pass Σ-Δ modulators have received attention in all-digital transmitter architectures [27]–[30].

A NTF with zeros spread across the signal band, for improved in-band SNR, is chosen for the demonstration of the low-pass MSLA modulator output spectrum. The NTF is synthesized using the MATLAB Delta Sigma Toolbox [31] with the following parameters: 7-th order filter, OSR = 16, use of optimized zeros and $NTF(\infty) = 2$. Lee's rule states that for a conventional 1-bit high-order Σ-Δ modulator stability is guaranteed when $NTF(\infty) < 1.5$ [1]. Indeed, MATLAB simulation indicates that this NTF is unstable when used in a conventional Σ-Δ modulator. Due to the low oversampling ratio (OSR), offering a wide fractional signal bandwidth, forcing $NTF(\infty) < 1.5$ results in low noise attenuation in the signal band. The MSLA modulator with this NTF, $r = k = 10$ and a sinusoidal input signal of amplitude 0.43 is stable. The output spectrum relative to the carrier of $2 \cdot 10^6$ output samples is shown in Fig. 16. Such a wide signal bandwidth combined with such noise attenuation is probably impossible with a conventional 1-bit Σ-Δ modulator. To back this claim, the highest possible $NTF(\infty)$ of a EF SDM with a NTF designed with the same parameters, is found to be $NTF(\infty) = 1.74$. Its SNDR is estimated at 61.5 dB, while the SNDR of the MSLA modulator with $NTF(\infty) = 2$ is 68.7 dB.

There are some out-of-band tones at frequencies higher than $0.25 f_s$, but they should be easily eliminated by a subsequent decimation filter. Simulations with various input amplitudes and frequencies, as well as different loop filters support the assertion that there are no frequency spurs in the signal band when the modulator operates far from overload.

3) Band-Pass Modulator With Sinusoidal Input: Direct digital synthesizers use an accumulator and a sinusoidal look-up table (LUT) to generate a multi-bit digital sinewave.

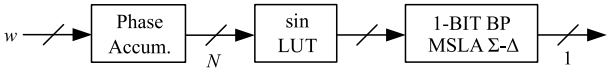

Fig. 17. All-digital frequency synthesis using the Multi-Step Look-Ahead band-pass modulator.

The frequency is determined by the frequency control word fed to the phase accumulator. Finally, the digital stream is converted to analog via a DAC. Multi-bit DAC non-linearities and low effective number of bits (ENOB) introduce numerous spurs. Several works have dealt with techniques to suppress the spurs [32]–[34].

Alternatively, one can use a band-pass Σ-Δ modulator [35] after the sinusoidal LUT for the generation of a 1-bit output with the quantization noise shaped out of the signal frequency band [36]–[41]. This is shown in Fig. 17. The NTF of this modulator should suppress the noise over a wide bandwidth to support signal generation with varying carrier frequency. MSLA modulator's bandwidth advantage is convenient. Furthermore, converting a 1-bit digital stream to analog is much less involved compared to a multi-bit one. 1-bit data conversion, apart from jitter affecting all types of DACs, is subject only to DC offset and gain errors, both harmless for the output spectrum.

In Fig. 18 the power spectrum relative to the carrier of $2 \cdot 10^6$ output samples of the band-pass MSLA modulator with $r = k = 7$ is shown. A sinusoidal input with frequency $\omega = 2\pi \cdot 0.3814$ rad/s and amplitude 0.31 was used, while the NTF was designed with the help of the MATLAB Delta Sigma Toolbox. The parameters used for the NTF were: 8-th order filter, $OSR = 16$, use of optimized zeros, $NTF(\infty) = 2$ and central frequency $\omega_0 = 2\pi \cdot 0.38$ rad/s. Again, the combination of wide signal bandwidth and in-band noise attenuation is not achievable with a conventional 1-bit Σ-Δ modulator. The EF SDM with a NTF designed using the same parameters is stable up to $NTF(\infty) = 1.69$ and achieves a SNDR of 48.7 dB. The band-pass MSLA modulator with $NTF(\infty) = 2$ exhibits a SNDR of 54.2 dB. Finally, it should be noted that there are no spurs in the whole power spectrum frequency range.

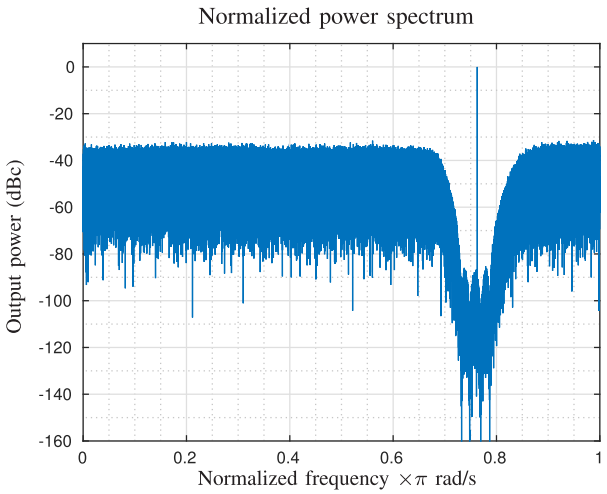

Fig. 18. Power spectrum relative to the carrier of $2 \cdot 10^6$ output samples of the band-pass MSLA modulator with $r = k = 7$ and a sinusoidal input with amplitude 0.31.

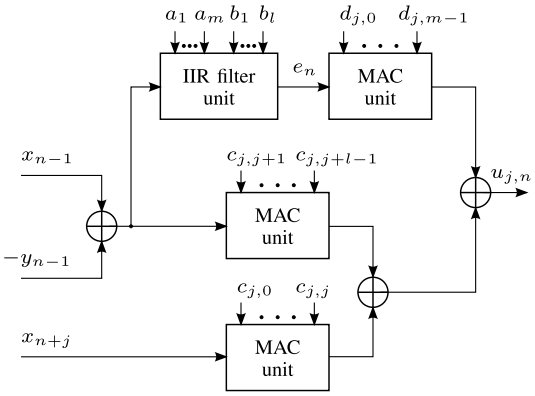

Fig. 19. The $u_{j,n}$ computation unit.

V. Hardware Implementation Aspects

The hardware implementation of the MSLA modulator is based on the evaluation of (14), while the quantizer inputs $u_{j,n}$ are given by (13). The hardware complexity depends on the look-ahead steps k, the quantizer's input vector length $r + 1$ and the comparison filter.

The proposed architecture is based on a modular design, in which the MSLA modulator consists of $r + 1$ two-input filters (L_0^j, L_1^j), which from now on we refer to as $u_{j,n}$ computation units. In comparison with the brute-force approach of calculating the total cost function for each possible output sequence, as it is common in other look-ahead Σ-Δ architectures [19], the proposed architecture requires only one calculation of vector $\mathbf{u}$ per output symbol. This fact emphasizes the importance of the analysis presented in section III.

The block diagram of a $u_{j,n}$ computation unit is shown in Fig. 19. This unit implements (13) and each multiply-and-accumulate (MAC) unit calculates each of the three sums involved. Moreover, the IIR filter unit computes e_n using the difference equation corresponding to (16). The quantizer can be implemented either with combinational logic (e.g. comparators) or with a ROM-based LUT. Its mapping function f is

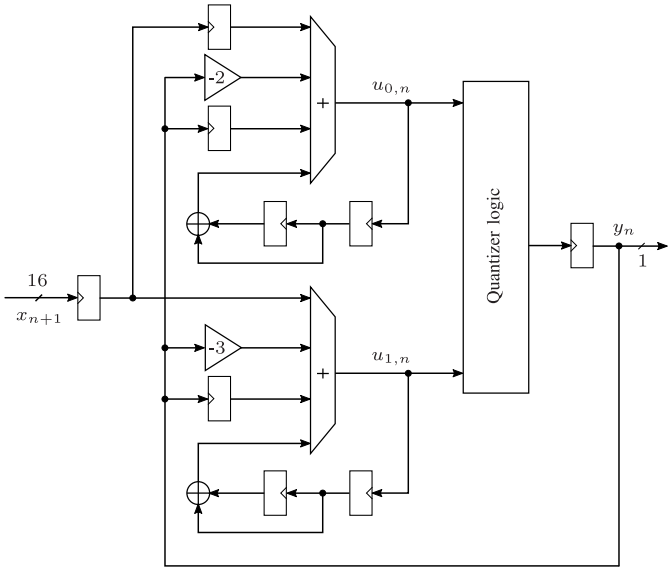

Fig. 20. The proposed hardware architecture of the MSLA modulator with $NTF = (1 - z^{-1})^2$, $k = 1$ and $r = 1$.

determined by the NTF, the number of look-ahead steps k, the value of r and the choice of Manhattan or Euclidean distance. Further research is currently performed in order to determine the best implementation for the quantizer.

The topology of the loop filter implementation has an effect on the number of registers, adders and multipliers required, as well as on the total quantization noise. The most robust topologies in terms of quantization noise are the cascade and parallel forms (second-order sections), but the transposed form II implementation is more efficient in terms of required hardware [42]. Significant hardware reduction and speed improvement are possible if the loop filter and the MAC unit coefficients are powers of 2 or a sum of powers of 2. Then, all multiplications are reduced to shift operations or two shift operations and an addition.

The cascaded integrator with feedback topology seems to be the optimal structure for a hardware implementation of the loop filter as it offers the possibility to reduce the number of bits needed after each integrator while it maintains low delay [27].

A. FPGA Implementation

As a simple test case, the hardware implementation of the MSLA modulator with $NTF = (1 - z^{-1})^2$, $k = 1$ and $r = 1$ is depicted in Fig. 20. Clock signals have been omitted for simplicity. The output register doubles as the delay element for the feedback signal. This modulator is very hardware efficient, since all multiplications reduce to shift and add operations. The bit width of the input and the registers has been set to 16 bits with 1 bit output. Further reduction of the bit widths along the signal path is possible following the design procedure in [27]. The top 4-input adder forms the $u_{0,n}$ computation unit, i.e., the two-input filter (L_0^0, L_0^1), and the bottom one the $u_{1,n}$ computation unit, i.e., the two-input filter (L_1^0, L_1^1). The transfer functions of these filters are given by (18) and (19) respectively. In our test case we find

$L_0^0(z) = 1/(1-z^{-1}+z^{-2})$, $L_0^1(z) = (-2z^{-1}+z^{-2})/(1-z^{-1}+z^{-2})$ for the top filter and $L_1^0(z) = z/(1-z^{-1}+z^{-2})$, $L_1^1(z) = (-3z^{-1}+2z^{-2})/(1-z^{-1}+z^{-2})$ for the bottom one. The quantizer logic module implements the mapping function of Fig. 10a and has two 16-bit inputs and a 1-bit output.

In order to obtain a rough estimation of hardware requirements, the modulator has been synthesized for a Xilinx Kintex-7 development board using 16-bit fixed-point representation for the modulator signals. The synthesis tool reports 7 2-input and 2 3-input 16-bit adders, 7 16-bit and 3 1-bit registers in addition to 2 2-input 16-bit multiplexers, 1 2-input 15-bit multiplexer and 1 2-input 1-bit multiplexer. That is about 1% utilization of the FPGA resources. The maximum clock frequency was reported at 330 MHz for this FPGA, but IC implementation allows for much higher clock frequencies [43].

The proposed hardware architecture is suitable for FPGA and IC CMOS implementations. The superior speed of an IC implementation is of great importance as the OSR can be increased, and thus the noise attenuation in the pass-band can be even higher. In any case, the hardware overhead of the MSLA modulator is low, which means it can be easily and cheaply incorporated in a larger mixed-signal or all-digital design. Furthermore, the 1-bit output eliminates the need for a multi-bit DAC, leading to inherently linear, all-digital designs.

VI. Conclusions

The MSLA modulator, which is a modification of the 1-bit EF SDM taking into account future input samples, has been introduced. It exhibits superior stability characteristics, allowing for higher input dynamic range and more aggressive NTFs resulting in higher SNDR than conventional 1-bit Σ-Δ modulators. Moreover, comparison of the MSLA modulator with other look-ahead algorithms highlights its performance advantage and low relative complexity, which enables real-time operation. The MSLA modulator has been analyzed mathematically and shown to be equivalent to a number of conventional Σ-Δ modulators in parallel, sharing a common multi-input 1-bit quantizer. The simulation results have illustrated the advantages of the MSLA modulator in a variety of applications. Finally, a hardware architecture has been proposed and a specific FPGA implementation has been presented, showing that moderate values of k and r do not impose a significant increase in hardware complexity when compared to a conventional 1-bit Σ-Δ modulator.

Appendix A
Notation Overview

G	Comparison filter transfer function.
b	Comparison filter numerator coefficients.
a	Comparison filter denominator coefficients.
ℓ	Comparison filter numerator order.
m	Comparison filter denominator order.
k	Number of look-ahead steps.
$r+1$	Number of partial costs involved in the calculation of the total cost.
$\{x\}$	The MSLA modulator input sequence.
$\{y\}$	The MSLA modulator output sequence.
$\{e\}$	Comparison filter G output sequence.
$\{v\}$	The trial feedback sequence.
j	The j-th look-ahead sample ($k-r \le j \le k$).
$S_{j,n}$	Partial cost associated with the j-th look-ahead sample at time instant n.
$c_{j,i}$	Coefficients associated with MSLA modulator loop filters $\left(L_j^0(z), L_j^1(z)\right)$.
$d_{j,i}$	Coefficients associated with MSLA modulator loop filters $\left(L_j^0(z), L_j^1(z)\right)$.
$u_{j,n}$	The output of the loop filter $\left(L_0^j(z), L_1^j(z)\right)$.
$\mathbf{u}$	$\left(u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n}\right)$
$\mathbf{v}$	$(v_0, v_1, \ldots, v_k)$
$D(\mathbf{v})$	The total cost function.
$f(\mathbf{u})$	The MSLA quantizer mapping function.
L_j^0	The transfer function of the MSLA modulator's j-th loop filter X input.
L_j^1	The transfer function of the MSLA modulator's j-th loop filter Y input.
NTF	The NTF of the EF SDM (Fig. 1).
STF	The STF of the EF SDM (Fig. 1).
NTF_{MSLA}	The NTF of the MSLA modulator.
STF_{MSLA}	The STF of the MSLA modulator.

Appendix B

This appendix demonstrates the derivation of (12) and (13) from (8). In the following analysis it is assumed that $\ell, m > j$. The same equations are still valid if $\ell \le j$ or $m \le j$ by setting $b_i = 0$ for $i > \ell$ and $a_i = 0$ for $i > m$ respectively.

The first step is to express every $e_{n+j}, k-r \le j \le k$ in terms of the inputs x_i, the previous outputs y_i, the previous filter G outputs $e_{n-i}, i \ge 0$ and a linear combination of $v_0, v_1, \ldots, v_{j-1}$. This is accomplished by application of the filter difference equation (9) for every $e_{n+i}, 0 < i \le j$. Using matrix notation this is written

$$\mathbf{e}_{n+1}^{n+j} = \mathbf{B}_x \mathbf{x}_{n+1-\ell}^{n+j-1} - \mathbf{B}_v \mathbf{v}_0^{j-1} - \mathbf{B}_y \mathbf{y}_{n+1-\ell}^{n-1} - \mathbf{A}\mathbf{e}_{n+1-m}^{n+j-1} \tag{28}$$

where the vector notation $\mathbf{q}_i^{i+p} = [q_{i+p}, q_{i+p-1}, \ldots, q_i]^\top$ is used, $\mathbf{v}_0^{j-1} = [v_{j-1}, v_{j-2}, \ldots, v_0]^\top$ and

$$\mathbf{B}_v = \begin{bmatrix} b_1 & b_2 & b_3 & \cdots & b_j \\ 0 & b_1 & b_2 & \cdots & b_{j-1} \\ \vdots & \ddots & \ddots & \ddots & \vdots \\ 0 & \cdots & 0 & b_1 & b_2 \\ 0 & 0 & \cdots & 0 & b_1 \end{bmatrix} \tag{29}$$

$$\mathbf{B}_y = \begin{bmatrix} b_{j+1} & b_{j+2} & \cdots & b_\ell & 0 & 0 & \cdots & 0 \\ b_j & b_{j+1} & \cdots & b_{\ell-1} & b_\ell & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ b_3 & b_4 & \cdots & b_{\ell-j+2} & b_{\ell-j+3} & \cdots & b_\ell & 0 \\ b_2 & b_3 & \cdots & b_{\ell-j+1} & b_{\ell-j+2} & \cdots & b_{\ell-1} & b_\ell \end{bmatrix} \tag{30}$$

$$\mathbf{B}_x = \begin{bmatrix} \mathbf{B}_v & \mathbf{B}_y \end{bmatrix} \tag{31}$$

with $\mathbf{B}_v$ a $j \times j$ matrix, $\mathbf{B}_y$ a $j \times (\ell-1)$ matrix and $\mathbf{B}_x$ a $j \times (j+\ell-1)$ matrix. In order to solve for e_{n+j} the last term of (28) is rewritten as

$$\mathbf{A}\mathbf{e}_{n+1-m}^{n+j-1} = \mathbf{A}_1\mathbf{e}_{n+1}^{n+j} + \mathbf{A}_2\mathbf{e}_{n+1-m}^{n} \tag{32}$$

where

$$\mathbf{A}_1 = \begin{bmatrix} 0 & a_1 & a_2 & \cdots & a_{j-2} & a_{j-1} \\ 0 & 0 & a_1 & a_2 & \cdots & a_{j-2} \\ \vdots & \vdots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & a_1 & a_2 \\ 0 & 0 & 0 & \cdots & 0 & a_1 \\ 0 & 0 & 0 & \cdots & 0 & 0 \end{bmatrix} \tag{33}$$

$$\mathbf{A}_2 = \begin{bmatrix} a_j & a_{j+1} & \cdots & a_m & 0 & 0 & \cdots & 0 \\ a_{j-1} & a_j & \cdots & a_{m-1} & a_m & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \ddots & \ddots & \vdots \\ a_2 & a_3 & \cdots & a_{m-j+2} & a_{m-j+3} & \cdots & a_m & 0 \\ a_1 & a_2 & \cdots & a_{m-j+1} & a_{m-j+2} & \cdots & a_{m-1} & a_m \end{bmatrix} \tag{34}$$

with $\mathbf{A}_1$ a $j \times j$ matrix and $\mathbf{A}_2$ a $j \times m$ matrix. Combining (28) with (32) we get

$$\mathbf{e}_{n+1}^{n+j} = (\mathbf{I}+\mathbf{A}_1)^{-1}\Big(\mathbf{B}_x\mathbf{x}_{n+1-\ell}^{n+j-1} - \mathbf{B}_v\mathbf{v}_0^{j-1} - \mathbf{B}_y\mathbf{y}_{n+1-\ell}^{n-1} - \mathbf{A}_2\mathbf{e}_{n+1-m}^{n}\Big). \tag{35}$$

Matrix $\mathbf{I}+\mathbf{A}_1$ is upper unitriangular Toeplitz [44]. Its inverse is also upper unitriangular Toeplitz, i.e.

$$\mathbf{M} \triangleq (\mathbf{I}+\mathbf{A}_1)^{-1} = \begin{bmatrix} 1 & \beta_1 & \beta_2 & \cdots & \beta_{j-2} & \beta_{j-1} \\ 0 & 1 & \beta_1 & \beta_2 & \cdots & \beta_{j-2} \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ 0 & \cdots & 0 & 1 & \beta_1 & \beta_2 \\ 0 & 0 & \cdots & 0 & 1 & \beta_1 \\ 0 & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \tag{36}$$

where $\beta_1 = -a_1$ and

$$\beta_i = -a_i - \sum_{p=1}^{i-1} a_{i-p}\beta_p \tag{37}$$

for $2 \le i \le j-1$. Therefore e_{n+j} is derived from the first row of (35) which is written as

$$e_{n+j} = \boldsymbol{\beta}_{j-1}^{0\top}\Big[\mathbf{B}_v\left(\mathbf{x}_n^{n+j-1} - \mathbf{v}_0^{j-1}\right) + \mathbf{B}_y\left(\mathbf{x}_{n+1-l}^{n-1} - \mathbf{y}_{n+1-l}^{n-1}\right) - \mathbf{A}_2\mathbf{e}_{n+1-m}^{n}\Big] \tag{38}$$

where $\boldsymbol{\beta}_{j-1}^{0\top} = [\beta_0, \beta_1 \ldots, \beta_{j-1}]$ is a row vector with $\beta_0 \equiv 1$. In (38) we used $\mathbf{B}_x = \begin{bmatrix}\mathbf{B}_v & \mathbf{B}_y\end{bmatrix}$. Performing the matrix multiplications gives

$$e_{n+j} = \sum_{i=1}^{j} c_{j,i}\left(x_{n+j-i} - v_{j-i}\right) + \sum_{i=j+1}^{j+\ell-1} c_{j,i}\left(x_{n+j-i} - y_{n+j-i}\right) + \sum_{i=0}^{m-1} d_{j,i}e_{n-i} \tag{39}$$

where coefficients $c_{j,i}, 1 \le i \le j+\ell-1$ form the elements of row vector $\boldsymbol{\beta}_{j-1}^{0\top}\mathbf{B}_x$ and coefficients $d_{j,i}, 0 \le i \le m-1$ form the elements of row vector $-\boldsymbol{\beta}_{j-1}^{0\top}\mathbf{A}_2$. Defining $\beta_i = 0$ for $i \ge j$ is convenient for writing them explicitly as

$$c_{j,i} = \begin{cases} \sum_{p=1}^{i} \beta_{i-p}b_p, & 1 \le i \le \ell \\ \sum_{p=1}^{\ell} \beta_{i-p}b_p, & \ell < i \le j+\ell-1 \end{cases} \tag{40}$$

and

$$d_{j,i} = \begin{cases} -\sum_{p=0}^{j-1} \beta_p a_{i+j-p}, & 0 \le i \le m-j \\ -\sum_{p=0}^{m-i-1} \beta_{p+i+j-m}a_{m-p}, & m-j < i \le m-1. \end{cases} \tag{41}$$

In addition, we define for all j $c_{j,0} = 1$. The substitution of e_{n+j} as given by (39) into (10) yields the equivalent expression of $S_{j,n}(v_0, v_1, \ldots, v_j)$ given in (12).

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