A Nearly All-Digital Frequency Mixer Based on Nonlinear Digital-to-Analog Conversion and Intermodulation Cancellation

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***Abstract*—We propose a nearly all-digital frequency mixer producing either the sum or difference of two frequencies provided as digital clocks. No filtering of the clock inputs is needed to suppress intermodulation products at the output. The mixer achieves high spurious-free dynamic range through optimization of an output nonlinear DAC and a multiphase intermodulation cancellation technique. A programmable logic implementation demonstrates feasibility and performance of the architecture.**

***Index Terms*—Frequency mixer, frequency synthesis, mixed-signal, nonlinear DAC, multiphase, intermodulation, spurious-free dynamic range.**

I. Introduction

FREQUENCY mixers form an important class of analog circuits used in communication and instrumentation [1]. One such application is the multiloop frequency synthesizer, such as the Diophantine frequency synthesizer [2], which combines outputs of PLLs through frequency mixers. Other uses of frequency mixers common in communications include frequency translation and frequency modulation/demodulation.

An ideal frequency mixer produces a single frequency output at either $\omega_1 - \omega_2$ or $\omega_1 + \omega_2$ when provided input frequencies of ω_1 and ω_2. However, any realizable frequency mixer will deviate from this ideality. There are two relevant conventional frequency mixers against which the proposed mixer should be compared.

1) Linear multipliers: The Gilbert multiplier [3], for example, acts as frequency mixer by multiplying two input sinusoids of frequencies ω_1 and ω_2. The resulting output will have two components, the sum frequency $\omega_1 + \omega_2$ and the difference frequency $\omega_1 - \omega_2$. The desired component is selected through filtering.
2) Analog switching mixers: These mixers use diode or transistor switching to multiply an input sinusoid at frequency ω_1 with an input square wave at frequency ω_2 [4]. The resulting output contains components at frequencies $k\omega_2 \pm \omega_1$, where k is any odd integer.

Frequency mixers of type 1 are more spectrally pure, as only two large components appear at the output if the multiplier has high linearity. However, both types of mixers require filtering at the output to select the desired component. Additionally, both require filtering at the input. This is because harmonics at the input will produce intermodulation products at the output.

Such requirements of conventional mixers are undesirable because 1) high quality filters, especially tunable filters, are costly to implement and 2) some undesired intermodulation products can be impossible to filter since they can appear close to the desired output frequency.

In this work, we show that these inherent problems of analog frequency mixers can be largely overcome by a mixed-signal alternative which uses minimal analog circuitry. The use of almost completely digital circuitry to implement frequency mixing yields the advantages of digital circuits, such as lower power, ease of design under low voltages, and design portability across technologies. Additionally, its frequency inputs are provided as digital clocks, which removes the need for input filters. The proposed frequency mixer circumvents the filtering problem by determining the frequencies of its inputs based on their rising (or falling) edges. Although the inputs to the proposed mixer are spectrally impure, the mixer achieves high spectral purity through an optimal nonlinear DAC and an intermodulation cancellation technique. These aspects of the proposed mixer allow for increased system integration and thus lowered costs.

The use of digital logic for mixing has been in use for many years. For example, [5] describes using digital gates and multivibrators to perform frequency mixing of input square waves. Digital logic such as XOR gates have long been used in place of analog multipliers as PLL phase detectors. Such approaches, however, have been hampered by the lack of spectral purity in the outputs of digital circuits. We will show that spectral purity can be greatly improved using a nonlinear DAC in conjunction with digital logic.

Use of nonlinear DACs for sinusoidal synthesis has previously been studied in many works [6]–[10]. However, our proposed nonlinear DAC is fundamentally different from those of past works in that it has low resolution (typically 7 quantization levels) but synthesizes these amplitudes with very high accuracy with a small number of analog components (typically 8 small-ratio resistors in a voltage-mode implementation). As we will show, high spectral purity can be attained even with low resolution, provided that accuracy is high. Use of a low-resolution, high-accuracy nonlinear DAC was proposed in [11], but the circuit architecture and harmonic distortion of such a DAC was not provided.

The intermodulation cancellation technique of the proposed mixer is based on multiphasing, a concept introduced in [12] for up-and-down-conversion in radio transceivers and further expanded in [13] and [14]. Past works [14]–[16] have presented the proposed mixer architechture without the details of its spectral properties or the design of the DAC.

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II. Periodic Piecewise-Constant Functions

A. Spectral Properties

While the inputs to the proposed mixer are digital clocks, the mixer's output is neither a square wave, nor a product of square waves. Instead it is the product of periodic signals of the form

$$a(t) = p_i \quad \text{for all } t \in \left[i\frac{T}{N}, (i+1)\frac{T}{N} \right) \text{ and integers } i$$

where sequence $\{p_i\}$ is periodic with period N (divisions) and continuous-time signal $a(t)$ is periodic with period T. We refer to such a signal $a(t)$ as being periodic piece-wise constant (PPWC) and we use it to approximate the ideal sinewave.

In such an approximation, it is desirable that low-order harmonics are zero or minimal resulting in high spurious free dynamic range in a frequency interval extending as much as possible beyond the fundamental.

We now state certain facts about PPWC signals, with derivations provided in the Appendix.

Proposition 1: Consider the class of PPWC signals with N divisions and fundamental frequency ω. Let $a(t)$ be one of them with the fewest possible frequency harmonics $j = 0, 1, \ldots, N$ of nonzero amplitude. Then the levels, p_i, of $a(t)$ are given by the sampling of a sinusoid for any $\theta \in [0, 2\pi/N)$

$$p_i = \cos\left(\frac{2\pi i}{N} + \theta \right). \tag{1}$$

Moreover, $a(t)$ has harmonics precisely at frequencies $(rN + 1)\omega$ and $(rN - 1)\omega$, for all integers r.

For the remainder of this work, we assume PPWC signals of this form (1). The proposed frequency mixer generates the product of two such PPWC signals, which is converted to analog form with an optimized nonlinear DAC.

Note that a PPWC signal with levels of the form (1) and even number of divisions, N, has the property

$$p_i = -p_{N/2+i}. \tag{2}$$

Therefore, the product of two such signals also takes values that occur in oppositely signed pairs.

Note that when considering the multiplication of two PPWC signals, it is not, in general, convenient (or meaningful) to treat them as discrete-time signals because each has a different sampling period. Suppose the two PPWC signals to be multiplied are $a(t)$ and $b(t)$, with respective periods T_1 and T_2, both having N intervals of constant amplitude. If we represent $a(t)$ and $b(t)$ with discrete sequences $a[n]$ and $b[n]$ respectively, then their sampling periods are T_1/N are T_2/N, respectively, making $a[n]b[n]$ unrelated to $a(t)b(t)$ in general.

B. Generating PPWC Signals With Digital Circuits

Although the proposed mixer's output is an analog product of two PPWC signals $a(t)$ and $b(t)$, the mixer does not internally generate the analog signals $a(t)$ and $b(t)$. Instead, it produces only digital representations of $a(t)$ and $b(t)$.

As an illustrative example, consider a PPWC function $a(t)$ with $N = 4$ divisions per period T. Let the fundamental frequency of $a(t)$ be $\omega = 2\pi/T$ and let the four levels of $a(t)$ be p_0, p_1, p_2, and p_3.

Fig. 1 shows two circular shift registers. At the active clock edge, bits shift from left to right, except for the right-most element, which shifts its data to the left-most element in the ring.

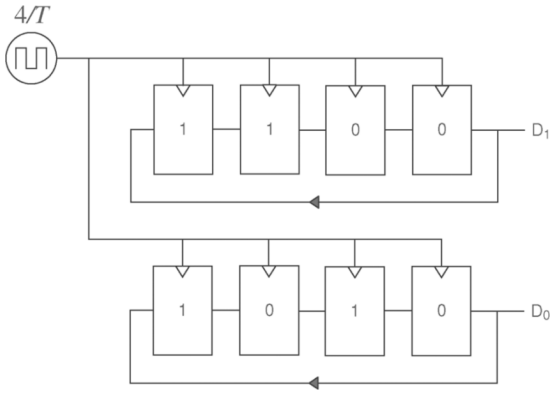

Fig. 1. Generating $a(t)$ with circular shift registers for $N = 4$. Both shift registers rotate their data at the active edge of the same clock.

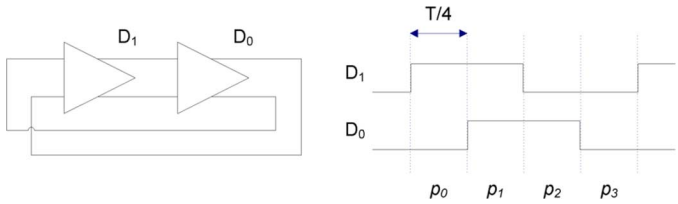

Fig. 2. Digital representation of $a(t)$ can be generated using a 2-stage ring oscillator with frequency equal to the fundamental frequency of $a(t)$.

Both shift registers are clocked at frequency $4/T$ Hz or alternatively angular frequency 4ω rad/s.

The contents of the shift registers are initialized to hold a desired pattern. In this particular example, the pair of shift registers acts as a 2-bit counter. Let the binary number 00 represent p_0, 01 represent p_1, 10 represent p_2, and 11 represent p_3. Then the pattern outputted by the shift register pair has fundamental frequency ω and represents signal $a(t)$.

The sequence of amplitudes p_0, p_1, p_2, p_3 were encoded using a direct binary code 00, 01, 10, 11. However, we prefer to permute the codes to form a Gray code sequence: 00, 01, 11, 10 and have only one bit change between subsequent codes.

Note that this circuit generates three additional phase-shifted versions of $a(t)$ if we tap the other outputs: $a(t + T/4)$, $a(t + 2T/4)$, and $a(t + 3T/4)$. The use of these additional phases is discussed later. We will refer to this pair of shift registers as the phase generation circuit. In general, it can consist of S shift registers, each N bits long, to form an S-bit representation of $a(t)$.

One may notice that the above approach requires an input frequency to the shift registers which is N times the fundamental frequency of $a(t)$. However, an alternative approach allows for generating $a(t)$ using an input clock of the same frequency as the fundamental frequency of $a(t)$.

This is done using the phases of a ring oscillator, as depicted in Fig. 2 for the case $N = 4$. By taking two phases of the ring oscillator's output, one can form a Gray-coded binary sequence with a period of $N = 4$. In many cases a ring oscillator is already present at the sources of the two frequency clocks. Alternatively, one can phaselock it to an input of the same fundamental frequency as $a(t)$.

Additionally, by also using complementary outputs, $\bar{D}_0$ and $\bar{D}_1$, one can produce all N phases of $a(t)$, as shown in Fig. 3.

For simplicity of presentation, in the remainder of the paper, we assume that the digital representation of $a(t)$ is generated using shift registers clocked with frequency of N/T Hz.

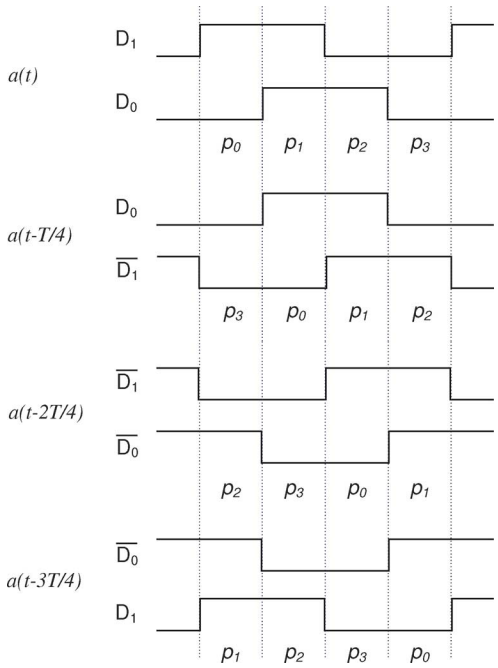

Fig. 3. By using all output phases of the ring oscillator, one can generate all N phase shifts of $a(t)$.

III. Generating the Product of PPWC Signals

Consider two PPWC signals $a(t)$ and $b(t)$ which are time-scaled versions of each other

$$b(t) = a(\lambda t),$$

where λ is a positive real number. Although it is not necessary to restrict $a(t)$ and $b(t)$ to be time-scaled versions of each other, it simplifies the discussion and design of the mixer. Let $a(t)$ have period T_1 and fundamental frequency ω_1 and let $b(t)$ have period T_2 and fundamental frequency ω_2.

Consider the digital representations of $a(t)$ and $b(t)$ produced by the circular shift registers discussed previously. Our mixer computes a digital representation of the product $a(t)b(t)$ and converts it in an analog value.

Suppose the product $a(t)b(t)$ assumes r distinct values. As is discussed later, our DAC produces only nonnegative values, so we add a constant offset to these r product values to form nonnegative values $C_1 < C_2 < \cdots < C_r$, with $C_1 = 0$ and $C_r = 2(p_{\max})^2$, where $p_{\max}$ is the maximum of both signals $a(t)$ and $b(t)$. Typically, r is a small number, thus, given the digital code representations of $a(t)$ and $b(t)$, a digital representation of their product $a(t)b(t)$ can be computed using a small look-up table (LUT).

A. LUT Multiplier

Consider the LUT-based multiplier shown in Fig. 4 for the case where $N = 4$. Shift register A_1 is a 4-bit shift register connected in a ring as in the earlier example of the phase generation circuit. As before, it holds a 4-bit sequence which rotates at the active edge of a clock of angular frequency $4\omega_1$ rad/s. Q_0 through Q_3 are the four outputs of this shift register.

Shift register A_2 operates similarly to A_1 except that it holds a different 4-bit pattern. Thus A_1 and A_2 form a shift register pair that can generate a digital representation of any PPWC signal $a(t)$ with $N = 4$ and fundamental frequency ω_1. We will arbitrarily pick the Q_1 outputs of registers A_1 and A_2 to form a 2-bit representation of $a(t)$, although any other pair of outputs would be equally suitable. Shift registers B_1 and B_2 are constructed similarly to produce the digital representation of PPWC signal $b(t)$ of fundamental frequency ω_2. Again, we have arbitrarily chosen the Q_1 outputs to represent $b(t)$. Together, the Q_1 outputs of the four shift registers form the 4-bit address input into an LUT. This 4-bit input into the LUT determines the current values of $a(t)$ and $b(t)$ and thus the product $a(t)b(t)$. The output of the LUT is thus a digital code for $a(t)b(t)$. This digital code will be the input to a nonlinear DAC to produce the desired analog value $a(t)b(t)$.

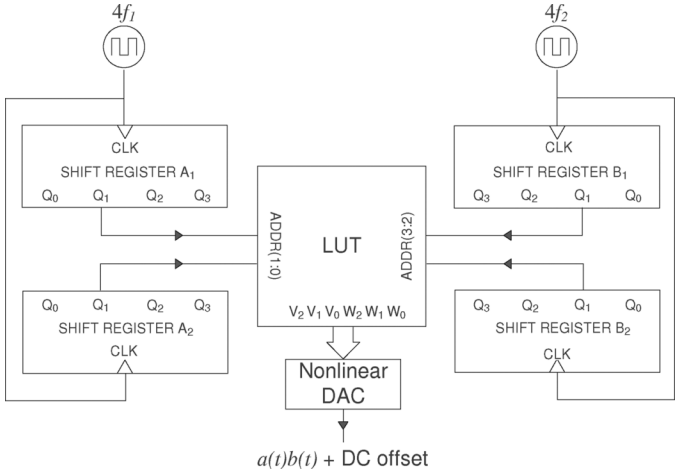

Fig. 4. Multiplying $a(t)$ and $b(t)$ with an LUT. Shift registers produce digital representations of $a(t)$ and $b(t)$ which are inputs to the LUT. The LUT computes the product $a(t)b(t)$ and sends the corresponding digital code to the nonlinear DAC. The DAC, being unipolar, exhibits a dc offset.

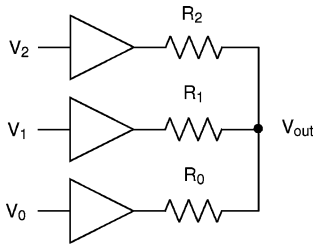

Fig. 5. Nonlinear DAC using a resistor network. V_2, V_1, V_0 form the digital code to be converted by the DAC.

Note that the output of the LUT can change at every active edge of the two clocks. If $f_1/f_2 = \rho_2/\rho_1$ for integers ρ_1, ρ_2 then the output can be considered as a synchronous one clocked at frequency $4\rho_1 f_1/\gcd(\rho_1, \rho_2)$. If f_1/f_2 is an irrational number then the output is asynchronous.

B. Digital-to-Analog Conversion of LUT Output Codes

Since the possible number of products is small, the analog product $a(t)b(t)$ is more efficiently produced with a nonlinear DAC. Fig. 5, shows a basic example of a 3-bit nonlinear DAC. The signals V_i are the outputs of logic gates, which are consider to be 0 or 1 V. The DAC output is

$$V_{\text{out}} = K\left(\frac{V_2}{R_2} + \frac{V_1}{R_1} + \frac{V_0}{R_0}\right),$$

where K is a constant.

For reasons to be discussed, it is desirable for the DAC to produce outputs which occur in oppositely signed pairs (ignoring the dc offset). That is, if the DAC can produce an output of A, then it should be able to produce an output of $-A$. This is

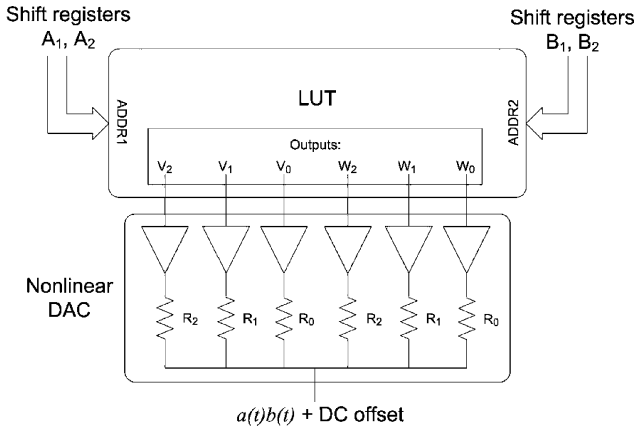

Fig. 6. Nonlinear DAC consisting of buffers driving a resistor network. $V_2V_1V_0W_2W_1W_0$ is the digital code to be converted by the DAC.

achieved when the amplitudes of the PPWC signals occur in oppositely signed pairs. This can be satisfied by choosing the number of divisions, N, to be even, since this results in amplitudes $p_i = -p_{i+N/2}$. From here on we assume that this is always the case.

Consider the DAC of Fig. 6. This DAC consists of the output drivers of the LUT and a resistor network. The values of the signals V_i and W_j are 0 or 1 V. Note that this DAC uses two identical sets of resistors. Since this DAC can only produce positive outputs, the resulting analog representation of $a(t)b(t)$ will have a dc offset. DAC's output is given by

$$v_{\text{out}} = K\sum_{i=0}^{2}\frac{V_i}{R_i} + K\sum_{i=0}^{2}\frac{W_i}{R_i}$$

where

$$K = \left(\frac{2}{R_2} + \frac{2}{R_1} + \frac{2}{R_0}\right)^{-1}.$$

We construct the DAC so that the most negative product corresponds to analog output of 0 V produced with LUT output $V_2V_1V_0W_2W_1W_0 = 000000$. The maximum value of the product corresponds to $V_2V_1V_0W_2W_1W_0 = 111111$. These choices are arbitrary but allow us to make use of the full output swing of the circuit. Finally, the zero product $a(t)b(t) = 0$ corresponds to $V_2V_1V_0W_2W_1W_0 = 000111$ and analog output

$$K\left(\frac{1}{R_2} + \frac{1}{R_1} + \frac{1}{R_0}\right). \tag{3}$$

Thus, (3) is DAC's dc offset.

The DAC can produce any output of the form

$$K\sum_{i=0}^{2}\frac{\sigma_i}{R_i} + K\sum_{i=0}^{2}\frac{1}{R_i} \tag{4}$$

where $\sigma_i \in \{-1, 0, 1\}$, simply by setting $V_i = W_i = 0$ when $\sigma_i = -1$, $V_i = 0, W_i = 1$ when $\sigma_i = 0$ and $V_i = W_i = 1$ when $\sigma_i = 1$.

In general, a similar DAC with two identical sets of B resistors produces the 3^B output values of the form

$$K\sum_{i=0}^{B-1}\frac{\sigma_i}{R_i} + K\sum_{i=0}^{B-1}\frac{1}{R_i}. \tag{5}$$

Note that these 3^B values are not necessarily distinct, depending on the choice of the R_is.

Neglecting the dc offset, we see that this DAC structure produces values which occur in oppositely signed pairs, regardless of the choice of the resistors.

C. Spectral Properties of the LUT-Based Mixer

Although the spectrum of the LUT-based mixer can be well approximated by the spectrum of $a(t)b(t)$, an important result can be obtained by examining the exact output of the mixer, since the mixer generates an approximation of the product $a(t)b(t)$, with an accuracy determined by the nonlinear DAC:

Theorem 1: Consider a mixer in which resistors are pairwise identical. That is, resistances which are intended to be identical are indeed exactly identical. Then regardless of the values of the resistances, the mixer eliminates all intermodulation products of the form

$$k\omega_1 \pm m\omega_2, k \text{ or } m \text{ even}. \tag{6}$$

To prove this, we use the following result from [17]:

Proposition 2: A function $f(t)$ with period T has no even harmonics if and only if $f(t) = -f(t - T/2)$.

As before, we assume that $a(t)$ and $b(t)$ have respective periods T_1 and T_2 and that their periods are divided into N equal-length intervals on which the function is constant. In this section, $a(t)$ and $b(t)$ will be the digital inputs into the LUT, but the DAC output will not be exactly $a(t)b(t)$. However, we will assume that the DAC can produce outputs that occur in oppositely signed pairs. Achieving this does *not* require all resistors to be simultaneously matched. Instead we only need to assume that the resistors are pairwise matched: it is not necessary that the actual resistance ratios are equal to the designed values; we only need the pairs of resistors that are supposed to be matched to be equal. In this section we assume this to be true, so that the DAC outputs occur in oppositely signed pairs, although the amplitudes can have errors.

Define the ith interval as $[iT_2/N, (i+1)T_2/N)$. Let the LUT input $b(t)$ be constant on this interval and that its value be $b_{i \bmod N}$.

Normally, the inputs of the LUT are $a(t)$ and $b(t)$. However, let us momentarily make the inputs instead be $a(t)$ and b_i, $i \in \{0, 1, \ldots, N-1\}$, for all time t. Define the corresponding output of the DAC as $x_i(t)$. If the values of the resistors of the DAC are known, then $x_i(t)$ is known as well.

Now restore the inputs to the LUT back to the original signals $a(t)$ and $b(t)$. Consider the $(i + rN)$th interval, for $i \in \{0, 1, \ldots, N-1\}$ and any integer r. On this interval, the inputs to the LUT are $a(t)$ and b_i. On this interval, the output of the DAC is thus

$$y(t) = x_i(t). \tag{7}$$

Let us now define a periodic function $s(t)$ with period T_2

$$s(t) = \begin{cases} 1, & \text{if } t \in [0, T_2/N) \\ 0, & \text{if } t \in [T_2/N, T_2). \end{cases}$$

Equation (7) can then be rewritten as $y(t) = x_i(t)s(t - iT_2/N)$. On the $(i + rN)$th interval, for $i \in \{0, 1, \ldots, N-1\}$, $x_j(t)s(t - jT_2/N) = 0$ for any $j \neq i$, $j \in \{0, 1, \ldots, N-1\}$. Thus, the output of the DAC on this interval can be rewritten as

$$y(t) = \sum_{i=0}^{N-1} x_i(t)s(t - iT_2/N). \tag{8}$$

Since any interval can be expressed as the $(i+rN)$th interval, the output of the DAC for all times t is given by (8).

Recall from (2) that the PPWC signal satisfies

$$b_i = -b_{i+N/2} \tag{9}$$

for all i. Suppose momentarily that the inputs to the LUT are $a(t)$ and $-b_{(i+N/2) \bmod N}$ for all times t. Then the DAC output is $-x_{(i+N/2) \bmod N}(t)$. However, we also know that $-b_{(i+N/2) \bmod N} = b_{i \bmod N}$ because of (9). Thus, the output of the DAC can also be expressed as $x_{i \bmod N}(t)$. We thus arrive at the conclusion that

$$x_{i \bmod N}(t) = -x_{(i+N/2) \bmod N}(t). \tag{10}$$

Let us now restore the inputs of the LUT to $a(t)$ and $b(t)$ and rewrite the DAC output as

$$\begin{aligned} y(t) &= \sum_{i=0}^{N-1} x_i(t) s\left(t - i\frac{T_2}{N}\right) \\ &= \sum_{i=0}^{N/2-1} x_i(t) s\left(t - i\frac{T_2}{N}\right) \\ &\quad + \sum_{i=0}^{N/2-1} x_{i+N/2}(t) s\left(t - \left(i + \frac{N}{2}\right)\frac{T_2}{N}\right) \\ &= \sum_{i=0}^{N/2-1} x_i(t) s\left(t - i\frac{T_2}{N}\right) \\ &\quad - \sum_{i=0}^{N/2-1} x_i(t) s\left(t - i\frac{T_2}{N} - \frac{T_2}{2}\right) \\ &= \sum_{i=0}^{N/2-1} x_i(t) \left[s\left(t - i\frac{T_2}{N}\right) - s\left(t - i\frac{T_2}{N} - \frac{T_2}{2}\right)\right]. \end{aligned} \tag{11}$$

Let

$$g_i(t) = s\left(t - i\frac{T_2}{N}\right) - s\left(t - i\frac{T_2}{N} - \frac{T_2}{2}\right).$$

It can be seen that $g_i(t)$ has period T_2 and that $g_i(t - T_2/2) = -g_i(t)$ for all i. Thus, by Prop. 2, $g_i(t)$ does not have even harmonics. Additionally, $x_i(t)$ has no even harmonics because the DAC produces outputs in oppositely signed pairs. Thus, (11) involves the sum of products of functions which do not possess even harmonics. This means that the mixer eliminates all intermodulation products of the form

$$k\omega_1 \pm m\omega_2, k \text{ or } m \text{ even}, \tag{12}$$

which proves the claim.

From an implementation standpoint, this property makes the mixer less sensitive to mismatch errors since elimination of intermodulation products of the form of (12) only requires paired resistors to be matched rather than all resistors simultaneously matched. For example, suppose resistors R_1 and R_2 are a pair which should be identical and resistors R_3 and R_4 are another pair which should be identical. Then if R_1 and R_2 are scaled by a constant and then R_3 and R_4 are scaled by a different constant, the above intermodulation products still remain cancelled.

IV. Nonlinear DAC Optimization

As shown previously, one can use simple circuit components to generate products of PPWC signals. However, in constructing the DAC, there are many degrees of freedom. The ideal product $a(t)b(t)$ has a known set of intermodulation products. However, the DAC can only produce an approximation of $a(t)b(t)$, and this approximation will have a slightly different spectrum, with the degree of difference depending on the design of the DAC.

Since the spectrum of the DAC's output is a complicated function of its resistor values and input codes, our approach to finding the optimal DAC is to find the DAC that closely approximates the amplitudes of $a(t)b(t)$ in the time domain. By the Parseval relation, the total energy in the error component is the same in both the time and frequency domains, and thus producing an accurate time-domain approximation will bound errors in the frequency domain.

We now present our optimization algorithm for constructing the DAC. For simplicity, we will continue to require that the signals $a(t)$ and $b(t)$ are time-scaled versions of each other.

In a monolithic design, the resistors are typically integer multiples of a reference resistance value for matching purposes, and the sum of these integer multiples must be bounded because of area constraints.

Recall that the DAC is constructed from two sets of B resistors $R_0, \ldots, R_{B-1}$. Let $R_n = \mu_n R$ where μ_n is an integer and R is the reference resistance. Then the area constraint is

$$\sum_{n=0}^{B-1} \mu_n \le M_T \tag{13}$$

where M_T is a constant chosen by the designer based on available chip area. The constant B is also be chosen by the designer based on available area since B determines the LUT output width and the number of voltage buffers.

Suppose for the moment that we have chosen a particular value for phase shift θ in (1). Let $c = (c_1, \ldots, c_r)$ be the vector of all positive values of the product $a(t)b(t)$ with $c_{\max} = \max(c_i)$.

Recall that $a(t)b(t)$ takes values in oppositely signed pairs and that the DAC produces values which occur in oppositely signed pairs (neglecting the dc offset), according to (5). Note that the DAC can always produce an output of 0.

For each ideal product value c_i, let $\hat{c}_i$ be the corresponding DAC output (without dc offset) which approximates c_i

$$\hat{c}_i = \alpha \sum_{n=0}^{B-1} \frac{\sigma_{i,n}}{\mu_n}, \quad \sigma_{i,n} \in \{-1, 0, 1\} \tag{14}$$

where α is an arbitrary constant. Note that vector $\hat{c} = (\hat{c}_1, \ldots, \hat{c}_r)$ does not necessarily have the same Euclidean length $\|\hat{c}\|_2$ as c. To determine the accuracy of the approximation we compare the normalized versions of $\hat{c}$ and c, i.e.,

$$u = c/\|c\|_2, \quad \hat{u} = \hat{c}/\|\hat{c}\|_2.$$

Thus, given vector c (or equivalently, the phase difference θ at $t = 0$), our optimization problem is

$$\begin{gathered} \min \|u - \hat{u}\|_2 \\ \text{subject to} \\ \textstyle\sum_{n=0}^{B-1} \mu_n \le M_T, \quad \mu_n \in \mathbb{N} \end{gathered} \tag{15}$$

where $\mathbb{N}$ is the set of positive integers.

Combinatorial optimization problem (15) is hard. However, approximate solutions can be derived via the following proposed method consisting of a sequence of iterations in each of which we evaluate a feasible vector $(\mu_n)_{n=0}^{B-1} = (\mu_0, \ldots, \mu_{B-1})$ for constructing approximation vector $\hat{c}$. When M_T is reasonably small, it is computationally practical to examine every possible vector $(\mu_n)_{n=0}^{B-1}$.

Now let us consider a single iteration of the resistor optimization algorithm. Starting with a set of resistor ratios vector $(\mu_n)_{n=0}^{B-1}$ satisfying (13) we construct set γ as follows.

For every vector $(\mu_n)_{n=0}^{B-1}$, the DAC can synthesize at most 3^B distinct outputs, of which we use only a subset. First, we define set γ as follows. Consider the total set of 3^B possible values that can be synthesized with the resistor ratios μ_n, ignoring the dc offset, i.e.,

$$\sum_{n=0}^{B-1} \frac{\sigma_{i,n}}{\mu_n}, \quad \sigma_{i,n} \in \{-1, 0, 1\}$$

for $i = 1, \ldots, 3^B$. Divide the elements of this set by the largest one, resulting in a normalized set with largest element 1 and smallest element -1. We form set γ by keeping the nonnegative elements of this set. Recall that we are currently only interested in the positive outputs, since negative outputs are the exact negative of the positive ones.

We then construct the DAC output vector $\hat{c}$ by choosing each $\hat{c}_i$ as an element from the normalized set γ. Thus $\hat{c}$ will be a vector of numbers between 0 and 1. Recall that the DAC maps the most positive product to its maximum possible output voltage. Thus, we require that $\max \hat{c}_i = 1$. The choice of the remaining $\hat{c}_i$ is made as follows.

To compare the ideal products c with the approximation $\hat{c}$, we normalize values $c_i/c_{\max}$, since

$$0 < \frac{c_i}{c_{\max}} \leq 1.$$

Then for each c_i, we choose $\hat{c}_i$ from set γ that is closest to $c_i/c_{\max}$, i.e.,

$$\hat{c}_i = \underset{x \in \gamma}{\operatorname{argmin}} |x - c_i/c_{\max}|, \quad \text{for all } i$$

Then we compute the value of the cost function $||u - \hat{u}||_2$.

The above step is reiterated for all feasible vectors $(\mu_n)_{n=0}^{B-1}$. Thus, for a given vector c, the best approximation $\hat{c}$ is found through

$$\begin{gathered} \min ||u - \hat{u}||_2 \\ \text{subject to} \\ \textstyle\sum_{n=0}^{B-1} \mu_n \leq M_T, \quad \mu_n \in \mathbb{N}, \\ \hat{c}_i = \operatorname{argmin}_{x \in \gamma} |x - c_i/c_{\max}|, \quad \text{for all } i. \end{gathered} \tag{16}$$

Among all values of vector $\hat{c}$ derived, one of them leading to minimum $||u - \hat{u}||_2$ is stored and the whole process is repeated for a different vector c resulting from a new value of $\theta \in [0, 2\pi/N)$. Since θ is a continuous variable, we change θ by incrementing it by a predetermined step size.

When all values of θ have been examined, we keep the $c, \hat{c}$ pair that yields the minimum error $||u - \hat{u}||_2$. Thus, the complete optimization problem is

$$\begin{gathered} \min ||u - \hat{u}||_2 \\ \text{subject to} \\ \theta \in [0, 2\pi/N), \\ \textstyle\sum_{n=0}^{B-1} \mu_n \leq M_T, \quad \mu_n \in \mathbb{N}, \\ \hat{c}_i = \operatorname{argmin}_{x \in \gamma} |x - c_i/c_{\max}|, \quad \text{for all } i. \end{gathered} \tag{17}$$

As it is seen later, solutions to this problem can yield a very high accuracy DAC using only small resistor ratios.

While the exhaustive evaluation of all combinations of resistor ratios satisfying (13) may seem computationally intensive, the search is typically short due to the small values for M_T prefered in designing the DAC to minimize component spread.

V. Intermodulation Product Cancellation by Multiphase Mixing

Now that we have covered the basic concepts behind PPWC multiplication, we present a method to reduce the intermodulation products content.

A. Basics of Multiphase IMD Product Cancellation

We first consider the case in which the mixer is intended to produce the difference frequency $\omega_1 - \omega_2$ of two signal $a(t)$ and $b(t)$ with fundamental frequencies $\omega_1 = 2\pi/T_1$ and $\omega_2 = 2\pi/T_2$ respectively. The signals are assumed to have no dc value and so they can be expressed as

$$\begin{aligned} a(t) &= \sum_{k=1}^{\infty} A_k \cos(k\omega_1 t + \theta_k) \\ b(t) &= \sum_{m=1}^{\infty} B_m \cos(m\omega_2 t + \phi_m). \end{aligned}$$

Now consider their phase-shifted versions

$$\begin{aligned} a\left(t + \frac{nT_1}{P}\right) &= \sum_{k=1}^{\infty} A_k \cos\left(k\omega_1 t + \theta_k + \frac{2\pi kn}{P}\right) \\ b\left(t + \frac{nT_2}{P}\right) &= \sum_{m=1}^{\infty} B_m \cos\left(m\omega_2 t + \phi_m + \frac{2\pi mn}{P}\right) \end{aligned}$$

where n and P are integers. The sum of products of phase-shifted pairs is

$$\begin{aligned} &y_{\omega_1 - \omega_2}(t) \\ &= \sum_{n=0}^{P-1} a\left(t + \frac{nT_1}{P}\right) b\left(t + \frac{nT_2}{P}\right) \\ &= \sum_{n=0}^{P-1} \sum_{k=1}^{\infty} \sum_{m=1}^{\infty} A_k \cos\left(k\omega_1 t + \theta_k + \frac{2\pi kn}{P}\right) \\ &\quad \times B_m \cos\left(m\omega_2 t + \phi_m + \frac{2\pi mn}{P}\right) \\ &= \sum_{k=1}^{\infty} \sum_{m=1}^{\infty} \sum_{n=0}^{P-1} \frac{A_k B_m}{2} \\ &\quad \times \left[\cos\left((k\omega_1 + m\omega_2)t + \theta_k + \phi_m + \frac{2\pi(k+m)n}{P}\right)\right. \\ &\quad \left. + \cos\left((k\omega_1 - m\omega_2)t + \theta_k - \phi_m + \frac{2\pi(k-m)n}{P}\right)\right]. \end{aligned} \tag{18}$$

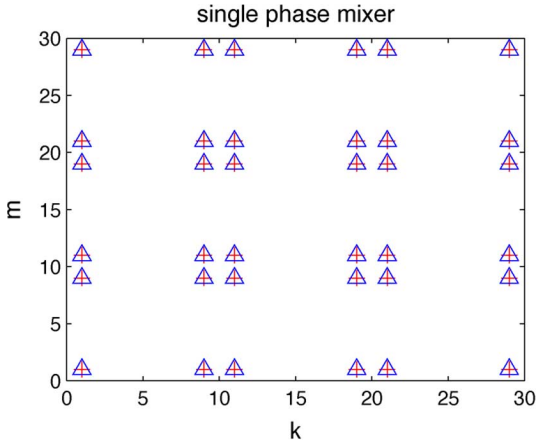

Fig. 7. Intermodulation product locations of a single phase mixer. A Δ at coordinates (k, m) in the plot indicates the presence of an intermodulation product $k\omega_1 - m\omega_2$ at the mixer's output. A $+$ at coordinates (k, m) in the plot indicates the presence of an intermodulation product $k\omega_1 + m\omega_2$. Note that in this plot the Δ and $+$ locations are overlapping.

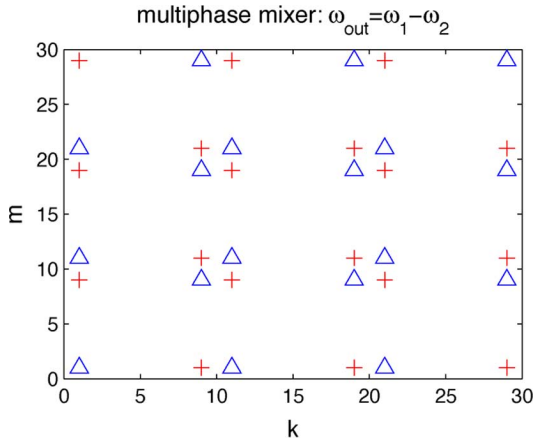

Fig. 8. Intermodulation product locations of a 5-phase mixer with output $\omega_1 - \omega_2$. Note that the 5-phase mixer canceled half the intermodulation products produced by the single phase mixer of Fig. 7.

We rewrite this expression by using the following identity:[1]

$$\sum_{n=0}^{P-1} \cos\left(x + \frac{2\pi rn}{P}\right) = P\cos(x)\delta[r \bmod P], \qquad (19)$$

where r is any integer and

$$\delta[n] = \begin{cases} 1, & \text{if } n = 0 \\ 0, & \text{otherwise.} \end{cases}$$

Using this identity, (18) is rewritten as

$$\begin{aligned} &y_{\omega_1-\omega_2}(t) \\ &\quad = \sum_{k=1}^{\infty}\sum_{m=1}^{\infty} \frac{PA_kB_m}{2} \\ &\qquad \times \{\cos((k\omega_1 + m\omega_2)t + \theta_k + \phi_m)\delta[(k+m) \bmod P] \\ &\qquad + \cos((k\omega_1 - m\omega_2)t + \theta_k - \phi_m)\delta[(k-m) \bmod P]\} \end{aligned} \qquad (20)$$

which is the output of the multiphase mixer for P phases. It can be compared to the original single phase mixer by letting $P = 1$. In this case the delta terms have no effect.

However, for $P > 2$, many of the terms are eliminated because the delta term become 0.

This result is depicted graphically in the plots of Figs. 7 and 8 for the case where $a(t)$ and $b(t)$ are PPWC sampled sinusoids with $N = 10$ and $P = 5$. By Prop. 1, $a(t)$ and $b(t)$ have harmonics $1, 9, 11, 19, 21, \ldots$.

Fig. 7 shows the locations of intermodulation products for the single phase mixer (that is, no multiphase cancellation occurs) on the (k, m) plane. Locations of the sum frequency intermodulation products $k\omega_1 + m\omega_2$ are indicated by the $+$ symbol and locations of difference intermodulation products $k\omega_1 - m\omega_2$ are indicated by the Δ symbol. In this case, the sum and difference components are overlapping on the (k, m) plane.

Fig. 8 shows the case where 5 phases are combined to cause cancellation of many intermodulation products.

[1]It can be proven by using the sum of exponentials $\exp(j2\pi rn/P)$.

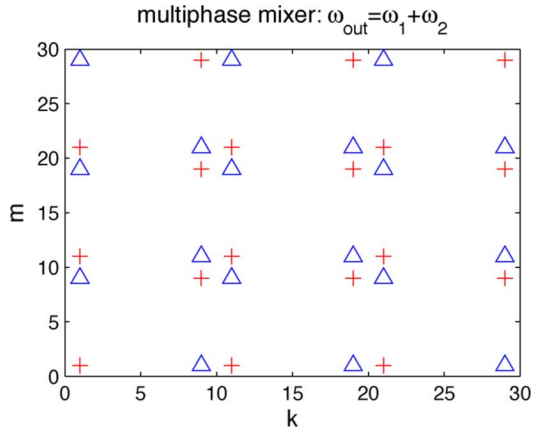

Fig. 9. Intermodulation product locations of a 5-phase mixer with output $\omega_1 + \omega_2$. This 5-phase mixer differs from that of Fig. 8 in that the difference frequency $\omega_1 - \omega_2$ is cancelled and $\omega_1 + \omega_2$ is retained.

Here the $\omega_1 - \omega_2$ component is kept while the $\omega_1 + \omega_2$ component is indeed cancelled as is desired. The multiphase technique can also be used to keep the $\omega_1 + \omega_2$ component and cancel the $\omega_1 - \omega_2$ instead. This is done by inverting the phase offset of one of the phase-shifted signals, i.e.,

$$\begin{aligned} &y_{\omega_1+\omega_2}(t) \\ &\quad = \sum_{n=0}^{P-1} a\left(t + \frac{nT_1}{P}\right) b\left(t - \frac{nT_2}{P}\right) \\ &\quad = \sum_{k=1}^{\infty}\sum_{m=1}^{\infty} \frac{PA_kB_m}{2} \\ &\qquad \times \{\cos((k\omega_1 + m\omega_2)t + \theta_k + \phi_m)\delta[(k-m) \bmod P] \\ &\qquad + \cos((k\omega_1 - m\omega_2)t + \theta_k - \phi_m)\delta[(k+m) \bmod P]\}. \end{aligned} \qquad (21)$$

The resulting plot of intermodulation products on the (k, m) plane is shown in Fig. 9.

The circuit for combining the multiphase products is depicted in Fig. 10 for P phases (this figure does not explicitly show the phase generation shift registers shown earlier in Fig. 4). The products are summed simply by connecting the outputs of the individual mixers at a common node.

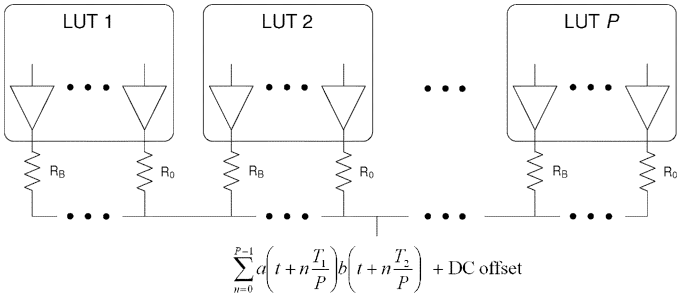

Fig. 10. Multiphase mixer with P phases. Each LUT receives its inputs from a different phase output of the shift registers.

TABLE I
ALL POSSIBLE NONNEGATIVE PRODUCTS OF THE APPROXIMATION FUNCTION FOR TEST CIRCUIT (ALL NEGATIVE VALUES ARE EXACTLY NEGATIVE OF POSITIVE VALUES LISTED)

ideal product	resistor network approximation of product	approximation error	encoding of LUT $\sigma_3, \sigma_2, \sigma_1, \sigma_0$
1	1	0%	1, 1, 1, 1
0.6180340	0.6180308	0.00052%	1, −1, 1, 1
0.3819660	0.3819692	0.00084%	0, 0, 0, 1
0	0	0%	0, 0, 0, 0

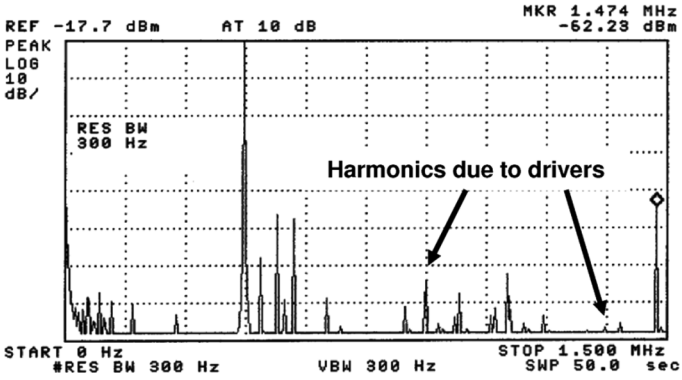

Fig. 11. Spectrum of a single phase mixer for input frequencies 551 kHz and 1 MHz.

VI. MEASUREMENTS

As an example of the proposed optimization method, we considered the case in which $a(t)$ has $N = 10$ divisions of the period. Thus, $a(t)$ lacks harmonics $2, 3, \ldots, 8$, etc. We chose $B = 4$ resistors and restricted the sum of the resistor ratios to be within $M_T = 60$.

The solution to the optimization problem (17) yielded resistor ratios $\mu_0 = 6$, $\mu_1 = 7$, $\mu_2 = 12$, and $\mu_3 = 23$, and, $\theta = \pi/10$.

Table I lists the resulting DAC outputs for generating positive values of $a(t)b(t)$ (in this table we have removed the DAC's dc offset). Recall that the DAC produces values which occur in oppositely signed pairs (for any resistor values, as long as resistors are *pairwise* matched). Thus the negative values of the DAC output are the exact negative of the positive values listed in the table.

For these ideal resistor ratios, this DAC has an equivalent accuracy of approximately 18 bits for producing the desired values using only eight small-ratio resistors.

The complete mixer was implemented using the Xilinx Coolrunner 2 CPLD and discrete resistors. We chose $P = 5$ phases. Note that $P = 5$ and $P = 10$ ideally yield similar output spectrum because $a(t)$ and $b(t)$ possess only odd harmonics.

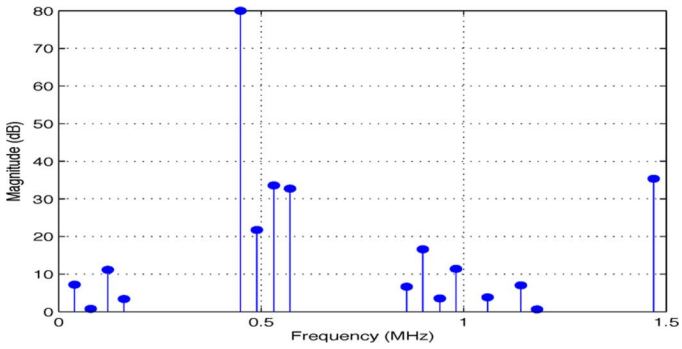

Fig. 12. MATLAB-simulated spectrum of a single phase mixer for input frequencies 0.551 and 1 MHz.

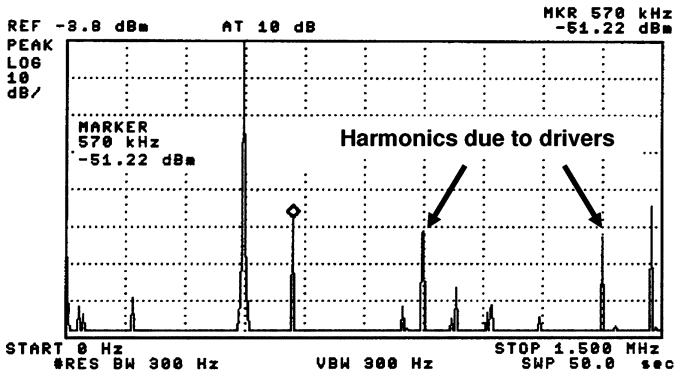

Fig. 13. Spectrum of 5-phase mixer for input frequencies 551 kHz and 1 MHz. Note the presence of harmonics of the output frequency due to distortion from the CMOS drivers.

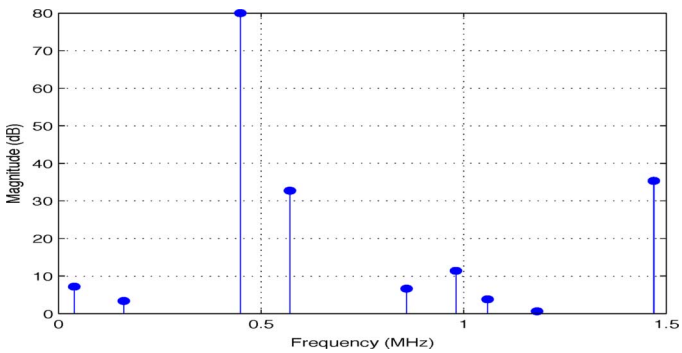

Fig. 14. MATLAB-simulated spectrum of a 5-phase mixer for input frequencies 0.551 and 1 MHz.

This is because the multiphase (20) indicates that an intermodulation product is present only if $(k + m) \bmod P = 0$ or $(k - m) \bmod P = 0$. Since $k \pm m$ is always even, $P = 5$ and $P = 10$ yield similar results.

Fig. 11 shows the measured spectrum of the single-phase mixer. The corresponding MATLAB simulation result is shown in Fig. 12. Fig. 13 shows the measured spectrum for the multiphase mixer, when the desirable output component is the difference frequency. Fig. 14 shows the corresponding MATLAB simulation results.

A. Discussion

Note that the measurement shows the presence of harmonics of the desired output frequency $\omega_1 - \omega_2$. These are most likely due to the nonlinear source resistance of the CMOS buffers driving the resistors; these drivers had significant source resistance, particularly in the PMOS. These harmonics are much

smaller in the measurement of the single phase mixer's spectrum due to the fact that the output signal level is 5 times as large for the 5-phase mixer. If we model the nonlinearity with a Taylor series expansion, then the 2nd harmonic is determined primarily by the quadratic term of the series. Then raising the mixer's output signal voltage by 5 times will raise the 2nd harmonic voltage by 25 times. Thus, while the fundamental component (the desired component) is raised by $20\log 5 = 14$ dB, the 2nd harmonic is raised by $20\log 25 = 28$ dB. Since the 2nd harmonic is -51 dBc in the multiphase measurement, it would be approximately -65 dBc in the single phase measurement. Similar arguments apply for higher order harmonics.

The measurements, obtained with discrete-component test circuits, demonstrate the feasibility of the proposed architecture. The discrepancies between simulation and measurement can be greatly reduced with monolithic implementation.

Due to better matching, one may consider using switched-capacitors (SC) rather than resistors in the nonlinear DAC. However, because the inputs to the mixer are two arbitrary frequencies, their product will, in general, not be synchronous to a clock. This precludes using SC techniques, as it would result in both glitching and aliasing.

A current-mode nonlinear DAC is the best option as it has fewer nonidealities compared to a voltage-mode DAC. As observed earlier, the nonlinearity of the CMOS voltage buffers resulted in the presence of harmonics at the output, since the output signal modulates the buffers' output resistance. Current-steering provides for both fast switching and high spectral purity and can be implemented in standard CMOS processes [18]. In this case, one constructs the nonlinear DAC by choosing optimal transistor sizes rather than resistor sizes. The high current draw of conventional linear current-steering DACs is greatly reduced for the nonlinear DAC, since far fewer current sources are needed (an order of magnitude less). Such a DAC would show greatly reduced effects of signal-dependent distortion observed in measurements.

VII. Conclusion

We have presented a nearly digital frequency mixer. The mixer utilizes nonlinear digital-to-analog conversion and multiphase intermodulation products cancellation to achieve high SFDR. Due to the digital nature of its implementation and the fact that no input analog filters are required, it can easily be integrated in digital CMOS with minimal size and cost.

Appendix

The Appendix provides a proof of Prop. 1 of Section II.

Let $d(t)$ be the periodic delta train with $p_i = p_{i \bmod N}$

$$d(t) = \sum_{i=-\infty}^{\infty} p_i \delta(t - iT/N), \tag{22}$$

Let D_k be the kth Fourier series coefficient of $d(t)$, i.e.,

$$\begin{aligned} D_k &= \frac{1}{T}\int_{0^-}^{T^-} \sum_{i=-\infty}^{\infty} p_i \delta(t - iT/N) e^{-jk\omega_0 t} dt \\ &= \frac{1}{T}\sum_{i=0}^{N-1} p_i e^{-j2\pi ki/N} \end{aligned} \tag{23}$$

where $\omega_0 = 2\pi/T$. The last sum is the N-point DFT of the partial sequence of $p_i, i = 0, 1, \ldots, N-1$ and so from [19]

$$D_k = D_{k \bmod N} \tag{24}$$

and

$$D_k = D^*_{N-k}. \tag{25}$$

The Fourier transform of $d(t)$ is

$$D(\omega) = \sum_{k=-\infty}^{\infty} 2\pi D_k \delta(\omega - k\omega_0).$$

Let $f(t) = d(t) * h(t)$, where $*$ denotes convolution and $h(t)$ is an arbitrary function. Then

$$F(\omega) = D(\omega)H(\omega) = \sum_{k=-\infty}^{\infty} 2\pi D_k H(k\omega_0)\delta(\omega - k\omega_0).$$

Let F_k be the Fourier series coefficients for $f(t)$. Then

$$F_k = D_k H(k\omega_0). \tag{26}$$

Now consider (26) when applied to the case where $h(t)$ is a rectangular pulse

$$h(t) = \begin{cases} 1, & \text{if } t \in [0, T/N) \\ 0, & \text{otherwise.} \end{cases}$$

Then we have

$$H(\omega) = \frac{2}{\omega}\sin\left(\frac{\omega T}{2N}\right) e^{-j\omega\left(\frac{T}{2N}\right)}. \tag{27}$$

The phase shift term in (27) represents only an inconsequential time delay, so we will neglect it in future equations. The convolution of $d(t)$ and $h(t)$ yields a PPWC $f(t)$ with uniform transition times

$$f(t) = \sum_{i=-\infty}^{\infty} p_i h(t - iT/N).$$

Thus, we can represent the PPWC function $a(t)$ as a convolution of the delta train $d(t)$ with the rectangular pulse $h(t)$: $a(t) = d(t) * h(t)$. Thus, we have the following:

Proposition 3: A PPWC function $a(t)$ with period T divided into N partitions has complex Fourier series coefficients

$$A_k = D_k H(k\omega_0) \tag{28}$$

where D_k are Fourier series coefficients given by (23) and

$$H(k\omega_0) = \frac{T}{N}\operatorname{sinc}\left(\frac{k\pi}{N}\right)$$

with $\operatorname{sinc}(x) = \sin(x)/x$.

Note that $H(k\omega_0) = 0$ if and only if k is a nonzero integer multiple of N. For a function without a dc component, $D_k = 0$ for all k that are integer multiples of N, so the locations of null components of A_k are determined by $d(t)$ alone. Since we are interested in signals without a dc component, we have that $A_k = 0 \Leftrightarrow D_k = 0$ when $k = 0, 1, \ldots, N-1$.

By using (24) and (25) the real PPWC function with the fewest harmonics must have a $d(t)$ with nonzero coefficients D_1 and $D_{N-1} = D_1^*$. Applying the inverse DFT to the vector $(0, D_1, 0, \ldots, 0, D_1^*)$, we obtain

$$p_i = \cos\left(\frac{2\pi i}{N} + \theta\right), \tag{29}$$

where $\theta \in [0, 2\pi/N)$. Here $\theta \in [0, 2\pi/N)$ rather than $[0, 2\pi)$ because choosing $\theta \in [2\pi/N, 2\pi)$ is equivalent to some $\theta \in [0, 2\pi/N)$.

By (24) and (25) the PPWC signal with coefficients of the form (29) has nonzero discrete spectral components only at frequencies $(rN + 1)\omega$ and $(rN - 1)\omega$, where r is any integer. This proves Prop. 1.

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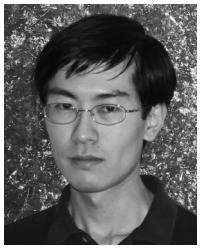

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