Information Capacity of Nanowire Crossbar Switching Networks

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***Abstract*—Crossbar switching networks formed by nanowires are promising future data storage devices. This work addresses the fundamental question: *What is the information storage capacity of a crossbar switching network?* The two major classes of nanowire crossbar switching networks are considered, those with ohmic and those with semiconductive switches. The focus is on the first class which is in the center of current nanotechnology research. Exact, simple approximate, and asymptotic expressions of the information storage capacity are provided as functions of the network size. The derivations indicate technological and geometrical considerations in the design of efficient nanowire devices.**

***Index Terms*—Array, capacity, crossbar, device, information, memory, nanotechnology, nanotube, nanowire, network, storage, switching.**

I. Introduction

RECENT advances in nanotechnology have enabled the development of crossbar switching networks (CSNs) using nanowires [1]–[7]. The small size and high density of these structures makes them favorable candidates for future high density interconnect, computation and information storage devices [1]–[26]. In this work we consider rectangular $N \times M$ crossbar switching networks with *ohmic* (resistive) contact switches between every horizontal and every vertical wire as shown in Fig. 1. Every switch has two possible states, one of high and one of low resistance (*open* and *closed* respectively). We refer to this class of crossbar switching networks as R-CSNs to distinguish them from crossbar switching networks with *semiconductive* (*diode*) switches, D-CSNs, shown in Fig. 2.

The exact information storage capacity of rectangular $N \times M$ R-CSNs is derived along with simple approximate and asymptotic[1] expressions. In particular, it is shown that the capacity of $N \times N$ R-CSNs is asymptotic[1] to $2N \log_2 N$ *bits* for $N \to \infty$. This is in contrast to the capacity of $N \times N$ D-CSNs which is N^2 *bits*. Although D-CSNs are much superior than R-CSNs in terms of capacity, R-CSNs are more prevalent nanostructures currently and they are expected to find significant applications in the future [1], [2].

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[1]In the sense of [27, p. 8].

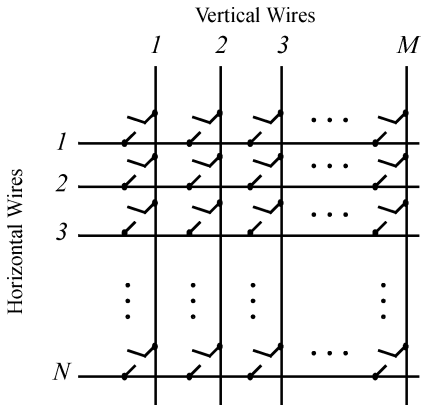


Fig. 1. An $N \times M$ crossbar switching network with ohmic switches.

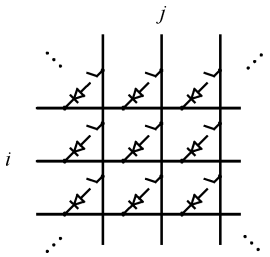


Fig. 2. A crossbar switching network with semiconductive switches.

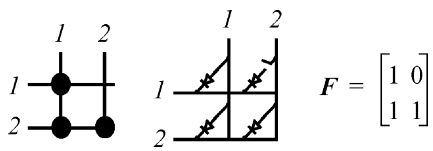


Fig. 3. An R-CSN and a D-CSN having the same configuration.

II. Preliminaries

Throughout the paper we consider rectangular $N \times M$ CSNs with N horizontal and M vertical wires. The numbering of the wires is as shown in Fig. 1, i.e., similar to that of an $N \times M$ matrix. The pair (i, j), with $i = 1, 2, \ldots, N$ and $j = 1, 2, \ldots, M$, is used to denote either the pair of the ith horizontal and jth vertical wires or the corresponding switch between them. For pictorial simplification in R-CSNs *only*, a black *dot* at the intersection (i, j) is used to indicate that switch (i, j) is closed. This convention is shown in Fig. 3. The configuration of the switches in an $N \times M$ CSN is formally defined as follows.

Definition 1: A configuration, $\boldsymbol{F}$, of the switches of $N \times M$ CSNs is an $N \times M$, 0–1 matrix whose i, j entry, $F_{i,j}$, is 0 if the (i, j) switch is open and 1 if the (i, j) switch is closed.

Example 1: A 2×2 R-CSN and D-CSN having the same *configuration* are shown in Fig. 3.

Remark 1: A configuration of a CSN can be viewed as a bipartite graph whose vertices are the sets of the horizontal and the vertical wires and whose edges are the *ones* in matrix F.

Definition 2: Two wires (of any type) are connected if there is a path of closed switches between them, otherwise, they are disconnected.

Remark 2: A path between two *horizontal* wires i_a, i_b is of the form $(i_a, v_1), (h_1, v_1), (h_1, v_2), (h_2, v_2), \ldots, (h_{k-1}, v_{k-1}), (h_{k-1}, v_k), (i_b, v_k)$ and its length, number of switches, is $2k$, $k \geq 1$, i.e., *even*. Similarly, a path between two *vertical* wires j_a, j_b is of the form $(h_1, j_a), (h_1, v_1), (h_2, v_1), (h_2, v_2), \ldots, (h_{k-1}, v_{k-1}), (h_k, v_{k-1}), (h_k, j_b)$ and its length is $2k$, $k \geq 1$, i.e., *even*. Finally, a path between a *horizontal* wire i and a *vertical* wire j is of the form $(i, v_1), (h_1, v_1), (h_1, v_2), (h_2, v_2), \ldots, (h_{k-2}, v_{k-2}), (h_{k-2}, v_{k-1}), (h_{k-1}, v_{k-1}), (h_{k-1}, j)$ and its length is $2k-1$, $k \geq 1$ i.e *odd*.

A. Assumptions

To estimate the information capacity of R-CSNs, we make the following assumptions that are important for every practically useful implementation: 1) The switches have high[2] *open/closed* resistance ratio $r_{\text{open}}/r_{\text{closed}}$. 2) The resistance of the wires is much smaller than the r_{open} of the switches.[2] 3) The states of the switches, *closed* or *open*, can be set independently. These assumptions imply that by measuring the resistance between any two wires we can accurately conclude whether there is a path of closed switches between them or not, i.e., whether the wires are *connected* or not. In other words, the resistance measurement provides the correct *binary* answer. In the analysis that follows, assumptions 1)–3) allow us to think of CSNs as being composed out of ideal switches and ideal wires. In the case of D-CSNs we can consider the diodes as being ideal as well.

B. R-CSN Versus D-CSN

Consider a D-CSN, like that in Fig. 2, with (ideal) diodes whose anodes and cathodes are connected to vertical and horizontal wires, respectively. Let the $N \times M$ switches have a given, yet unrevealed to us, *closed–open* configuration. To extract the particular configuration we can perform a series of $N \times M$ measurements, i.e., for $i = 1, 2, \ldots, N$ and for $j = 1, 2, \ldots, M$ we measure the current $I_{i,j}$ as in Fig. 4; if $I_{i,j}$ is nonnegligible, we conclude that the switch (i, j) is closed, otherwise, we conclude that the switch (i, j) is open.

The main issue here is that the $N \times M$ connections are *independent* in the sense that for every pair (i, j) the measured current $I_{i,j}$ depends *only*[2] on the state of switch (i, j), i.e., it is independent of the state of every other switch. This is in contrast to the case of R-CSNs. In Fig. 5, for example, the resistance between the *first* horizontal and the *second* vertical wires is low in both configurations. Concluding that the $(1, 2)$ switch is closed in both cases is incorrect. Therefore, in R-CSNs, the results of the measurements do *not* necessarily represent the states of the corresponding switches.

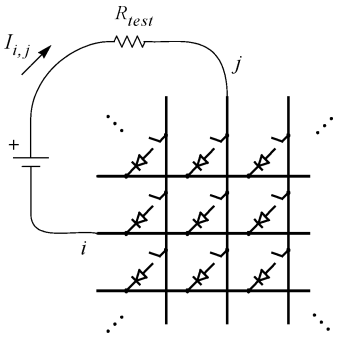


Fig. 4. Extracting the configuration of a D-CSN; the current measurement.

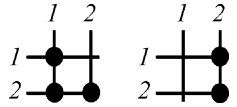


Fig. 5. Two distinguishable configurations of a 2×2 R-CSN.

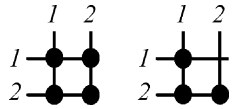


Fig. 6. Two different but indistinguishable configurations of a 2×2 R-CSN.

Although we cannot tell which of the switches are closed or open in the left configuration of Fig. 5, we can still distinguish it from the right one (in Fig. 5) by examining the whole set of $6 = \binom{2+2}{2}$ resistance measurements (every pair of the four wires). By doing so, we infer that the pairs of *connected* wires in the left configuration are $(1, 1), (1, 2), (2, 1)$, and $(2, 2)$, while the pairs of connected wires in the right configuration are $(1, 2)$ and $(2, 2)$. However, we cannot distinguish between the two configurations of the switches in Fig. 6. They imply the same electrical behavior of the network, i.e., all wires are connected together. The above examples and discussion are extended directly to R-CSNs of any sizes N, M.

It is reasonable to assume that the device is connected to the rest of the circuitry through CSN's terminals and that the states of the switches *cannot* be observed from the outside in any other manner, i.e., the switches are *hidden* inside the CSN, as illustrated in Fig. 7.

An $N \times M$ R-CSN with a given configuration of its switches is an $(N+M)$-terminal *device* with a certain electrical behavior. We use the term *device* for the whole set of information we can extract from an R-CSN, with a given configuration, by measuring the resistance between every pair of its terminals (wires),[3] i.e., $\binom{N+M}{2}$ measurements. A formal definition is in order.

[2]Assumptions 1 and 2 can be stated more formally as follows. There is some "threshold" resistance value R_T such that for every given configuration of the switches: a) the (total) resistance between any "point" on a wire a and any "point" on another wire b is less than R_T if and only if the two wires are *connected* (Definition 2).

[3]Following the assumptions stated before, we consider the results of resistance measurements being binary and correct in the sense that we measure low resistance between two wires if and only if there is a path of closed switches between them.

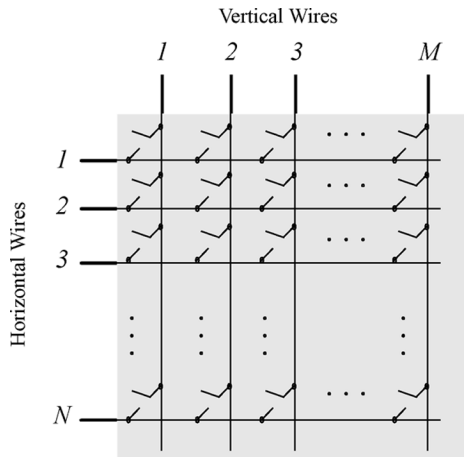


Fig. 7. The R-CSN as an $N + M$ terminal device.

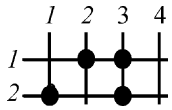


Fig. 8. The 2×4 R-CSN of Example 2.

Definition 3: A device, $\boldsymbol{D}$, realized by an $N \times M$ R-CSN along with a given configuration of its switches, is an $N \times M$, 0–1 matrix whose i, j entry $\boldsymbol{D}_{i,j}$ is 1 if the ith horizontal wire is *connected* to the jth vertical wire, through any connection path, and 0 otherwise. The set of devices realized by an $N \times M$ R-CSN is denoted by D_S and is a subset of $\{0,1\}^{N \times M}$.

Remark 3: According to the previous discussion one might expect that a device is not defined as an $N \times M$, 0–1 matrix but rather as an $(N + M) \times (N + M)$ matrix $\overline{\boldsymbol{D}}$ representing the conductivity between every wire pair (including the degenerate same-wire pair). However, following Remark 2, two distinct horizontal wires are connected if and only if there is a vertical one that is connected to both of them. Similarly, for a pair of vertical wires. Therefore,

$$\overline{\boldsymbol{D}} = \left[\begin{bmatrix} \boldsymbol{D}\boldsymbol{D}^T & \boldsymbol{D} \\ \boldsymbol{D}^T & \boldsymbol{D}^T\boldsymbol{D} \end{bmatrix} \right]_{>0}$$

where for a real matrix $\boldsymbol{A} = (\boldsymbol{a}_{i,j})$, $[\boldsymbol{A}]_{>0}$ is a 0–1 matrix, of the same dimension ,with 1 in the i, j entry if $a_{i,j} > 0$ and zero otherwise. So $\overline{\boldsymbol{D}}$ and $\boldsymbol{D}$ carry the same amount of information.

Example 2: The R-CSN of Fig. 8 has configuration

$$\boldsymbol{F} = \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 0 \end{bmatrix}$$

and realizes the device

$$\boldsymbol{D} = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 \end{bmatrix}.$$

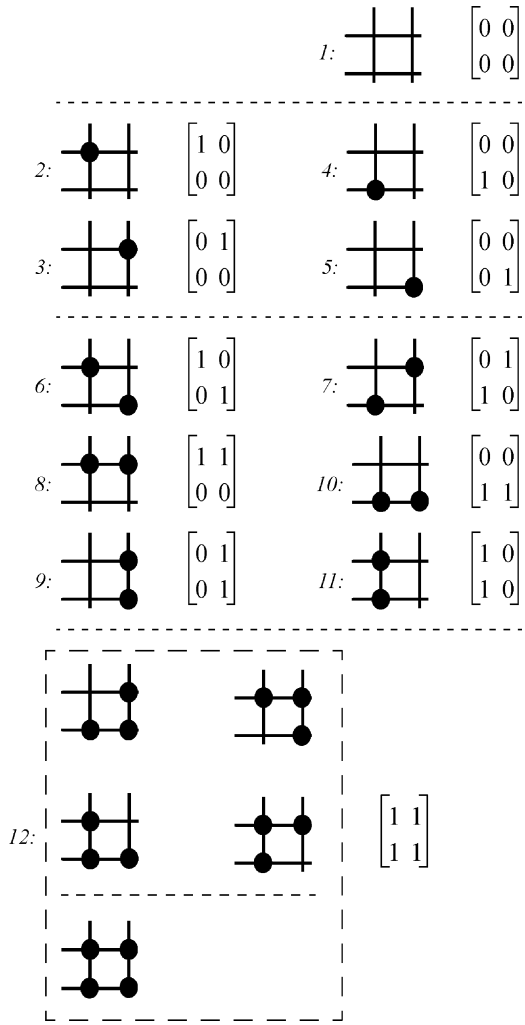


Fig. 9. The 16 configurations of a 2×2 *R-CSN* realize only 12 devices.

Example 3: 2×2 R-CSNs have 16 configurations that realize 12 devices. All are shown in Fig. 9. A device may be realized by more than one configuration, for example, all five configurations

$$\begin{bmatrix} 0 & 1 \\ 1 & 1 \end{bmatrix}, \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}, \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}, \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}, \text{ and } \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$$

realize the device $\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$.

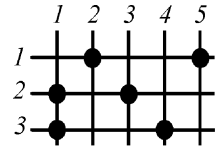
The following lemma provides a relation between configurations of the switches and their corresponding devices.

Lemma 1: If $\boldsymbol{F}$ is a configuration of $N \times M$ R-CSNs, $\boldsymbol{D}$ is the corresponding device and $K = \min\{N, M\}$, then

$$\boldsymbol{D} = [\boldsymbol{F} + \boldsymbol{F}\boldsymbol{F}^T\boldsymbol{F} + (\boldsymbol{F}\boldsymbol{F}^T)^2\boldsymbol{F} + \cdots + (\boldsymbol{F}\boldsymbol{F}^T)^{K-1}\boldsymbol{F}]_{>0} \quad (1)$$

where operator $[\cdot]_{>0}$ is defined in Remark 3.

Proof: Consider an $N \times M$ R-CSN with a configuration $\boldsymbol{F}$. Entry $(\boldsymbol{F})_{i,j}$ is the number of length-1 paths (length = number of switches) between the ith horizontal wire and the jth vertical one (i.e., if $(\boldsymbol{F})_{i,j} = 1$ switch (i, j) is closed and the two wires are connected, if $(\boldsymbol{F})_{i,j} = 0$ the wires are not connected by a length-1 path). Recall from Remark 2 that all paths between a horizontal and a vertical wire have



$$\Leftrightarrow \boldsymbol{F} = \begin{bmatrix} 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \end{bmatrix}$$

Fig. 10. A 3×5 R-CSN with a given configuration.

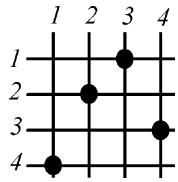


Fig. 11. Example: 1–1 connection of the wires.

odd length. Moreover, the number of length-$(2k-1)$ paths between the ith horizontal wire and the jth vertical one is $((\boldsymbol{F}\boldsymbol{F}^T)^{k-1}\boldsymbol{F})_{i,j}$ [30]. Every such path involves k horizontal and k vertical wires. Therefore, the i,j entry of the matrix

$$\Phi = \boldsymbol{F} + \boldsymbol{F}\boldsymbol{F}^T\boldsymbol{F} + (\boldsymbol{F}\boldsymbol{F}^T)^2\boldsymbol{F} + \cdots + (\boldsymbol{F}\boldsymbol{F}^T)^{K-1}\boldsymbol{F}$$

equals the number of paths between the ith horizontal wire and the jth vertical one of length less than or equal to $2K-1$, and, since there exist only N horizontal and M vertical wires, it suffices to take $K = \min\{N, M\}$ in order to include all simple paths.

□

Example 4: Consider the 3×5 R-CSN in Fig. 10. It is

$$\boldsymbol{F} = \begin{bmatrix} 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 \end{bmatrix}$$

and $K = \min\{3, 5\} = 3$. Therefore,

$$\Phi = \boldsymbol{F} + \boldsymbol{F}\boldsymbol{F}^T\boldsymbol{F} + (\boldsymbol{F}\boldsymbol{F}^T)^2\boldsymbol{F} = \begin{bmatrix} 0 & 7 & 0 & 0 & 7 \\ 13 & 0 & 8 & 5 & 0 \\ 13 & 0 & 5 & 8 & 0 \end{bmatrix}$$

and the realized device is

$$\boldsymbol{D} = [\Phi]_{>0} = \begin{bmatrix} 0 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 \end{bmatrix}.$$

C. The Notion of Capacity

Consider an $N \times M$ D-CSN like that in Fig. 2. All 2^{NM} configurations of the switches are distinguishable[4] using the current measurement tests in Fig. 4. Every configuration corresponds in a one-to-one fashion to a unique electrical behavior, i.e., a *device*. Therefore, the information capacity of the network is $NM = \log_2 2^{NM}$ bits. By extending this idea to the case of R-CSNs, the storage capacity of an $N \times M$ R-CSN is $B = \log_2 D$ bits, where D is the number of devices that can be realized by it.

[4]See the discussion in the beginning of Section II-B Every measurement in Fig. 4 is independent of the other ones.

A simple exact and an asymptotic lower bound of the capacity B is derived in the following lemma.

Lemma 2: The information capacity B of $N \times N$ R-CSNs is at least $\log_2(N!)$ bits and is asymptotically equal to or greater than $N \log_2 N$ bits as $N \to \infty$.

Proof: There are $N!$ configurations of the switches such that every horizontal wire is connected to exactly one vertical wire (e.g., Fig. 11). Therefore, $B \geq \log_2(N!)$ bits. Also, for every N, there exists θ_N, $0 < \theta_N < 1$, such that

$$N! = \sqrt{2\pi} N^{N+\frac{1}{2}} \exp\left(-N + \frac{\theta_N}{12}\right)$$

[29]. We conclude that $\lim_{N\to\infty} \frac{\log N!}{N \log N} = 1$. □

III. The Number of Devices

To simplify notation, we use subscript h to indicate *horizontal* wires and subscript v to indicate *vertical* wires. The set of all wires of the R-CSN is $T = \{1_h, 2_h, \ldots, N_h, 1_v, 2_v, \ldots, M_v\}$.

Definition 4: The connectivity partition of a device $\boldsymbol{D}$ is a partition P of the wires' set T such that two wires are in the same block of P if and only if they are connected (through a path). Every wire that is not connected to any other wire forms a singleton in the partition.

Example 5: The wires' set of the 2×2 R-CSNs in Fig. 5 is $T = \{1_h, 2_h, 1_v, 2_v\}$. The connectivity partitions of the devices realized by the left and the right configurations in Fig. 5 are $P_1 = \{\{1_h, 2_h, 1_v, 2_v\}\}$ and $P_2 = \{\{1_h, 2_h, 2_v\}, \{1_v\}\}$, respectively. Compare P_1 and P_2 with their corresponding devices $\begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix}$ and $\begin{bmatrix} 0 & 1 \\ 0 & 1 \end{bmatrix}$, respectively.

Example 6: The wires' set of the 3×5 R-CSN in Fig. 10 is $T = \{1_h, 2_h, 3_h, 1_v, 2_v, 3_v, 4_v, 5_v\}$ and the connectivity partition corresponding to that particular configuration is

$$P = \{\{1_h, 2_v, 5_v\}, \{2_h, 3_h, 1_v, 3_v, 4_v\}\}.$$

Remark 4: The connectivity partition of an R-CSN with a given configuration, and the device it realizes carry exactly the same amount of information. In several instances one is more convenient to use than the other.

Remark 5: Although every device has a unique connectivity partition, there are connectivity partitions that do not correspond to any device. For example, there is no device realized by a 2×2 R-CSN having connectivity partition $P = \{\{1_h, 2_h\}, \{1_v, 2_v\}\}$ because for any two horizontal wires to be connected, to each other, they must be connected to a vertical ones as well.

Definition 5: Let Θ be the set of all partitions of the wires' set T having the following properties: for every $P \in \Theta$ and every block $S \in P$, S is either a singleton or it contains at least one horizontal and at least one vertical wire.

Lemma 3: The set Θ contains the connectivity partitions of all devices realized by $N \times M$ R-CSNs and no other partition of T.

Proof: Let P be the connectivity partition of a device realized by an $N \times M$ R-CSN. Let $S \in P$ be a block of it. By definition S is not empty. If S is not a singleton, then, not all wires in S can be horizontal because in this case they cannot be connected to each other, similarly, not all wires in S can be vertical. Therefore, $P \in \Theta$.

Conversely: given $P \in \Theta$ we close all switches (a, b) of the $N \times M$ R-CSN, such that a and b belong to some (the same) block $S \in P$, a is a horizontal wire, and b is a vertical wire.[5] We open all the remaining switches. Let $\boldsymbol{D}$ be the realized device and Q its connectivity partition. We show that $P = Q$. Note that P is finer than Q since every block S of P is by construction a subset of a block $\tilde{S}$ of Q. Now we show that $S = \tilde{S}$. Let $S = \{a_1, a_2, \ldots, a_r, b_1, b_2, \ldots, b_t\}$ where a_i's are the horizontal wires and b_i's are the vertical wires in S. Suppose that there exists a horizontal wire $a \in \tilde{S} - S$. By construction of the configuration, there exists a minimum-length path of closed switches from a to either a vertical or a horizontal wire in S. The last switch in this path connects a wire in $\tilde{S} - S$ with a wire in S. By construction again, this switch is open, therefore, we have a contradiction. Hence, it must be $S = \tilde{S}$ and so $P = Q$. □

Remark 6: Note that the correspondence between devices and connectivity partitions is bijective. Therefore, Lemma 3 leads to the following corollary that will be used in the counting of the devices realized by R-CSNs.

Corollary 1: The number of devices, D, realizable by $N \times M$ R-CSNs is $|\Theta|$.

Instead of using brute-force enumeration of all possible connectivity partitions to calculate D, we can construct a bijective map between the set of connectivity partitions, Θ, and another set whose elements we can enumerate easier. This is done in Lemma 4.

Note that the sets of the horizontal and the vertical wires of an $N \times M$ R-CSN are denoted by $\boldsymbol{H} = \{1_h, 2_h, \ldots, N_h\}$ and $\boldsymbol{V} = \{1_v, 2_v, \ldots, M_v\}$, respectively.

Lemma 4: The set of connectivity partitions of $N \times M$ R-CSNs, Θ, can be mapped bijectively into the set Ω containing the six-tuples (H, V, q, P, R, f) satisfying the following properties 1) to 6):

1) H is a proper subset of $\boldsymbol{H}$, possibly the empty set.
2) V is a proper subset of $\boldsymbol{V}$, possibly the empty set.
3) q is an integer such that $1 \leq q \leq \min\{N - |H|, M - |V|\}$.
4) P is a partition of $\boldsymbol{H} - H$ into q (nonempty) blocks.
5) R is a partition of $\boldsymbol{V} - V$ into q (nonempty) blocks.
6) f is a bijection from P to R.

and the six-tuple $(\boldsymbol{H}, \boldsymbol{V}, 0, \emptyset, \emptyset, f_d)$, where $f_0 : \{0\} \to \{0\}$ is a dummy function.

Proof: The lemma is proved by constructing a bijection $g : \Theta \to \Omega$. Consider a connectivity partition $P_{\boldsymbol{D}} = \{T_1, T_2, \ldots, T_r\}$ in Θ corresponding to a device $\boldsymbol{D}$. Let H be the set of the horizontal wires that are *not* connected to any (vertical) wire; similarly, let V be the set of the vertical wires that are *not* connected to any (horizontal) wire. Set $i = |H|$, $j = |V|$, and $q = r - (i + j)$, it may be $i = 0$ or $j = 0$. Note that the $i + j$ wires in $H \cup V$ appear as singletons in $P_{\boldsymbol{D}}$. Without loss of generality, we assume that $T_{q+1}, T_{q+2}, \ldots, T_r$ are these singletons and so $H \cup V = T_{q+1} \cup \cdots \cup T_r$, i.e., all disconnected wires.

If $q = 0$, then $P_{\boldsymbol{D}}$ contains only singletons and so $H = \boldsymbol{H}$, $V = \boldsymbol{V}$. In this case, we set $g(P_{\boldsymbol{D}}) = (\boldsymbol{H}, \boldsymbol{V}, 0, \emptyset, \emptyset, f_0)$. If $q > 0$, every one of the remaining subsets $T_1, T_2, \ldots, T_q$ contains at least one horizontal and one vertical wire.[6] For $k = 1, 2, \ldots, q$, T_k is uniquely decomposed as $T_k = H_k \cup V_k$ where $H_k \subset \boldsymbol{H}$ and $V_k \subset \boldsymbol{V}$. We define P, R to be the partitions $P = \{H_1, H_2, \ldots, H_q\}$, $R = \{V_1, V_2, \ldots, V_q\}$ of the sets $\boldsymbol{H} - H$ and $\boldsymbol{V} - V$, respectively (based on the connectivity of the wires). The six-tuple is completed by defining the bijection f from P to R such that $f(H_k) = V_k$ for $k = 1, 2, \ldots, q$. Finally, we set $g(P_{\boldsymbol{D}}) = (H, V, q, P, R, f)$.

Surjectivity: Starting from a six-tuple (H, V, q, P, R, f) in Θ we configure an $N \times M$ R-CSN in the following way. If $(H, V, q, P, R, f) = (\boldsymbol{H}, \boldsymbol{V}, 0, \emptyset, \emptyset, f_0)$, we open all switches. Otherwise, we close all switches (a, b) such that $a \in S$ and $b \in f(S)$ for some $S \in P$ and we open all remaining ones. Let $\boldsymbol{D}$ be the realized device and $P_{\boldsymbol{D}}$ its corresponding connectivity partition. It is straightforward to verify that $g(P_{\boldsymbol{D}}) = (H, V, q, P, R, f)$.

Injectivity: Consider two distinct connectivity partitions $P_{\boldsymbol{D}_1}$, $P_{\boldsymbol{D}_2}$ of $N \times M$ R-CSNs corresponding to devices $\boldsymbol{D}_1$, $\boldsymbol{D}_2$, respectively, and let

$$g(P_{\boldsymbol{D}_1}) = (H^1, V^1, q^1, P^1, R^1, f^1)$$

and

$$g(P_{\boldsymbol{D}_2}) = (H^2, V^2, q^2, P^2, R^2, f^2).$$

Since $P_{\boldsymbol{D}_1} \neq P_{\boldsymbol{D}_2}$, there must exist two wires w_1, w_2 (horizontal, vertical, or both) that are connected, to each other, in one of the devices and not in the other one. If

$$(H^2, V^2, q^2, P^2, R^2) \neq (H^1, V^1, q^1, P^1, R^1)$$

we conclude that $g(P_{\boldsymbol{D}_1}) \neq g(P_{\boldsymbol{D}_2})$. If

$$(H^2, V^2, q^2, P^2, R^2) = (H^1, V^1, q^1, P^1, R^1)$$

then one of w_1, w_2 must be horizontal and one must be vertical. This along with the assumption about the connectivity of two wires imply that $f^1 \neq f^2$ which leads to $g(P_{\boldsymbol{D}_1}) \neq g(P_{\boldsymbol{D}_2})$. □

The following corollary results from the combination of Corollary 1 and Lemma 4.

Corollary 2: The capacity of the R-CSN is $B = \log_2 |\Omega|$.

IV. Exact Expressions for R-CSNs' Capacity

The following theorem provides the exact information capacity of $N \times M$ R-CSNs. The expressions involve Stirling's numbers of the second kind $S(n, m)$. By definition, $S(n, m)$ is

[5] Notation is slightly violated here.

[6] It is not possible to have two horizontal wires connected together without being connected to a vertical wire.

TABLE I
THE NUMBER OF DEVICES, $D(N, M)$

		M								
		1	2	3	4	5	6	7	8	9
N	1	2	-	-	-	-	-	-	-	-
	2	4	12	-	-	-	-	-	-	-
	3	8	34	128	-	-	-	-	-	-
	4	16	96	466	2100	-	-	-	-	-
	5	32	274	1688	9226	48032	-	-	-	-
	6	64	792	6154	40356	245554	1444212	-	-	-
	7	128	2314	22688	177466	1251128	8380114	54763088	-	-
	8	256	6816	84706	788100	6402586	48510036	354298186	2540607060	-
	9	512	20194	320168	3541066	33044432	281910994	2288754728	18082589146	140893490432

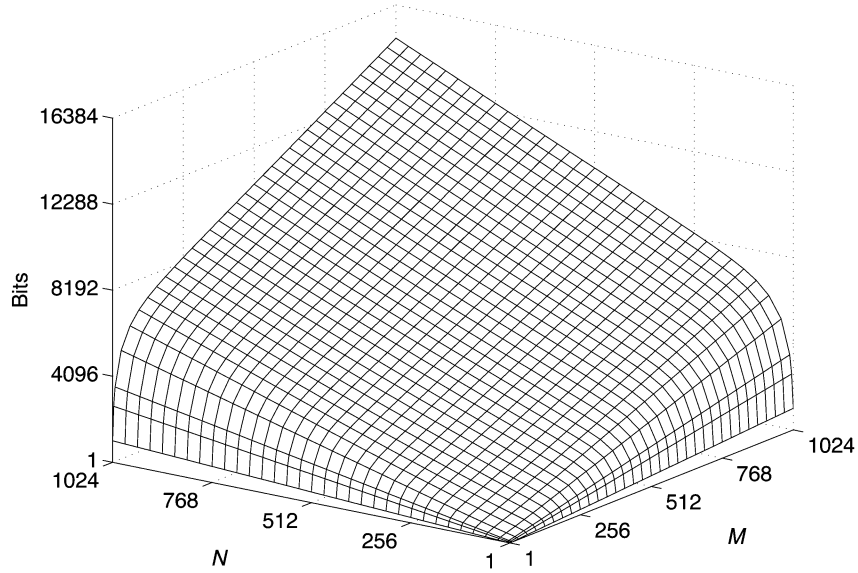


Fig. 12. Information capacity of $N \times M$ R-CSNs for independently varying N and M.

the number of distinct ways that a set of n elements can be partitioned into m nonempty subsets [28]. A useful expression of $S(n, m)$ is given by (2) [29]

$$S(n,m) = \frac{1}{m!}\sum_{t=0}^{m}(-1)^{m-t}\binom{m}{t}t^n. \tag{2}$$

Theorem 1: The information capacity of $N \times M$ R-CSNs is $B = log_2(D)$ bits, where

$$D = 1 + \sum_{i=0}^{N-1}\sum_{j=0}^{M-1}\binom{N}{i}\binom{M}{j} \times \sum_{q=1}^{\min\{N-i,M-j\}} S(N-i,q)S(M-j,q)q!. \tag{3}$$

Proof: The proof is based on Corollary 2, the definitions of Ω, $\boldsymbol{H}$, $\boldsymbol{V}$, H, V, i, j, P, R, q in Lemma 4 and its proof, and the enumeration of the elements in Ω. We count 1 for $(\boldsymbol{H}, \boldsymbol{V}, 0, \emptyset, \emptyset, f_0)$, corresponding to the case that all wires are disconnected and we use properties 1)–6) of the rest of the elements in Ω. For $i = 0, 1, \ldots, N-1$ and $j = 0, 1, \ldots, M-1$, there are $\binom{N}{i}\binom{M}{j}$ ways to choose the sets of disconnected horizontal and vertical wires $H \subset \boldsymbol{H}$ and $V \subset \boldsymbol{V}$ such that $|H| = i$ and $|V| = j$. Then, q, the number of block in partitions P and R, ranges from 1 to $\min\{N - |H|, M - |V|\}$. For every value of q, we can choose partition P in $S(N - i, q)$ possible ways[7] and partition R in $S(M - j, q)$ possible ones. Finally, there are $q!$ ways to map P into R bijectively. □

The values of $D(N, M)$ for $N, M = 1, 2, \ldots, 9$ are shown in Table I. Note that $D(N, M) = D(M, N)$.

The information capacity $B = \log_2(D)$ (bits) of $N \times M$ R-CSNs is shown in Fig. 12, where the sizes N, M vary independently from 1 to 1024. As expected, the maximum capacity is achieved for maximum sizes.

A. The Capacity When $N + M$ is Fixed

In practical circuits the sizes N, M may have to satisfy certain constraints due to physical size, circuit related or other limitations. It is interesting to examine how the capacity depends on such possible constraints. For example, Fig. 13 shows the capacity of $N \times M$ R-CSNs when the number of terminals $N+M$

[7]Note that $|\boldsymbol{H} - H| = N - i$, $|\boldsymbol{V} - V| = M - j$, and use the definition of Stirling's numbers of the second kind.

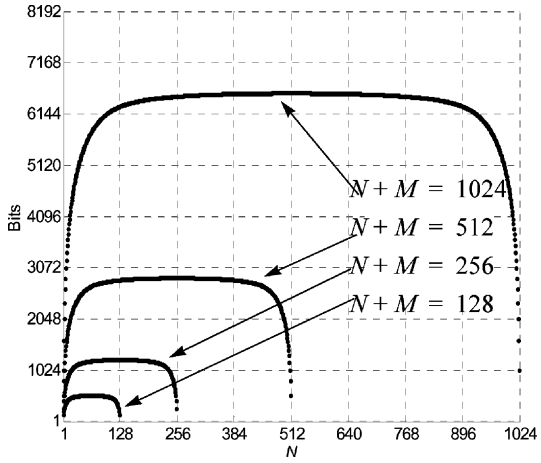


Fig. 13. Information capacity of $N \times M$ R-CSNs, as a function of N, when $N + M$ is fixed.

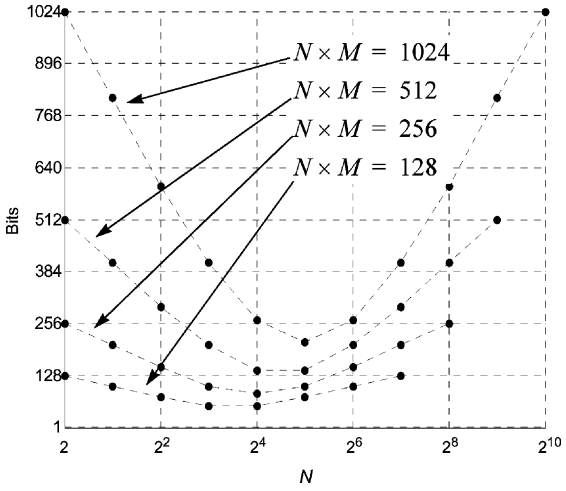


Fig. 14. Information capacity of $N \times M$ R-CSNs, as a function of N, when NM is fixed.

is fixed and equals 128, 256, 512, and 1024, while N varies between 1 and 127, 255, 511, and 1023, respectively. Capacity is maximized when $N = M$.

B. The Capacity When NM is Fixed

In the case of D-CSNs, the capacity depends only on the product NM of their sizes. How does the capacity of R-CSNs depend on the product NM? In Fig. 14, we see the graphs of the capacity for varying N when the product NM is fixed. The capacity is maximized when $N = 1$ or $M = 1$. This is expected since in this case all 2^{NM} configurations of the switches result in distinct devices. The graphs are convex and the capacity is minimized when $|N - M|$ is minimum; if $NM = p^2$ for some integer p, the minimum is achieved when $M = N = p$.

C. More Compact Expressions of D and B

By changing the order of summation in (3), we can get the alternative expression for D given in Corollary 3. The proof is similar to that of Theorem 1; here we count first with respect to the number of the blocks in the partitions q, then we count with respect to the number of disconnected horizontal and vertical wires.

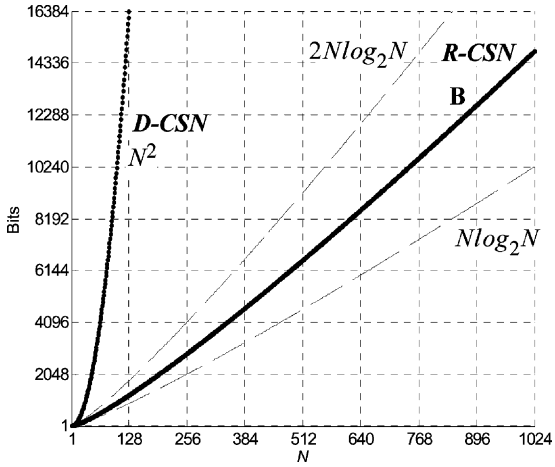


Fig. 15. Exact expression and bounds for the capacity of $N \times N$ R-CSNs, in comparison with the capacity of D-CSNs.

Corollary 3: The number of devices D can be expressed as

$$D = 1 + \sum_{q=1}^{\min\{N,M\}} \sum_{i=0}^{N-q} \sum_{j=0}^{M-q} \binom{N}{i} \binom{M}{j} \times S(N-i,q)S(M-j,q)q!. \quad (4)$$

A compact expression of D and B is given by Theorem 2.

Theorem 2: The information capacity of $N \times M$ R-CSNs is $B = \log_2(D)$ bits where

$$D = \sum_{q=0}^{\min\{N,M\}} S(N+1,q+1)S(M+1,q+1)q!. \quad (5)$$

Expression (5) can be used in commbnation with (2) for the exact calculation of the capacity. In the case of square $N \times N$ R-CSNs, expression (5) simplifies to

$$D = \sum_{q=0}^{N} S(N+1,q+1)^2 q!. \quad (6)$$

It can be shown that $B = \log_2(D)$ is bounded below by $N\log_2(N)$ for every N (see Section VII) and bounded above by $2N\log_2(N)$ for $N \geq 2$ (proof of Theorem 3 in the Appendix). Fig. 15 presents the graphs of the three expressions along with that of the capacity of D-CSNs. The dependence of the ratio $\frac{B(N)}{N\log_2(N)}$ on N is illustrated in Fig. 16.

The proof of Theorem 2 is based on the following lemma that introduces an identity on Stirling numbers of the second kind.

Lemma 5: For every two positive integers n, m with $n \geq m$

$$S(n+1,m+1) = \sum_{j=0}^{n-m} \binom{n}{j} S(n-j,m). \quad (7)$$

Proof: Recall that $S(n,m)$ is the number of partitions of a set with n elements into m nonempty blocks [28]. Now, consider the set $A = \{1,2,\ldots,n,n+1\}$ and let m be a fixed pos-

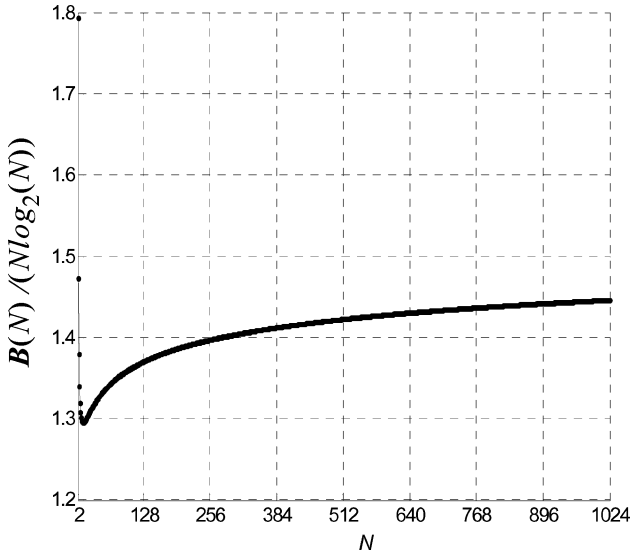


Fig. 16. The capacity of $N \times N$ R-CSNs relative to $N \log_2(N)$ for small to medium values of N.

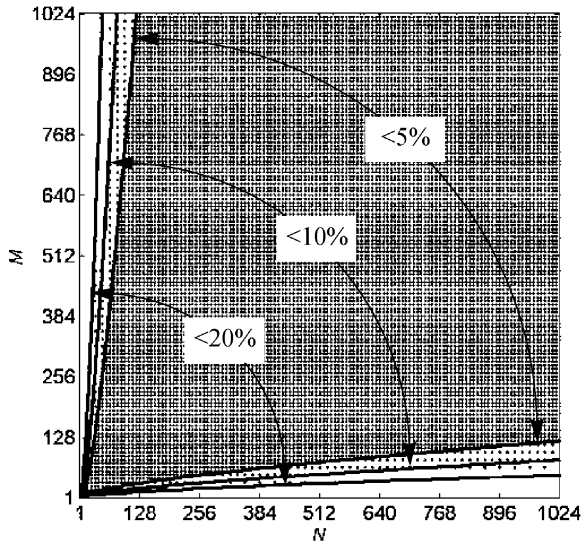


Fig. 17. Percentile difference between $B_1(N, M)$ and capacity $B(N, M)$.

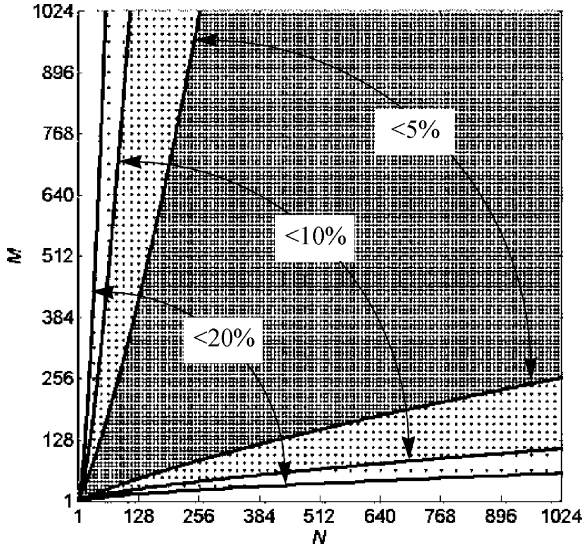


Fig. 18. Percentile difference between $B_2(N, M)$ and capacity $B(N, M)$.

itive integer with $m \leq n$. Let U be the set of all partitions of A into $m+1$ nonempty blocks, it is $|U| = S(n+1, m+1)$. The set U can be partitioned itself into $n+1-m$ blocks, $U_0, U_1, \ldots, U_{n-m}$, where U_j is the set of all partitions of A whose block containing the element $n+1$ has exactly $j+1$ elements (totally). There are $\binom{n}{j}$ subsets of A containing the element $n+1$ and having exactly $j+1$ elements (totally) and there are $S(n-j, m)$ ways that the remaining $n+1-(j+1)$ elements of A can be partitioned into m blocks. Therefore,

$$|U_j| = \binom{n}{j} S(n-j, m)$$

and since $|U| = \sum_{j=0}^{n-m} |U|$ we conclude that

$$S(n+1, m+1) = \sum_{j=0}^{n-m} \binom{n}{j} S(n-j, m). \qquad \square$$

Proof of Theorem 2: Rewriting (4) as

$$D = 1 + \sum_{q=1}^{\min\{N,M\}} \left(\sum_{i=0}^{N-q} \binom{N}{i} S(N-i, q) \right) \times \left(\sum_{j=0}^{M-q} \binom{M}{j} S(M-j, q) \right) q!$$

and applying Lemma 5 twice we derive (5). $\square$

V. Approximate Expressions for R-CSNs' Capacity

The exact calculation of R-CSNs' capacity, $B(N, M)$, may not be an easy computational task for large sizes M and N, and it may even be practically impossible for very large M and N. This motivates the derivation of low-complexity approximate expressions of the capacity. Such an expression is

$$B_1(N, M) = (N + M - q)\log_2(q) + q\log_2(e) \text{ bits} \quad (8)$$

with

$$q = \frac{N+M}{\ln(N+M)}$$

where ln is the natural logarithm and $e = 2.7183\ldots$. Note that $B_1(N, M)$ depends only on the sum, $N+M$, of the sizes and not explicitly on the pair (N, M). Fig. 17 shows the percentile error $100 \times \frac{B_1(N,M) - B(N,M)}{B(N,M)}\%$ of the approximation when N and M range from 1 to 1024. The approximation of $B(N, M)$ by $B_1(N, M)$ improves percentage-wise as $N, M \to \infty$. For large N, M, the approximation can be improved further if q is replaced by $\bar{q}$, the real solution of the transcendental equation $N + M = \bar{q}\log_2(\bar{q})$.

A simpler, empirical, but less accurate approximation of the capacity $B(N, M)$ is given by function $B_2(N, M)$ in (9). It also

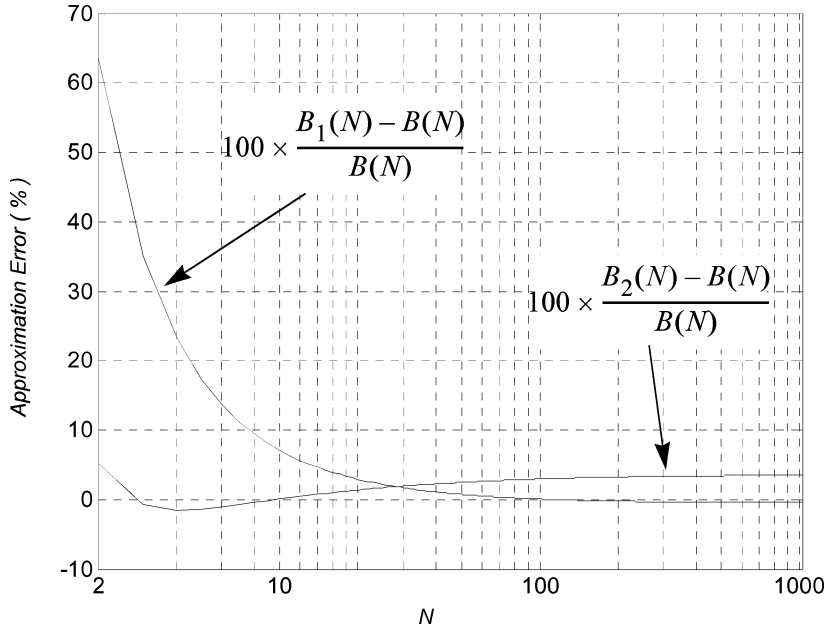


Fig. 19. Percentile difference between $B_1(N)$, $B_2(N)$ and capacity $B(N)$.

depends only on $N + M$ and is more accurate for large values of both N and M

$$B_2(N, M) = (N + M) \log_2 \left(\frac{2}{3} \cdot \frac{N + M}{\ln(N + M)} \right) \text{ bits.} \quad (9)$$

Fig. 18 presents the percentile error $100 \times \frac{B_2(N,M) - B(N,M)}{B(N,M)}\%$ of $B_2(N, M)$ when N and M range from 1 to 1024.

In the case of square $N \times N$ *R-CSNs*, expressions (8) and (9) become (10) and (11), respectively.

$$B_1(N) = (2N - q) \log_2(q) + q \log_2(e) \text{ bits} \quad (10)$$

with $q = \frac{2N}{\ln(2N)}$ and

$$B_2(N) = 2N \log_2 \left(\frac{4N}{3 \ln(2N)} \right). \quad (11)$$

Their percentile errors

$$100 \times \frac{B_1(N) - B(N)}{B(N)}\% \quad \text{and} \quad 100 \times \frac{B_2(N) - B(N)}{B(N)}\%$$

are shown in Fig. 19. Note that the x-axis is in *log-scale*.

VI. Asymptotic Capacity of R-CSNs

The information capacity $B(N)$ of square $N \times N$ R-CSNs is asymptotic to $2N \log_2 N$ for N approaching infinity. This is stated formally in Theorem 3 that is proved in the Appendix.

Theorem 3: The capacity $B(N) = log_2 D(N)$ of $N \times N$ R-CSNs has the property

$$\lim_{N \to \infty} \frac{B(N)}{N \log_2(N)} = 2. \quad (12)$$

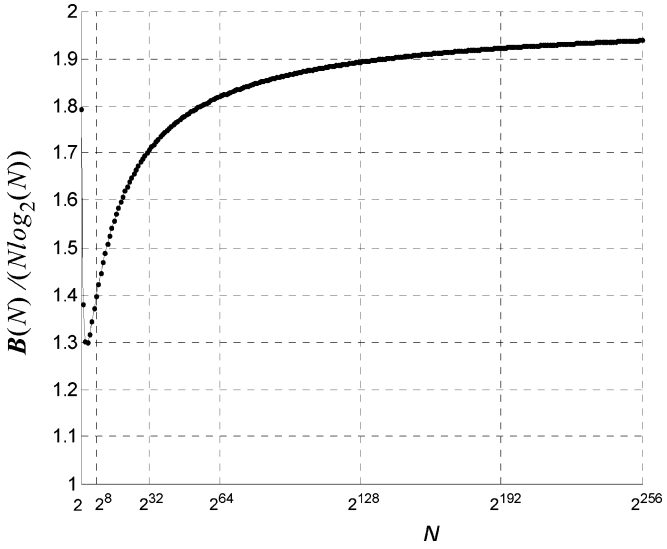


Fig. 20. The capacity of $N \times N$ R-CSNs relative to $N \log_2(N)$ for very large values of N.

Remark 7: Note that the statement is stronger than saying "$B(N)$ is in the order of $N \log_2 N$," which could have been derived using complexity theory, e.g., [23], [24].

Remark 8: Due to the nature of the asymptotic approximation of the capacity, the ratio $\frac{B(N)}{N \log_2(N)}$ approaches the limit 2 only for very large values of N. Fig. 20 shows the graph of this ratio for N ranging from 2^1 to 2^{256}.

Similarly, the information capacity $B(N, M)$ of rectangular $N \times M$ R-CSNs is asymptotic to $(N + M) \log_2(N + M)$ for *both* N and M approaching infinity. The proof of Theorem 4 is similar to that of Theorem 3 and is omitted.

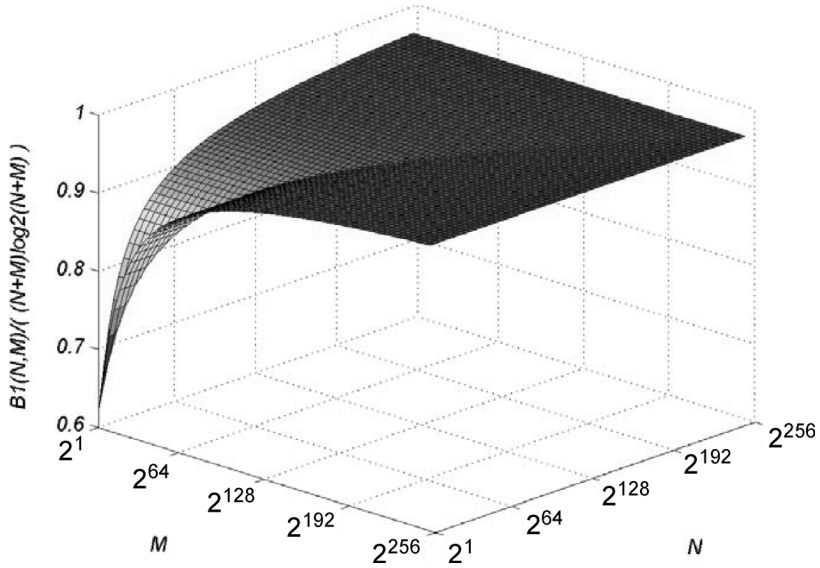


Fig. 21. The capacity of $N \times M$ R-CSNs relative to $(N+M)\log_2(N+M)$ for very large values of N and M.

Theorem 4: The capacity $B(N,M) = \log_2 D(N,M)$ of $N \times M$ R-CSNs has the property

$$\lim_{\substack{N,M\to\infty \\ N/M\to a>0}} \frac{B(N,M)}{(N+M)\log_2(N+M)} = 1. \tag{13}$$

Fig. 21 presents the ratio of the capacity, approximated using function $B_1(N,M)$, over the asymptotic expression $(N+M)\log_2(N+M)$. The approximation error is insignificant for large N, M. The slice $N = M$ coincides with the graph in Fig. 20.

Since N, M are positive, it is

$$N\log_2(N) + M\log_2(M) < (N+M)\log_2(N+M).$$

Moreover, $x\log_2(x)$ is convex, so for $a \in [0,1]$ and $x, y > 0$

$$(ax + (1-a)y)\log_2(ax + (1-a)y) \leq ax\log_2(x) + (1-a)y\log_2(y).$$

By choosing $a = \frac{1}{2}$, $x = 2N$, and $x = 2M$ we get

$$(N+M)\log_2(N+M) \leq N\log_2(2N) + M\log_2(2M).$$

Combination of the two inequalities gives

$$\begin{aligned} N\log_2(N) + M\log_2(M) &\leq (N+M)\log_2(N+M) \\ &\leq N\log_2(2N) + M\log_2(2M). \end{aligned} \tag{14}$$

From (13) and (14) we also conclude that

$$\lim_{\substack{N,M\to\infty \\ N/M\to a>0}} \frac{B(N,M)}{N\log_2(N) + M\log_2(M)} = 1. \tag{15}$$

VII. Data Storage in R-CSNs: Some Comments

In the standard paradigm of digital storage and digital signal processing, information is encoded in sets of binary variables. Unless error correction or other type of coding is used, these variables are considered independent *by default*, e.g., bits stored in non-ECC RAM.

Under the assumption that nanodevices, like R-CSNs, should operate the way traditional digital circuits do, or communicate directly with traditional digital circuits, a major question is raised: how is standard binary representation of data translated into configurations of R-CSNs[8] and *via versa*?

For an $N \times M$ R-CSN the answer is equivalent to finding an injection $\tilde{T} : A \to D_S$, where $A \subset \{0,1\}^L$ for some integer L and $D_S \subset \{0,1\}^{N\times M}$ is the set of *devices*[9] realized by the $N \times M$ R-CSN. Function $\tilde{T}$ should be realizable in hardware with the minimum possible complexity. To this end, sacrificing part of R-CSN's capacity may allow for simpler realization. For example, the domain of $\tilde{T}$ can be restricted and an injection $T : \{0,1\}^L \to D_S$ can be defined instead, where L is the maximum possible integer. Although the derivation of such a function is out of the scope of this work, the following observation is in order.

Consider the case where $N = 2^n$, $M = 2^m$ and the configuration[10] F of the R-CSN is restricted within the set

$$D_S' \equiv \{F \in \{0,1\}^{N\times M} \text{ s.t. } F \text{ has exactly one 1 in every row}\}.$$

Note that D_S' is also the set of devices corresponding to these configurations (since for $F \in D_S'$ it is $[\boldsymbol{F}\boldsymbol{F}^T\boldsymbol{F}]_{>0} = \boldsymbol{F}$, see Lemma 1). The situation is illustrated in Fig. 22 for $n = 2$ and $m = 3$. Moreover, it is $|D_S'| = M^N$.

The advantage of this setup is that the encoding function T is the standard *one-hot encoder*[11] bijection (after reducing its

[8]See Section II-C.

[9]See Definition 3 in Section II-B.

[10]Definition 1, Section II.

[11]It maps the n-bit input vector to its binary value $+1$.

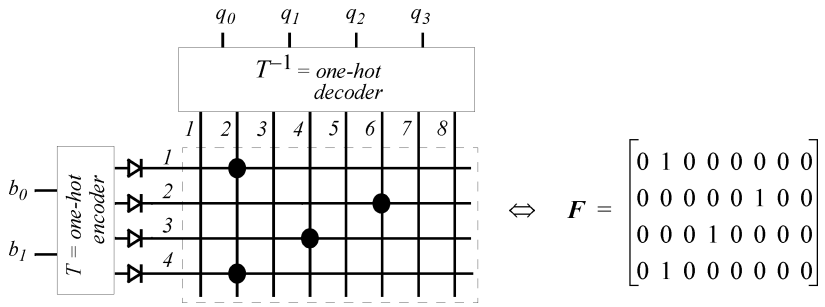


Fig. 22. A paradigm of encoding in a 4×8 R-CSN.

range to its image) from $\{0,1\}^n$ to $\{1,2,3,\ldots,2^n\}$. Similarly, the inverse function T^{-1} is the *one-hot decoder*. In this way we can store

$$\log_2(M^N) = N\log_2(M) = m2^n$$

bits of information.

Although making the nanodevices compatible with the standard digital world is very important, new paradigms of signal processing that do not require immediate data translation may also have their value. R-CSNs of the aforementioned class, for example, realize discrete functions from $\{0,1\}^N$ to $\{0,1\}^M$. By simply cascading the R-CSNs one can form the composition of these functions. Ability to temporarily store the output value and feed it back to the input allows for iterative mappings as well. The set-theoretic inverse of the function is also trivial to generate, etc.

More examples and discussion on encoding and decoding schemes can be found in [2], [22], [23], [25] and [26].

VIII. Concluding Remarks

The information storage capacity of $N \times M$ crossbar switching networks with ohmic (resistive) contact switches (R-CSNs) has been derived explicitly and has been compared to that of crossbar switching networks with semiconductive (diode) switches (D-CSNs). Simple approximate formulas of R-CSNs' capacity have been provided as well. It has been shown that the capacity of square $N \times N$ R-CSNs is asymptotic to $2N\log_2(N)$, for large values of N, and that the capacity of $N \times M$ R-CSNs is asymptotic to $(N+M)\log_2(N+M)$ under some conditions on N, M. Cases where N, M satisfy certain constraints have been considered and the maximization of the capacity has been discussed.

Appendix

Two Lemmas, A1 and A2, are introduced first in order to prove Theorem 3 in Section VI.

Lemma A1: For all positive integers n, m with $n \geq m$ it is

$$S(n,m) \leq \frac{n!}{m!}(e+1)^m. \tag{16}$$

Proof: The Stirling numbers of the second kind, $S(n,m)$, have the following generating function, [29]:

$$(e^z-1)^m = m!\sum_{\nu=m}^{\infty} S(\nu,m)\frac{z^\nu}{\nu!}. \tag{17}$$

Dividing both sides of (17) by z^{n+1} and integrating them on the positively oriented circle C, centered at the origin of the complex plane and having radius R, we get

$$S(n,m) = \frac{n!}{m!}\frac{1}{2\pi i}\oint_C \frac{(e^z-1)^m}{z^{n+1}}dz. \tag{18}$$

From (18) we have

$$\begin{aligned}\left|\frac{1}{2\pi i}\oint_C \frac{(e^z-1)^m}{z^{n+1}}dz\right| &\leq \frac{1}{2\pi}\oint_C \left|\frac{(e^z-1)^m}{z^{n+1}}\right||dz| \\ &\leq \frac{1}{2\pi}\left(\oint_C |dz|\right)\max_{z\in C}\left|\frac{(e^z-1)^m}{z^{n+1}}\right| \\ &\leq \frac{2\pi R}{2\pi}\cdot\frac{(e^R+1)^m}{R^{n+1}} \\ &= \frac{(e^R+1)^m}{R^n}.\end{aligned} \tag{19}$$

Combining (18) and (19) we get

$$S(n,m) \leq \frac{n!}{m!}\frac{(e^R+1)^m}{R^n}$$

which for $R=1$ implies inequality (16). □

Definition A1: Given two positive sequences, $\{\alpha_n\}$ and $\{\beta_n\}$, such that $\alpha_n, \beta_n \neq 1$ for sufficiently large n, we write[12] $\{\alpha_n\} \sim \{\beta_n\}$ if and only if

$$\frac{\ln(\alpha_n)}{\ln(\beta_n)} \to 1, \quad \text{for } n \to \infty.$$

It can be verified directly from Definition A1 that $\sim$ is an *equivalence relation* having the following basic properties.

1. $\alpha_n \sim \beta_n \Rightarrow (\alpha_n)^{\gamma_n} \sim (\beta_n)^{\gamma_n}$ for every sequence $\{\gamma_n\}$. In particular, $\alpha_n \sim \beta_n \Rightarrow \frac{1}{\alpha_n} \sim \frac{1}{\beta_n}$.
2. If $\alpha_n^1 \sim \beta_n^1$ and $\alpha_n^2 \sim \beta_n^2$ then $\alpha_n^1\alpha_n^2 \sim \beta_n^1\beta_n^2$ as long as
$$\left\{\frac{\left|\ln(\alpha_n^1)\right| + \left|\ln(\alpha_n^2)\right|}{\left|\ln(\alpha_n^1)+\ln(\alpha_n^2)\right|}\right\} \quad \text{or} \quad \left\{\frac{\left|\ln(\beta_n^1)\right| + \left|\ln(\beta_n^2)\right|}{\left|\ln(\beta_n^1)+\ln(\beta_n^2)\right|}\right\}$$

[12]With a slight abuse of notation we also write $\alpha_n \sim \beta_n$.

is bounded, e.g., when $\alpha_n^1, \alpha_n^2 > 1$ for sufficiently large n, or when $\beta_n^1, \beta_n^2 > 1$ for sufficiently large n.

3. If $\alpha_n^1 \sim \beta_n^1$ and $\alpha_n^2 \sim \beta_n^2$ then $\frac{\alpha_n^1}{\alpha_n^2} \sim \frac{\beta_n^1}{\beta_n^2}$ as long as
$$\left\{ \frac{\left|\ln(\alpha_n^1)\right| + \left|\ln(\alpha_n^2)\right|}{\left|\ln(\alpha_n^1) - \ln(\alpha_n^2)\right|} \right\} \quad \text{or} \quad \left\{ \frac{\left|\ln(\beta_n^1)\right| + \left|\ln(\beta_n^2)\right|}{\left|\ln(\beta_n^1) - \ln(\beta_n^2)\right|} \right\}$$
is bounded, e.g., when $\frac{\ln(\alpha_n^1)}{\ln(\alpha_n^2)} > c > 1$ for sufficiently large n, or when $\frac{\ln(\beta_n^1)}{\ln(\beta_n^2)} > c > 1$ for sufficiently large n.
4. $(c_n n)^n \sim n^n$ if $0 < \underline{c} < c_n < \overline{c}$ for sufficiently large n.
5. $(n + c_n)^{n+d_n} \sim n^n$ if $\{c_n\}, \{d_n\}$ are bounded sequences.
6. $n! \sim n^n$.
7. $(n + c_n)! \sim n^n$ for every bounded integer sequence $\{c_n\}$.
8. $[an + b_n]! \sim n^{an}$ for every bounded sequence $\{b_n\}$ and $a > 0$.

Stirling's formula, $n! = \sqrt{2\pi}\ n^{n+\frac{1}{2}} e^{-n+\frac{\theta}{12n}}$ for some $0 < \theta_N < 1$, can be used to derive properties 6)–8).

Lemma A2: For every given integer $\rho > 2$, there exists a positive sequence $\{\mu_n^\rho\}$ such that $\mu_n^\rho \sim n^{(2-1/\rho)n}$ and $D(n) > \mu_n^\rho$ for every $n > \rho$.

Proof: Let n, ρ be two integers such that $2 < \rho < n$. Then there exist integers τ, ζ so that $n = \tau\rho + \zeta$ and $0 \le \zeta < \rho$.

The function $(e^z - 1)^{\tau+1}$ of z is analytic and

$$\begin{aligned}(e^z - 1)^{\tau+1} &= \left(z + \frac{z^2}{2!} + \frac{z^3}{3!} + \cdots\right)^{\tau+1} \\ &= \left(z + \frac{z^2}{2!} + \cdots + \frac{z^\rho}{\rho!} + \cdots\right)^{\tau} \\ &\quad \times \left(z + \frac{z^2}{2!} + \cdots + \frac{z^\zeta}{\zeta!} + \cdots\right) \\ &= A_0 + A_1 z + A_2 z^2 + A_3 z^3 + \cdots.\end{aligned}$$

Note that the coefficients of all powers of z in the parentheses above are positive. This, along with $\rho\tau + \zeta = n$ imply that A_n is larger than $\frac{1}{(\rho!)^\tau} \cdot \frac{1}{\zeta!}$. Since $0 \le \zeta < \rho$, we conclude that $A_n > \frac{1}{(\rho!)^{\tau+1}}$. From (18) and the fact that $1 \le \tau + 1 \le n$, we have

$$S(n, \tau+1) = \frac{n!}{(\tau+1)!} \frac{1}{2\pi i} \oint_C \frac{(e^z - 1)^{\tau+1}}{z^{n+1}} dz$$

which gives $S(n, \tau+1) = \frac{n!}{(\tau+1)!} A_n$. Therefore,

$$S(n, \tau+1) > \frac{n!}{(\tau+1)!} \cdot \frac{1}{(\rho!)^{\tau+1}}. \tag{20}$$

From (6), we get that

$$D(n-1) = \sum_{q=1}^{n} S(n, q)^2 (q-1)!$$

and so $D(n-1) > S(n, \tau+1)^2 \tau!$. Using (20) and the fact that $D(n)$ is an increasing function, i.e., $D(n) > D(n-1)$, we get

$$\begin{aligned}D(n) &> S(n, \tau+1)^2 \tau! \\ &> \left(\frac{n!}{(\tau+1)!} \cdot \frac{1}{(\rho!)^{\tau+1}}\right)^2 \tau! \\ &= \frac{(n!)^2}{(\tau+1)(\tau+1)!} \cdot \frac{1}{(\rho!)^{2\tau+2}}.\end{aligned} \tag{21}$$

Equation $n = \tau\rho + \zeta$ implies $\tau = \frac{n}{\rho} - \frac{\zeta}{\rho}$ which along with (21) gives

$$\begin{aligned}D(n) &> \frac{(n!)^2}{\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)!(\rho!)^{\frac{2n}{\rho} - \frac{2\zeta}{\rho} + 2}} \\ &> \frac{(n!)^2}{\left(\frac{n}{\rho} + 1\right)\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)!(\rho!)^{2\frac{n}{\rho} + 2}}.\end{aligned} \tag{22}$$

Recall that ρ is fixed and $0 \le \zeta < \rho$ ($\zeta = \zeta(n)$). Directly from Definition A1 we have the equivalence ρ

$$\left(\frac{n}{\rho} + 1\right)\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)!(\rho!)^{2\frac{n}{\rho}+2} \sim \left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)!.$$

Since $0 \le \zeta/\rho < 1$, Property 8 gives that $\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)! \sim n^{n/\rho}$ and so

$$\left(\frac{n}{\rho} + 1\right)\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)!(\rho!)^{2\frac{n}{\rho}+2} \sim n^{n/\rho}. \tag{23}$$

Also, Property 6 along with Property 1 give

$$(n!)^2 \sim n^{2n}. \tag{24}$$

Now consider the four sequences

$$\begin{aligned}\alpha_n^1 &= (n!)^2 & \beta_n^1 &= n^{2n} \\ \alpha_n^2 &= \left(\frac{n}{\rho} + 1\right)\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)(\rho!)^{2\frac{n}{\rho}+2} & \beta_n^2 &= n^{n/\rho}.\end{aligned}$$

Since

$$\frac{\ln(\beta_n^1)}{\ln(\beta_n^2)} = \frac{2n\ln(n)}{(n/\rho)\ln(n)} = 2\rho > 1$$

and because of (23) and (24) we can apply Property 3 to get $\frac{\alpha_n^1}{\alpha_n^2} \sim \frac{\beta_n^1}{\beta_n^2}$, i.e.,

$$\frac{(n!)^2}{\left(\frac{n}{\rho} + 1\right)\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)!(\rho!)^{2\frac{n}{\rho}+2}} \sim \frac{n^{2n}}{n^{n/\rho}} = n^{n(2-\frac{1}{\rho})}. \tag{25}$$

The lemma is proved by combining (22) and (25) and setting

$$\mu_n^\rho \equiv \frac{(n!)^2}{\left(\frac{n}{\rho} + 1\right)\left(\frac{n}{\rho} - \frac{\zeta}{\rho} + 1\right)!(\rho!)^{2\frac{n}{\rho}+2}}. \tag{26}$$

□

Proof of Theorem 3: Expression (6) and inequality (16) lead to the following steps:

$$\begin{aligned}D(n) &= \sum_{q=0}^{n} S(n+1, q+1)^2 q! \\ &\le \sum_{q=0}^{n} \left(\frac{(n+1)!(e+1)^{q+1}}{(q+1)!}\right)^2 q!\end{aligned}$$

$$= ((n+1)!)^2 \sum_{q=0}^{n} \frac{(e+1)^{2(q+1)}}{(q+1)!} \cdot \frac{1}{q+1}$$
$$< ((n+1)!)^2 \sum_{q=0}^{\infty} \frac{(e+1)^{2q}}{q!}$$
$$= e^{(e+1)^2}((n+1)!)^2.$$

Therefore, $D(n) < u_n$ where $u_n = e^{(e+1)^2}((n+1)!)^2$. Using Properties 1 and 7 we get that

$$u_n \sim n^{2n}. \tag{27}$$

Picking an integer $\rho > 2$ and combining the above results with Lemma A2 we also get that

$$\mu_n^\rho < D(n) < u_n. \tag{28}$$

Taking the logarithms of the three parts in (28) and dividing by $\ln(n^{2n})$ gives

$$\frac{\ln(\mu_n^\rho)}{\ln(n^{2n})} < \frac{\ln D(n)}{\ln(n^{2n})} < \frac{\ln(u_n)}{\ln(n^{2n})}$$

which implies directly that

$$\left(1 - \frac{1}{2\rho}\right) \frac{\ln(\mu_n^\rho)}{\ln(n^{(2-1/\rho)n})} < \frac{\ln D(n)}{\ln(n^{2n})} < \frac{\ln(u_n)}{\ln(n^{2n})}. \tag{29}$$

From Lemma A2, we have $\mu_n^\rho \sim n^{(2-1/\rho)n}$ which commbned with (27) imply that

$$\lim_{n\to\infty} \frac{\ln(\mu_n^\rho)}{\ln(n^{(2-1/\rho)n})} = \lim_{n\to\infty} \frac{\ln(u_n)}{\ln(n^{2n})} = 1. \tag{30}$$

Finally, by combining (29) and (30) we get

$$2 - \frac{1}{\rho} \le \liminf_{n\to\infty} \frac{\ln D(n)}{n\ln(n)} \le \limsup_{n\to\infty} \frac{\ln(D(n)}{n\ln(n)} \le 2$$

which holds for every $\rho > 2$. Taking $\rho \to +\infty$ we conclude that limit $\lim_{n\to\infty} \frac{\ln(D(n))}{n\ln(n)}$ exists and equals 2. □

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