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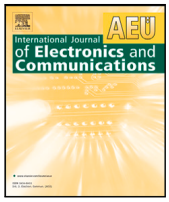

# An ultra-low power fully-programmable analog general purpose type-2 fuzzy inference system

Evangelos Georgakilas, Vassilis Alimisis *, Georgios Gennis, Charis Aletraris, Christos Dimas, Paul P. Sotiriadis

*Department of Electrical and Computer Engineering, National Technical University of Athens, Athens, 15780, Greece*

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ABSTRACT

Neuro-fuzzy systems is a soft computing technique for developing intelligent systems that solve complex real-world problems in a way that closely resembles human reasoning. In this work, a novel ultra-low power pure analog integrated type-2 fuzzy inference system architecture is proposed. The system consists of Gaussian membership function and MIN/MAX operator circuits and a center of gravity defuzzification block. The architecture is easily scalable in the design-level, regarding various system's hyperparameters, resulting in a general-purpose system that can be modified to suit a wide variety of applications. Moreover, the system is fully programmable and electronically tunable even post-fabrication. Finally, a novel fuzzy classifier is implemented in a 90 nm CMOS process using the Cadence IC Suite for the electrical and physical design utilizing the proposed architecture. The classifier is evaluated on the breast cancer Wisconsin (original) dataset and is compared with the equivalent software model and other analog classifiers. Post-layout simulation results confirm the proper operation of the design while demonstrating the optimal combination of ultra-low power and high accuracy performance relative to the other analog classifiers.

## 1. Introduction

Conventional hard computing techniques that rely on rule systems and algorithms based on precision and logic are not equipped to handle uncertainty and imprecision in data, which results in poor performance on input data that contains noise [1]. Soft computing techniques, on the other hand, can handle complex input data that are often incomplete, uncertain, and ambiguous [2–4].

Soft computing is an advanced approach to constructing intelligent systems that can solve intricate and complex real-world problems in a way that closely resembles how humans tackle them [4,5]. By leveraging a blend of complementary computational methods, such as Fuzzy Logic (FL) and Neural Networks (NNs), soft computing leads to the development of adaptable and robust hybrid intelligent systems that incorporate human expertise and knowledge and can manage uncertainty and inaccuracy [6].

Fuzzy set theory was first introduced by Lotfi A. Zadeh in 1965 [7] and is a mathematical logic which, in contrast to classical set theory, allows elements to belong partially to a set. It was established as a method of handling the imprecision, uncertainty and ambiguity found in many real-world problems [8] that are typically described linguistically. Correspondingly, the human perceptive organs capture vague and incomplete information that cannot always be described numerically with precision. Therefore, the human brain usually identifies categories rather than perfectly separated and well-defined sets, with the transition from one category to another being gradual, moving from situations with more to less correlation to the category in question [9,10].

Fuzzy set theory provides the mathematical tools to achieve numerical computations based on such categories which are described linguistically and defined mathematically by membership functions (MFs) as fuzzy sets. "A fuzzy set is a class of objects with a continuum of grades of membership. Such a set is characterized by a membership function that assigns to each object a grade of membership ranging between zero and one" [7]. This value indicates the degree of association of the object with the corresponding fuzzy set. Based on this value, if-then rules are the key components of Fuzzy Inference Systems (FISes) that effectively model human expertise and knowledge. The integration of FISes with NNs and Machine Learning (ML) based optimizations results in a novel discipline of intelligent soft computing systems called Neuro-Fuzzy Computing (NFC) [6].

Motivated by recent works highlighting the capabilities of neuro-fuzzy modeling, we propose a novel ultra-low power pure analog integrated general purpose type-2 FIS. The proposed architecture is

* Corresponding author.
*E-mail address:* alimisisv@gmail.com (V. Alimisis).

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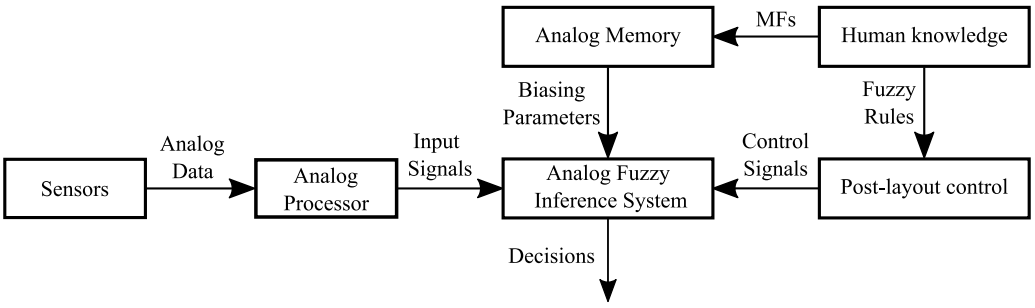



**Fig. 1.** A conceptual system-level design of a fully analog integrated on-chip fuzzy reasoning system.

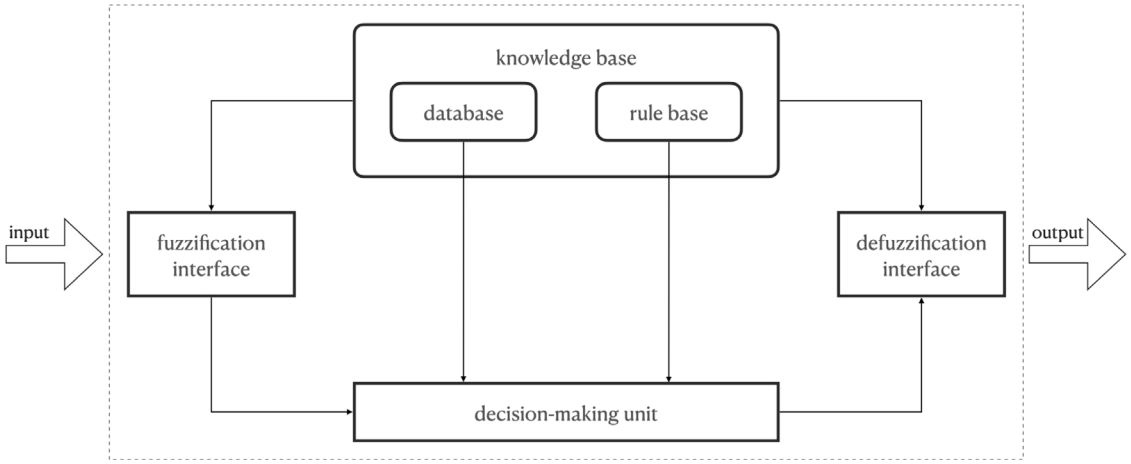



**Fig. 2.** Block diagram illustrating the key components of a FIS. The FIS consists of five functional blocks: the rule base, which defines the fuzzy if-then rules; the database, which contains the MFs of the fuzzy sets used in the rules; the fuzzification interface, which transforms the input data into degrees of compatibility with linguistic terms; the decision-making unit, which performs the fuzzy reasoning process; and the defuzzification interface, which converts fuzzy inferences into crisp output values.

fully electronically tunable and programmable, which allows for the realization of FISes that can be used in different problems. By leveraging the nature and the low-power properties of analog circuits, the proposed architecture is intended for integration within fully analog system-level designs for on-chip fuzzy reasoning, as conceptually illustrated in Fig. 1. The proposed FIS fulfills the role of the Analog Fuzzy Inference System block of Fig. 1. Its implementation and accuracy enables the development of high-performance ultra-low power analog hardware fuzzy systems.

The overall design utilizes three analog building blocks and is implemented as a fuzzy classifier which is evaluated on a breast-cancer classification problem using the open-source breast cancer Wisconsin (original) dataset [11]. The accuracy of the example implementation is confirmed through post-layout simulation results, which are conducted in a TSMC 90 nm CMOS process and simulated using Cadence IC Suite. The accuracy of the proposed FIS is validated by comparing it with an identical software-based implementation and with other analog classifiers. Overall, our work contributes to the development of a versatile and accurate FIS that can be applied to various fuzzy reasoning applications in different domains providing ultra-low power consumption.

The remainder of this paper is structured as follows. Section 2 provides the necessary background information on FISes. Section 3 reviews the prior research on analog hardware implementations of fuzzy systems. Section 4 analyzes the high-level architecture of the proposed FIS and describes the transistor-level implementation of its building blocks. In Section 5, the training and tuning capabilities of the proposed architecture are presented. Section 6 evaluates the accuracy of the proposed general-purpose FIS on a classification problem, using a real-life dataset. In Section 7, we compare our findings to our previous analog integrated classifiers evaluated using the same dataset. Finally, Section 8 concludes the work.

## 2. Fuzzy inference systems

Fuzzy reasoning, also referred to as approximate reasoning or generalized modus ponens (GMP), is the inference mechanism that derives conclusions based on a set of fuzzy if-then rules and known facts [6]. A fuzzy if-then rule assumes the form

if x is A then y is B,

where "x is A" is called the antecedent part and "y is B" is called the consequent part of the rule. Based on modus ponens logic, the truth of the consequent proposition is inferred from the truth of the antecedent proposition. The concept is illustrated as follows:

| | |
|---|---|
| premise 1 (fact): | x is $A'$, |
| premise 2 (fuzzy rule): | if x is A, then y is B, |
| consequence (conclusion): | y is $B'$, |

where typically A, A′, B and B′ are fuzzy sets of appropriate universes.

The diagram in Fig. 2 illustrates the constituent components of a FIS, as well as their interaction [12,13]. The input vector of the system can take the form of either fuzzy variables represented by fuzzy sets, or precise numerical values referred to as crisp inputs. In contrast, the output of the system is characterized by one or more well-defined numerical values, depending on the dimensions of the output vector.

As depicted in Fig. 2, a FIS comprises five distinct functional blocks. The rule base encompasses a set of fuzzy if-then rules, while the database defines the MFs of the fuzzy sets employed in the fuzzy rules. These two components represent the area where human knowledge is encoded within the system, and are commonly referred to as the knowledge base. In addition, the fuzzification interface serves to transform the input data into degrees of compatibility with linguistic terms that are described by fuzzy sets present in the system database. The

decision-making unit is responsible for carrying out the process of fuzzy reasoning, which is based on the input data, the corresponding rule base, and the selected synthesis operators. Finally, the defuzzification interface is responsible for converting the fuzzy inferences generated by the decision unit into inferences with a well-defined form, i.e. crisp output values.

Employing a variety of mathematical operators on fuzzy sets and different approaches in the consequent part of the rules, several types of FISes are constructed. In a type-2 FIS (Mamdani [14]) the overall fuzzy output is produced by applying a fuzzy union operator to the qualified fuzzy outputs of each fuzzy rule. The final crisp output of the system is derived by using a defuzzification operator on the overall fuzzy output, such as center of gravity (COG), bisector of area (BOA), mean of max (MOM), etc. Other realizations of FISes are type-1 (Tsukamoto [15]) that employ monotonic output MFs and type-3 (Takagi and Sugeno [16]) that utilize Takagi and Sugeno's fuzzy if then rules, where the output of each rule is a linear combination of the input variables plus a constant term. In that case, the overall output of the system is obtained by the weighted average of the crisp outputs of the rules, where the weighting factor for each rule corresponds to its firing strength.

Neuro-fuzzy and fuzzy systems are well-suited for a wide range of applications including control systems, robotics, image processing, medical diagnosis and financial analysis due to their effectiveness in handling ambiguous and imprecise data commonly encountered in many real-world applications [17]. With the development of technology and the prevalence of ultra-low power applications, such as embedded real-time systems, IoT and wearables, the software implementation of fuzzy systems fails short in meeting the criteria of speed and power consumption. As a result, numerous hardware solutions have been proposed. These hardware implementations consist of digital alternatives for higher accuracy and analog alternatives for improved speed performance and lower power demand [18,19].

Digital hardware implementations have been developed using Field Programmable Gate Array (FPGA) technology, which provides high integration density and power efficiency through parallelism and results to high-performance fuzzy reasoning systems [20–24]. However, the use of FPGA technology may not be sufficient for ultra-low power applications, and hence, analog circuits have been explored to overcome these limitations [25]. Analog circuits, operating in the sub-threshold region [26], have the potential to achieve lower power consumption compared to their digital counterparts. Another critical benefit of analog implementations is that they have a natural connection with input sensors and actuators eliminating the need of analog-to-digital (ADC) or digital-to-analog (DAC) converters. Additionally, mixed-mode Application-Specific Integrated Circuits (ASICs), which leverage both digital and analog technologies, have become increasingly popular. These mixed-mode ASICs can offer the benefits of both digital and analog technologies, and are proven to be suitable for a variety of applications [27–29]. Finally, memristive-based approaches leverage the unique properties of memristors, including their inherent resistance modulation capabilities, thereby yielding high-performance hardware FISes [30,31].

## 3. Related work

The literature on complete pure analog FISes is relatively scarce compared to digital ones. Although some literature presents innovative circuits for specific fuzzy building blocks such as MFs [32–35], MIN/MAX networks [36–44], multipliers [45–47], dividers [48], inference engines [49,50], and defuzzification techniques [51–54], only few contributions are available on complete systems, most of which pertain to controllers [55–60]. However, most of these studies focus on the implementation of fuzzy reasoning with analog computing and only few of them are dedicated to improving system's operating specifications and adaptability [25,60–62].

While many researchers validate that type-2 FISes outperform corresponding type-1, being more robust to systems uncertainties [25,60], type-2 FISes have also the capability to represent equivalent type-1 systems with smaller rule bases [63]. Leveraging this attribute to simplify computations and speed up processing, Khosla et al. in [60] and Azeem et al. in [61] propose an interval type-2 FIS that is realized by combining two type-1 FISes. This is accomplished in a typical architecture of a type-2 fuzzy model by adding a type-reducer block in between fuzzy inference engine and the defuzzifier. The type-reducer converts the type-2 fuzzy set outputs of the fuzzy inference engine to type-1 fuzzy sets and then the defuzzifier produces the crisp output from them. The use of input control signals in both implementations provides tunability and hence adaptability to the systems. In both cases input MFs are fully programmable, whereas [61] allows for control of the footprint of uncertainty (FOU) and [60] provides programmability to the rule base through control pins on IC of the proposed controller chip.

In [25] de Souza et al. identify the need of investing in generating analog FISes focused on the advantages that can bring in contrast to their digital counterparts, such as speed and power dissipation. Highlighting the drawback of having several copies of currents to represent the membership degrees in a FIS inference block, which increases area and power consumption, they propose the use of high-gain differential amplifiers operating with low bias currents, as comparators, creating digital signals that indicate the smallest/largest current to implement the MIN/MAX operator. This approach results in 4.4 times less power consumption compared to a typical analog FIS implementation, resulting in a low-power interval type-2 fuzzy inference engine.

## 4. Proposed architecture

In this Section the development of a programmable ultra-low power pure analog general-purpose type-2 FIS with high-accuracy fuzzy reasoning well-matched to the equivalent software-based model will be discussed.

### 4.1. Fuzzy modeling

It has been shown that the use of scaled Gaussian MFs to describe the terms of linguistic variables in both the antecedent and the consequent part of a fuzzy rule is a particularly beneficial feature for a FIS [6,12,64]. A scaled Gaussian MF is specified by three parameters A, c and $\sigma$ as follows:

$$\text{scaled gaussian}(x; A, c, \sigma) = A \cdot e^{-\frac{(x-c)^2}{2\sigma^2}}, \tag{1}$$

where A represents the amplitude of the Gaussian distribution (always equal to 1 in FL) while c and $\sigma$ correspond to its mean value and standard deviation, respectively.

The smoothness and symmetry of Gaussian MFs centered around their central peak that represents the most typical value for the linguistic term they describe, make them intuitive and easy to understand and interpret from a human perspective. In addition to their smoothness, Gaussian MFs are also continuous and differentiable over the entire range of inputs, which ensures that if there is enough/sufficient overlap in the antecedent MFs the output of the fuzzy system will also be smooth and continuous [6]. Additional important positive features gained by using Gaussian functions in the antecedent MFs are their functional equivalence with radial basis function networks (RBFNs) [65] and thus compatibility with ML techniques for system optimization [12].

Moreover, it has been proven that a FIS with Gaussian MFs to describe the fuzzy sets of the consequent parts of the fuzzy rules can satisfy the four criteria of the Stone–Weierstrass theorem and thus has the property of unlimited approximation power for matching any nonlinear function arbitrarily well on a compact set [6,12]. In particular, in that case it is proven that in any compact metric space $\mathcal{X}$ of $\mathcal{N}$

dimensions, for any $\epsilon > 0$ and any continuous, real-valued function g(x), there exists at least one FIS(x) such that: $\|g(x) - FIS(x)\| < \epsilon, \forall x \in \mathcal{X}$. [6,12]. This property provides significant value to the system since it has the ability to approximate any non-linear but continuous relationship between its input and output data.

After selecting the appropriate family of MFs to model the fuzzy sets, a type-2 FIS requires five operators; the AND, OR, implication, aggregation and defuzzification operators. T-norm and T-conorm operators, which are commonly used in a FIS as the AND and OR operators, respectively, can be implemented in hardware using a MIN/MAX circuit. The use of the MIN as the AND and the MAX as the OR operator is a well-established practise [6] that provides a conservative and a liberal approach, respectively, for estimating the firing strength of a rule. However, both of these operators are sensitive to outliers. In particular, a small degree of membership in one fuzzy set, in the case of the MIN operator, or a high degree of membership, in the case of the MAX operator, can significantly influence the overall firing strength of the rule [66]. To mitigate the impact of outliers on the fuzzy reasoning process, non-conventional FL operators [67], as well as the incorporation of outlier detection techniques, have been explored [66,68]. However, implementing these approaches in hardware poses challenges, as they often require large area and high power consumption, making them less efficient.

In contrast, a MIN/MAX circuit that combines both operators in one circuit offers area efficiency and the ability to use the same block for both AND-ed and OR-ed antecedents in different rules. Although the presence of outliers is acknowledged, the primary focus in this work was on the improvements and control capabilities enabled by the MIN/MAX circuit in the proposed architecture, rather than specifically addressing outlier handling.

The most popular method of defuzzification is that of COG. If $\mu_A(z)$ is the overall output function of a FIS on the universe of discourse $Z$, then the COG is defined as follows:

$$z_{COG} = \frac{\int_Z \mu_A(z) \cdot z\, dz}{\int_Z \mu_A(z)\, dz} \tag{2}$$

The COG method, according to Eq. (2), calculates the center of mass or centroid of the area under the function of the fuzzy set A, which is defined as the point at which the mass of the fuzzy set is uniformly distributed [6]. Its main advantage is its scale-invariability, i.e. it is not affected by the choice of measurement units used for the different variables of the system, and that it is continuous with respect to the membership function that it defuzzifies [69].

A specific advantageous feature of the proposed architecture is that it uses product for the implication operator and point-wise summation for the aggregate operator, the so-called sum–product composition [6,70]. Under sum–product composition, the final crisp output of a type-2 FIS via COG defuzzification is equal to the weighted average of the centroids of consequent MFs, where the weighting factor is equal to the firing strength of the corresponding fuzzy rule multiplied by the area of the consequent MF.

For example, in the case of a FIS with two fuzzy rules with two antecedents and one consequent, fuzzy reasoning is conceptually illustrated as follows:

| | |
|---|---|
| premise 1 (fact): | x is $A'$ and y is $B'$, |
| premise 2 (fuzzy rule 1): | IF x is $A_1$ AND y is $B_1$, THEN z is $C_1$, |
| premise 3 (fuzzy rule 2): | IF x is $A_2$ AND y is $B_2$, THEN z is $C_2$, |
| consequence (conclusion): | z is $C'$. |

By using the sum–product composition the MF of the resulting fuzzy set C′ is given by:

$$\mu_{C'}(z) = \mu_{C_1'}(z) + \mu_{C_2'}(z) = \omega_1 \cdot \mu_{C_1}(z) + \omega_2 \cdot \mu_{C_2}(z), \tag{3}$$

where $\mu_{C_i}(z)$ is the MF of the consequent fuzzy set $C_i$ defined in the universe of discourse $Z$ and $\omega_i$ is the firing strength of the fuzzy rule i, for $i = 1, 2$.

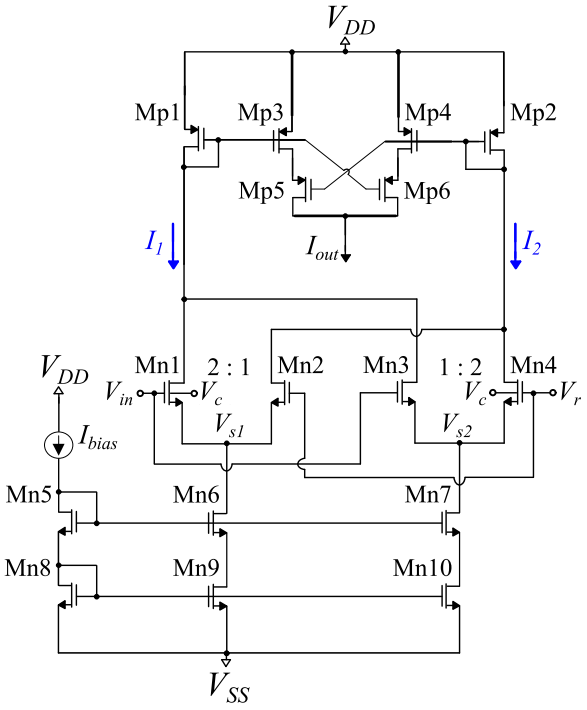



**Fig. 3.** FMF circuit (fuzzification block). The voltage $V_{in}$ corresponds to the system's input. The parameter voltages $V_r$ and $V_c$, and the bias current $I_{bias}$ control the mean value, the variance and the amplitude of the Gaussian MF. $VDD = -VSS = 0.3$ V.

In this case, according to Eq. (2), the COG of the overall output MF $\mu_{C'}$ of the system is given by:

$$z_{COG} = \frac{\int_Z \mu_{C'}(z) \cdot z\, dz}{\int_Z \mu_{C'}(z)\, dz}$$

$$z_{COG} = \frac{\omega_1 a_1 z_1 + \omega_2 a_2 z_2}{\omega_1 a_1 + \omega_2 a_2}, \tag{4}$$

where $a_i = \int_Z \mu_{C_i}(z)\, dz$ is the area of the region occupied by the MF $\mu_{C_i}(z)$, and $z_i = \frac{\int_Z \mu_{C_i}(z) \cdot z\, dz}{\int_Z \mu_{C_i}(z)\, dz}$ is the centroid of the MF $\mu_{C_i}(z)$ of the fuzzy set $C_i$.

In the proposed architecture, the MFs of the fuzzy sets in the consequent part of the rules are Gaussian MFs. According to Eq. (1), the terms $a_i$ and $z_i$ of Eq. (4) are equal to:

$$\text{centroid of } \mu_{C_i} : z_i = \frac{\int_Z \mu_{C_i}(z) \cdot z\, dz}{\int_Z \mu_{C_i}(z)\, dz} = \frac{\int_Z e^{-\frac{(z-c_i)^2}{2\sigma_i^2}} \cdot z\, dz}{\int_Z e^{-\frac{(z-c_i)^2}{2\sigma_i^2}}\, dz} = c_i, \tag{5}$$

$$\text{area of } \mu_{C_i} : a_i = \int_Z \mu_{C_i}(z)\, dz = \int_Z A_i \cdot e^{-\frac{(z-c_i)^2}{2\sigma_i^2}}\, dz$$

$$= \int_Z A_i \cdot e^{-\frac{z^2}{2\sigma_i^2}}\, dz = A_i \cdot \sigma_i \cdot \sqrt{2\pi}, \tag{6}$$

that is, the centroid $z_i$ is equal to the mean value $c_i$ of the Gaussian distribution and the area $a_i$ is equal to the product of the amplitude of the Gaussian distribution times its standard deviation times a constant number $\sqrt{2\pi}$.

Applying the Eqs. (6) and (5) to (4), it follows that the COG of $\mu_{C'}$ is now given by:

$$z_{COG} = \frac{\omega_1 A_1 \sigma_1 c_1 + \omega_2 A_2 \sigma_2 c_2}{\omega_1 A_1 \sigma_1 + \omega_2 A_2 \sigma_2} \tag{7}$$

Typically, all MFs in a FIS have by definition the same amplitude equal to unity, i.e. $A_1 = A_2 = 1$. Moreover, in the special case where the Gaussian MFs that describe the consequent parts of the rules have

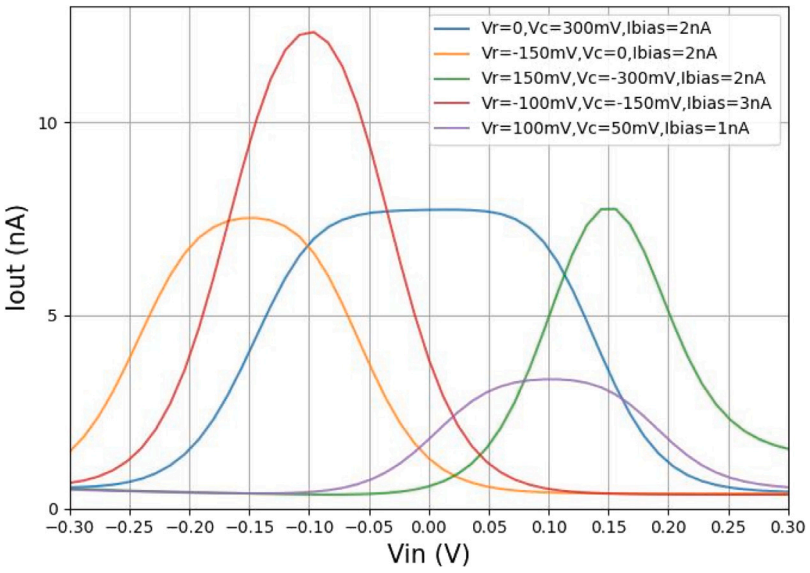



**Fig. 4.** Output current $I_{FMF}$ of the FMF circuit for various values of $V_r$, $V_c$ and $I_{bias}$. With the chosen ratio of the transistors $M_{n8} - M_{n9}, M_{n10}$ the output current should have had a height of 5 times $I_{bias}$. The discrepancy noted there does not affect the operation of the system but should be taken into account by the designer.

all the same standard deviation, i.e., $\sigma_1 = \sigma_2 = \sigma$, then Eq. (7) is further simplified to the following form:

$$z_{COG} = \frac{\omega_1 c_1 + \omega_2 c_2}{\omega_1 + \omega_2} = \frac{\sum_{i=1}^{2} \omega_i \cdot c_i}{\sum_{i=1}^{2} \omega_i}, \tag{8}$$

Accordingly, for the proposed FIS of m rules with Gaussian consequent MFs of the same amplitude and standard deviation, i.e. $A_1 = A_2 = \cdots = A_i$ and $\sigma_1 = \sigma_2 = \cdots = \sigma_i$ for every $i, 1 \leq i \leq m$, the COG of the overall output MF is given by:

$$z_{COG} = \frac{\sum_{i=1}^{m} \omega_i \cdot A_i \cdot sigma_i \cdot c_i}{\sum_{i=1}^{m} \omega_i \cdot A_i \cdot sigma_i}, \tag{9}$$

$$z_{COG} = \frac{\sum_{i=1}^{m} \omega_i \cdot c_i}{\sum_{i=1}^{m} \omega_i}, \tag{10}$$

From the form of Eq. (10) we observe that the output of the proposed type-2 Mamdani FIS is exactly equivalent to the output of a type-3 zero-order Takagi–Sugeno FIS [6]. Therefore, with the proposed FIS architecture we exploit the features of both types of fuzzy systems.

The upcoming subsections provide a comprehensive explanation of the analog building blocks used in the proposed architecture. Specifically, the Gaussian MFs are generated using a modified Bump circuit (Section 4.2). The fuzzy inference is implemented using a high-precision current-mode MIN/MAX circuit (Section 4.3), while the defuzzification block of the system is based on a classic topology of a follower-aggregation circuit [8] with wide-range operational transconductance amplifiers (OTAs) (Section 4.4). To minimize power consumption, all transistors in the system operate in the sub-threshold region and the power supply rails are set to $VDD = -VSS = 0.3$ V across the entire system. All circuits are implemented in a 90 nm CMOS technology that offers small saturation margin and diminished effective voltage ($V_{eff}$), with the employment of long transistors that address the challenges posed by noise and mismatches during the layout phase. The Cadence IC Suite is used for their electrical and physical design.

### 4.2. Fuzzification block

The fuzzification block serves as the interface between the FIS and the external environment, usually sensors that typically provide signals in voltage mode. Additionally, this block interacts with the fuzzy inference block (FI), i.e. the MIN/MAX operators. Although voltage-mode circuits are capable of performing the MIN/MAX operations, a current-mode circuit facilitates the operations in the subsequent blocks due to the simplicity of current additions achieved by joining nodes. To minimize the need for current to voltage (AV) and voltage to current (VA) converters, which occupy space and consume power, each of the circuits in the fuzzification block should receive a voltage input and produce an output current. In particular, the voltage input is the crisp input of the FIS and the output current is the degree of compatibility between the input and the fuzzy set that the circuit describes.

A plethora of research teams have dedicated their efforts towards designing improved Gaussian function circuits and integrating them into diverse domains [71]. The Fuzzy Membership Function (FMF) circuit used to generate antecedent Gaussian MFs of increased quality in the proposed architecture is a modified Bump circuit [72,73] that is illustrated in Fig. 3.

With reference to [74], a cross-coupled differential pair (transistors $M_{n1} - M_{n4}$) with ratio 2 and a symmetric current correlator (transistors $M_{p1} - M_{p6}$) generate high-precision symmetric Gaussian curves for voltage inputs around the mean value even for very small bias currents. The cascode current mirror composing of transistors $M_{n5} - M_{n10}$ is used to enhance current mirroring. The ratio of the transistors $M_{n8} - M_{n9}, M_{n10}$ is set to 5 as a technique to reduce the current in the left most rail and hence the power dissipation of the circuit. All transistors' dimensions are summarized in Table 6.

The generated Gaussian curve is completely defined by the selection of the parameters $V_r$, $V_c$ and $I_{bias}$. The mean value of the Gaussian curve is established by the voltage $V_r$. Moreover, the variance of the curve is controlled by the voltage $V_c$ through a non-linear, monotonically increasing, bounded function. Finally, the height of the curve is proportional to the bias current $I_{bias}$ multiplied by a constant value, which depends on the ratio of the input nMOS mirror to the output pMOS mirror and the size of the transistors.

The Gaussian circuit's output current $I_{out}$ is presented in Fig. 4 for various values of $V_r$, $V_c$ and $I_{bias}$ as well as the system input $Vin$.

In order to describe the high-level architecture of the Fuzzification block of the proposed FIS, let us assume that $V_{in1}$ is the system's input that corresponds to the linguistic variable A which in turn is described by n linguistic terms $A_1$ to $A_n$. Each of these linguistic terms is a fuzzy set described by a Gaussian MF which in system-level is defined by a corresponding FMF circuit and its biasing parameters. The high-level architecture of the fuzzification block of the proposed FIS is shown in Fig. 5.

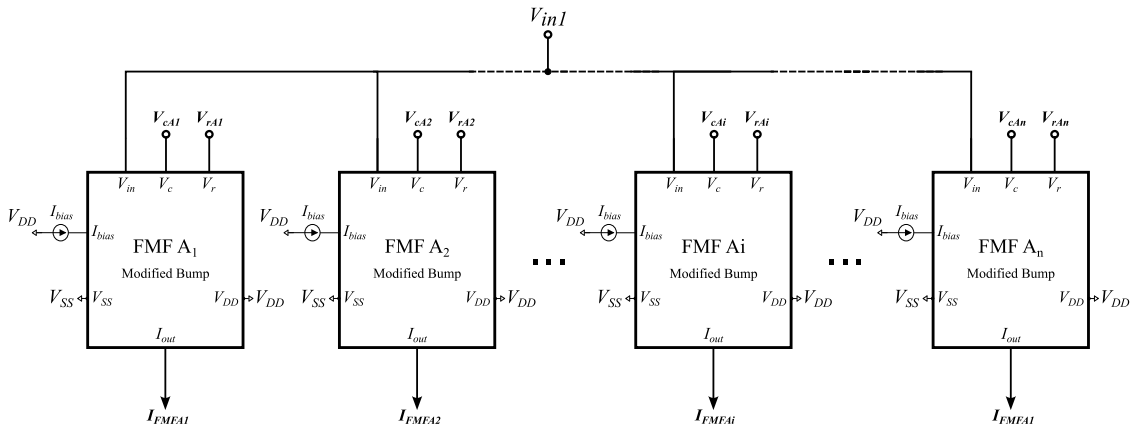



**Fig. 5.** High-level architecture of the fuzzification block of the proposed FIS. Each $FMF_{Ai}$ circuit represents the linguistic term $A_i$ of the linguistic variable A. The bias current $I_{bias}$ is a constant current (in our case $I_{bias}$ = 3 nA) for every FMF circuit while voltages $V_r$ and $V_c$ vary from −300 mV to + 300 mV. The output current $I_{FMF}$ of each FMF circuit denotes the degree of compatibility between the input $V_{in1}$ and the fuzzy set it describes. $VDD = -VSS = 0.3$ V.

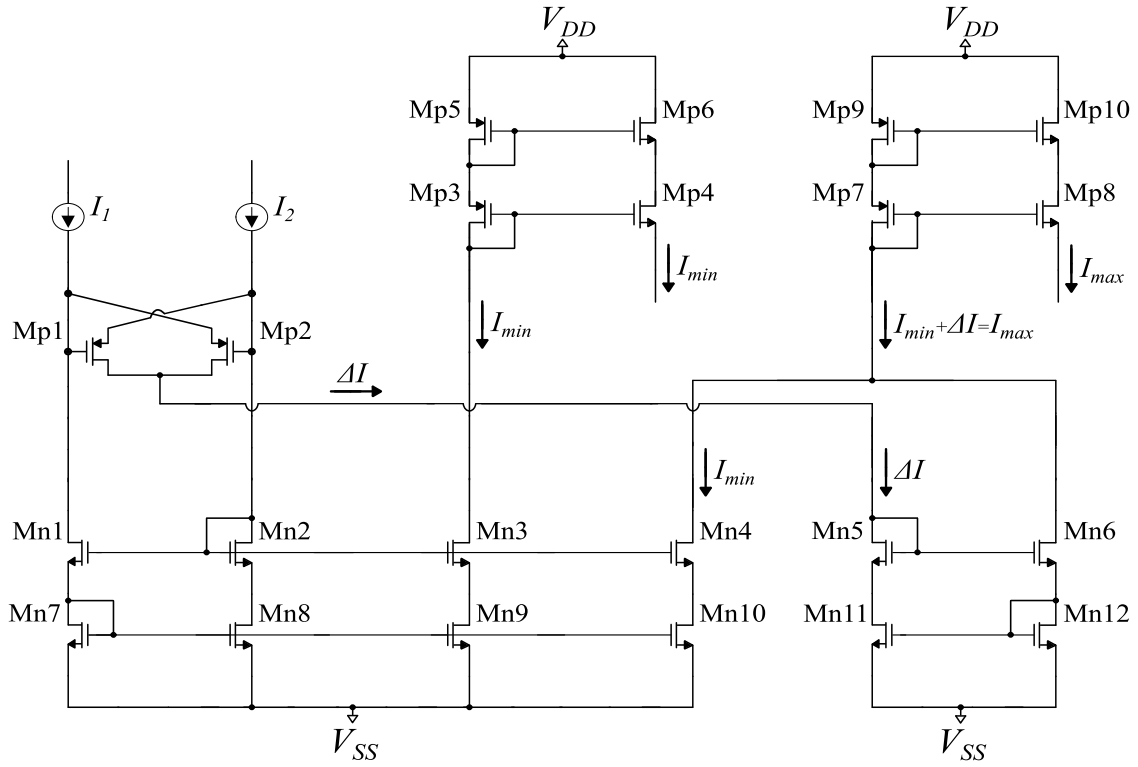



**Fig. 6.** FI circuit (fuzzy inference block). The currents $I_1$ and $I_2$ are the circuit's input currents produced by corresponding FMF circuits. $VDD = -VSS = 0.3$ V.

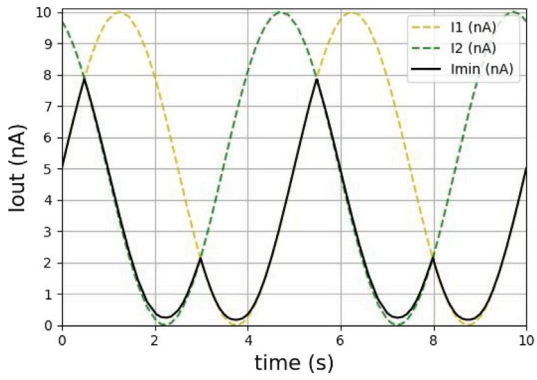
### 4.3. Fuzzy inference block

The MIN/MAX operators have gained widespread use in a multitude of nonlinear signal processing tasks, prompting significant interest from the scientific community. A variety of approaches have been proposed in literature, including LTA/WTA circuits and comparators [75,76]. While [75] recommends using multi-input circuits to implement MIN or MAX circuits, the proposed design utilizes a two-input circuit. For rules with multiple antecedents (more than two), cascading unit cells is required. While this approach seems not particularly area or power efficient, it does enable complex fuzzy reasoning and fuzzy rules with combined AND-ed and OR-ed antecedents. Moreover, the circuit used in this design performs both operations simultaneously, negating the disadvantage of increased area occupancy and power consumption associated with using separate blocks for MIN and MAX operations.

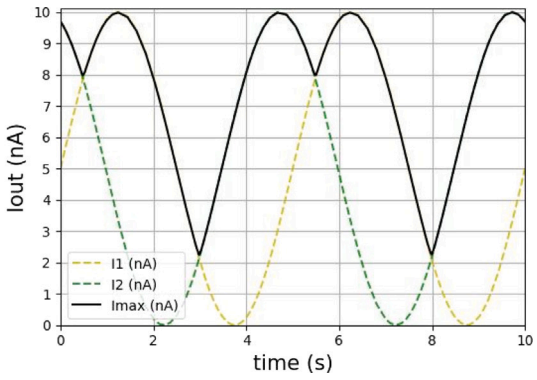
The FI circuit used to generate the firing strength of the rules in the proposed FIS is based on the current-mode MIN/MAX circuit of [77] and is illustrated in Fig. 6.

Since the input currents of the circuit are to be in the range of few nA, large components are used to enhance circuit's accuracy. Increased length results also in increased output and decreased input impedance. Moreover, reduced width increases the accuracy in mirroring small currents. Details of the dimensions of all transistors used in the FI circuit are provided in Table 1.

Considering that $M_{n7}$ and $M_{n11}$ share the same dimensions, a power-saving technique for the circuit involves reducing the currents that flow through the rails of $M_{n9}$, $M_{n3}$, $M_{p3}$, $M_{p5}$ and $M_{n10}$, $M_{n4}$, $M_{n12}$, $M_{n6}$, $M_{p7}$, $M_{p9}$. This reduction can be achieved by setting the width ratio of $M_{n9}$, $M_{n10}$, and $M_{n12}$ relative to $M_{n7}$, and setting the reverse width ratio to $M_{p5}$, $M_{p6}$, and $M_{p9}$, $M_{p10}$, respectively. In this scenario, the absolute difference between the input currents and the minimum




(a) Minimum output current $I_{FIMIN}$




(b) Maximum output current $I_{FIMAX}$

**Fig. 7.** Output currents $I_{FIMIN}$ and $I_{FIMAX}$ of the FI circuit for two input sinusoidal current waveforms with 10 nA amplitude and a phase shift of 110 deg.

**Table 1**
Dimensions of MOS transistors in the FI circuit (Fig. 6).

| Transistors | W/L (μm/μm) |
|---|---|
| $M_{p1}$, $M_{p2}$ | 0.2/1.6 |
| $M_{n1} - M_{n12}$ | 0.2/1.6 |
| $M_{p3} - M_{p10}$ | 0.2/1.6 |

**Table 2**
Dimensions of MOS transistors in the OTA (Fig. 10).

| Differential Pair | W/L (μm/μm) | Current mirrors | W/L (μm/μm) |
|---|---|---|---|
| $M_{n1}$, $M_{n4}$ | 1.4/16.0 | $M_{p1}$, $M_{p3}$ | 1.8/16.0 |
| $M_{n2}$, $M_{n3}$ | 0.2/16.0 | $M_{p2}$, $M_{p4}$ | 0.8/16.0 |
| $M_{nb1}$ | 0.2/16.0 | $M_{n5}$, $M_{n6}$ | 0.2/16.0 |
| $M_{nb2}$, $M_{nb3}$ | 0.2/16.0 | – | – |

one will be divided by the nMOS transistor ratio and then multiplied again by the same value (pMOS transistor ratio) in the output rails. This results in two rails with lower currents and, consequently, reduced power consumption. However, in our case the circuit's operation region already has very small currents in the order of 5 nA, and even a slight mismatch could cause problems.

In Fig. 7 the transient results of the FI circuit of the proposed architecture are depicted with two input sinusoidal current waveforms with 10 nA amplitude and a phase shift of 110 deg.

In the proposed FIS each FI block implements a particular fuzzy rule utilizing a cascade of FI circuits to combine multiple antecedents. Each FI circuit incorporates a fuzzy rule consisting of two antecedents. The FI's output current $I_{FI}$ is selectively determined as either the MIN or the MAX current ($I_{FIMIN}$ or $I_{FIMAX}$), resulting in ANDed or ORed antecedents, respectively. The implementation of a fuzzy rule with four antecedents in the high-level architecture of the FI block of the proposed FIS is shown in Fig. 8.

### 4.4. Defuzzification block

In accordance with Eq. (10), and taking into consideration that the firing strength $\omega_i$ of $Rule_i$ is equal to the output current of the $i$th FI block denoted as $I_{FIRulei}$, and that the centroid of the consequent Gaussian MF of the same rule is represented by the voltage setting $V_{rRulei}$, the COG of the overall output MF of the proposed FIS with m rules is given by the following expression:

$$COG = \frac{\sum_{i=1}^{m} I_{FIRulei} \cdot V_{rRulei}}{\sum_{i=1}^{m} I_{FIRulei}}, \tag{11}$$

Among the various approaches of analog COG defuzzification blocks reported in literature [75,78,79], the proposed architecture utilizes a voltage follower-aggregation technique proposed by Carver Mead in [8] that is illustrated in Fig. 9.

A total of m Operational Transconductance Amplifiers (OTAs), $OTA_1$ to $OTA_m$, are employed to aggregate the weighted inputs $V_{rRule1}$ to $V_{rRulem}$, and calculate the weighted average of Eq. (11) for each dimension of the system's output vector. Each OTA represents the consequent Gaussian MF of a rule. The operation of the structure is based on the feedback loop depicted in Fig. 9 and the Kirchhoff's current law to achieve:

$$\sum_{i=1}^{m} G_{mi} \cdot (V_{rRulei} - V_{out}) = 0 \tag{12}$$

The transconductance $G_{mi}$ of the $OTA_i$ operating in its linear range is given by:

$$G_{mi} = \frac{I_{FIRulei}}{2kT/(q\kappa)}, \tag{13}$$

where $I_{FIRulei}$ is the bias current of the $OTA_i$, k is the Boltzmann's constant ($k \approx 1.38 \cdot 10^{-23}$ J/K), $T$ is the absolute temperature in Kelvin, q is the elementary charge ($q \approx 1.6 \cdot 10^{-19}$ C) and $\kappa$ is the subthreshold slope factor of the OTA's input transistors.

Supposing that there are no mismatches among the OTA cells and they always operate in their linear region, evaluating Eqs. (13) to (12), results the expected weighted average, Eq. (11), as the voltage output of the follower-aggregation structure.

Since the defuzzification block serves as the interface of the proposed system to the external environment, having a voltage output is advantageous. Moreover, the proposed structure is convenient with the proposed FIS since the aggregate and the defuzzification operators are utilized with the need of only an extra Vr voltage setting for each of the consequent MFs, since the bias currents of the OTAs are generated by the FI block. Thus, VA and AV converters and large area multiplier/divider circuits needed otherwise are avoided.

To ensure the accuracy of the block a wide-range high open loop gain OTA is designed and is illustrated in Fig. 10.

The cross-coupled differential pair (transistors $M_{n1} - M_{n4}$) with ratio 7 and the current mirrors ($M_{p2}$, $M_{p4}$), ($M_{p1}$, $M_{p3}$) and ($M_{n5}$, $M_{n6}$) that eliminate simple OTA's $V_{min}$ problem [8], increase the linear operating region of the OTA. Long transistors $M_{p3}$ and $M_{n6}$ result in low drain conductance and provide the circuit with a high open loop voltage gain and output impedance. This, in turn, results in a more precise calculation of the COG. All transistors' dimensions are listed in Table 2.

The selected topology and transistor sizing result in OTAs with a clear linear region of at least 220 mV differential input range. Moreover, their output current is independent from variations in their output voltage in a range of at least 400 mV. These specifications are proven

$$\textbf{\textit{Rule}}_{\textbf{\textit{1}}}\textit{ : If } (V_{in1} \textit{ is } A_1 \textbf{ OR } V_{in2} \textit{ is } B_1) \textbf{ AND } (V_{in3} \textit{ is } C_1 \textbf{ AND } V_{in4} \textit{ is } D_1) \textit{ then ...}$$

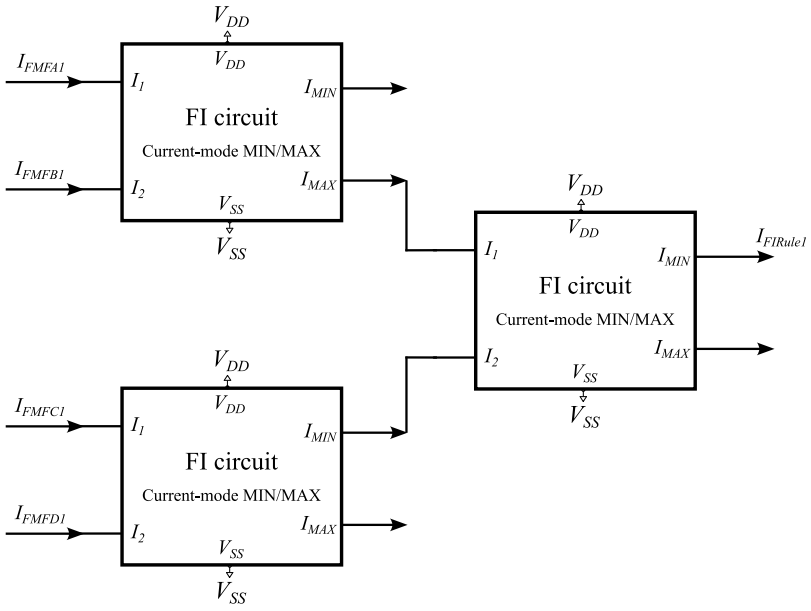



**Fig. 8.** High-level architecture of the FI block of the proposed FIS. Currents $I_{FMFA1}$, $I_{FMFB1}$, $I_{FMFC1}$ and $I_{FMFD1}$ are generated by corresponding FMF circuits $FMF_{A1}$, $FMF_{B1}$, $FMF_{C1}$ and $FMF_{D1}$ and indicate the membership grade between the inputs of the system and the fuzzy sets A1, B1, C1 and D1. The MIN or MAX current output of each FI circuit controls whether the antecedent parts are ANDed or ORed, respectively. The output current of the entire FI block corresponds to the firing strength of the fuzzy rule it implements. In the above case, $I_{FIRule1}$ denotes the firing strength $\omega_1$ of $Rule_1$ of the FIS. In the proposed architecture for a rule with n antecedents a total of $(n + (n \ mod \ 2) - 1)$ FI circuits is needed to implement the corresponding FI block. $VDD = -VSS = 0.3$ V.

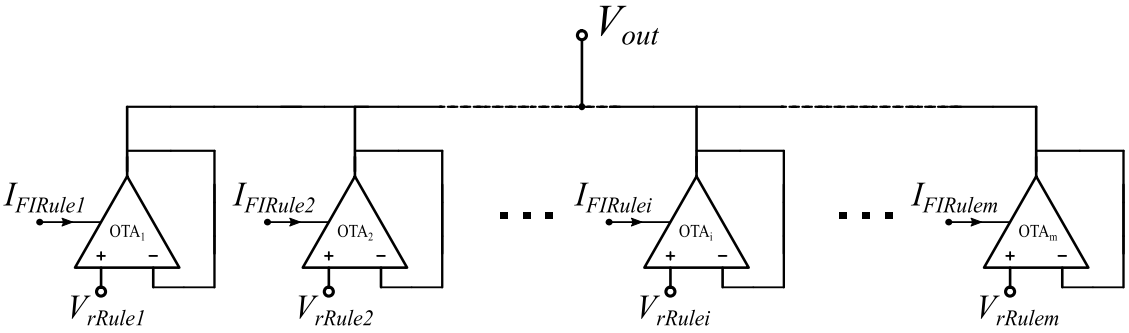



**Fig. 9.** High-level architecture of the defuzzification block of the proposed FIS. The follower aggregation structure composed by $OTA_1$ to $OTA_m$ produces the COG in the voltage output $V_{out}$. Each OTA represents the consequent Gaussian MF of a rule, with the voltage setting in its positive input corresponding to the centroid of the exact MF. The bias current is the firing strength of the fuzzy rule that concludes to this Gaussian MF and is produced by a corresponding FI block.

**Table 3**
Performance results of the OTA evaluated at extreme bias current values.

| Bias current (nA) | Linear region $\Delta V$ (mV) | Independent region Vout (mV) | DC gain (dB) | Rout (MΩ) | f-3dB (Hz) | Input offset voltage (mV) |
|---|---|---|---|---|---|---|
| 1 | [−110, 110] | [−250, 250] | 27.16 | 1615 | 100 | 0.58 |
| 10 | [−140, 140] | [−200, 200] | 31.07 | 408 | 390 | 1.72 |

enough to produce an accurate COG calculation well-matched to the equivalent software model. However, achieving them comes at the cost of circuit speed and frequency response. The performance of the OTA was evaluated at extreme bias current values (1 nA and 10 nA), and the results are presented in Table 3.

The output current $I_{out}$ and the transconductance $G_m$ of the OTA as functions of the differential input voltage $\Delta V in$ are shown in Fig. 11(a) and (b), respectively, while Fig. 11(c) illustrates the dependence of the output current on output voltage $V_{out}$ variations.

## 5. Training and tuning capabilities

The presented architecture possesses the capability to effect modifications even post-fabrication by using multiple control signals. This section demonstrates the exact means by which the attributes and number of the input and output MFs, as well as the fuzzy reasoning process, can be modified. All of these alterations occur at the model design-level within a software environment, in conjunction with the

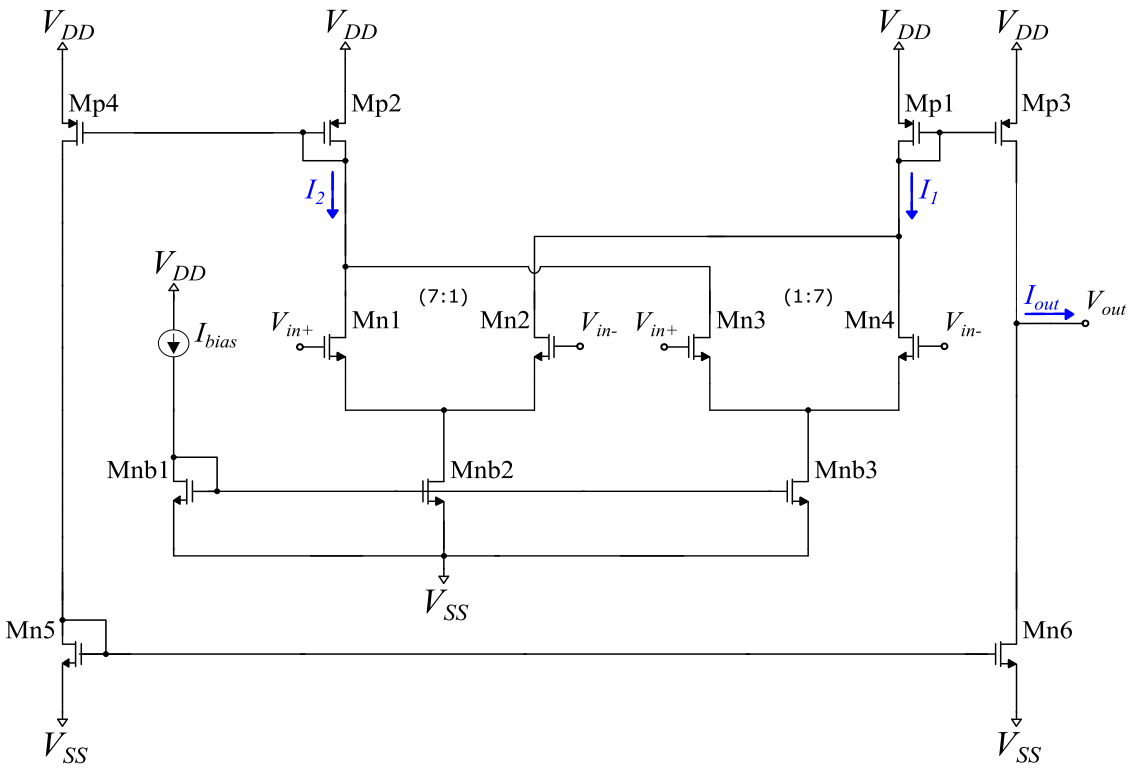



**Fig. 10.** Wide-range high open loop gain Operational Transconductance Amplifier (OTA) (defuzzification block). The current $I_{bias}$ is the circuit's bias current while $V_{in+}$ and $V_{in-}$ are its positive and negative voltage inputs, respectively. $VDD = -VSS = 0.3$ V.

model's training, and are subsequently converted into signals that are then exported to the hardware.

The construction of a FIS is typically application-dependent and always at the designer's discretion. A particularly critical process in the identification of the deep structure of a FIS is the partitioning of the input space. This process determines the number of antecedents, consequents and rules in a FIS. Therefore, when fabricating a chip, it is crucial to accommodate the potential need for additional inputs, rules and possible future changes. In order to access these post-fabrication capabilities, one should design a fairly larger system than the one needed since the number of active blocks can only be decreased. In light of these considerations, a flowchart is illustrated in Fig. 12 that outlines the pre-fabrication procedure for the design of the proposed FIS. Fig. 12 provides a visual representation of the steps involved in configuring the FIS prior to its physical realization. The processes depicted in each block of the flowchart will be comprehensively analyzed and explained in the subsequent subsection.

### 5.1. Offline training

In the offline training phase, the rule base of a FIS is constructed, which incorporates human knowledge, expertise and way of thinking into the system. This process typically involves interviews with human experts and/or system identification techniques. While defining the rule base of a FIS heuristically using domain knowledge and intuition is a straightforward solution, it does not guarantee the accuracy and robustness of the resulting FIS. However, assuming the availability of a desired input–output dataset, data-driven optimization methods solve this problem even when domain knowledge is missing.

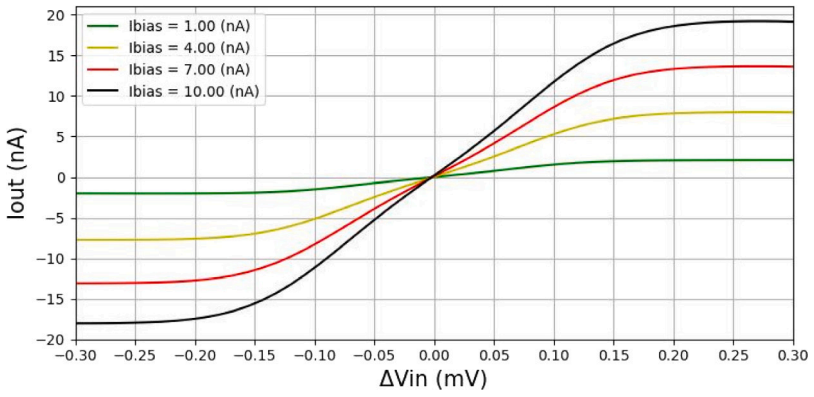
To provide with the circuit's necessary parameters, a software implementation is required. When the datasets are available in digital format, their features are pre-processed to account for the circuit's operational range (in this work, $[-155, 155]$ mV). Then, an equivalent software-based neuro-fuzzy system [12,80–82] with the same number of input and output dimensions can be trained on the same dataset and provide the appropriate optimized MF parameters and fuzzy rules.

The derived mean values and variances of the MFs are processed to generate the corresponding voltage settings $V_r$ and $V_c$ of the hardware implementation. This procedure is performed only once and the resulting parameters are exported and saved in an analog memory [83]. For each linguistic variable with m linguistic terms, parameter voltages $(V_{ri})_{i=1}^{m}$ correspond to the entries of the modeled Gaussian MF's mean value. These values can be written directly to an analog memory. On the other hand, the parameter voltages $(V_{ci})_{i=1}^{m}$ control the variance of each MF through a non-linear, monotonically increasing, bounded function. Similarly to [72], to derive this function, a single FMF circuit was simulated using different values over $V_c$, and the resulting Gaussian curves were used to fit a polynomial model that maps the acquired variances to the excitation voltages $V_c$.

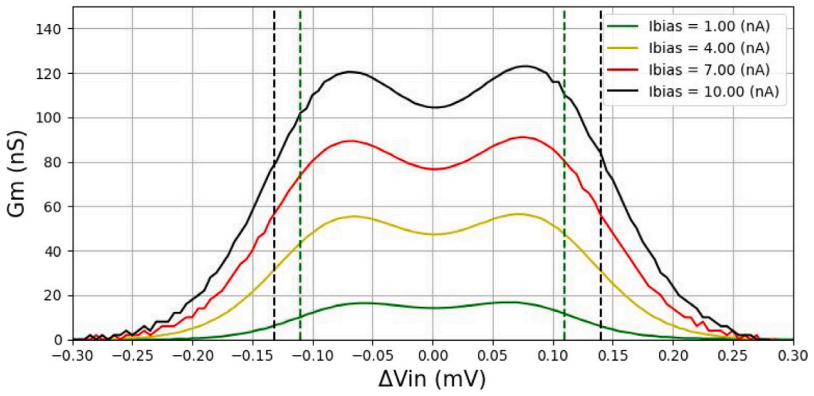
### 5.2. Architecture tunability

The number of input and output MFs corresponds to the number of Bumps and OTAs in the fuzzification and defuzzification block, respectively. Therefore, by deactivating their bias current, the operation of the associated components is disabled, resulting in the practical exclusion of the corresponding MF. Regardless of the origin of the bias current; the constant bias current of the FMFs, whereas the bias current of the OTAs which is actually the output current of the FI blocks, this can be accomplished by employing either a transmission gate or simple switches. Moreover, as described in Section 4.2, the modified Bump circuit enables the electrical tunability of the fuzzification block. By altering the $V_r$ and $V_c$ voltage settings one can effectively define any Gaussian MF for an antecedent fuzzy variable. Similarly, the mean value of the consequent Gaussian MFs is established by adjusting the bias voltage of the corresponding OTAs, given that their variance is constant.

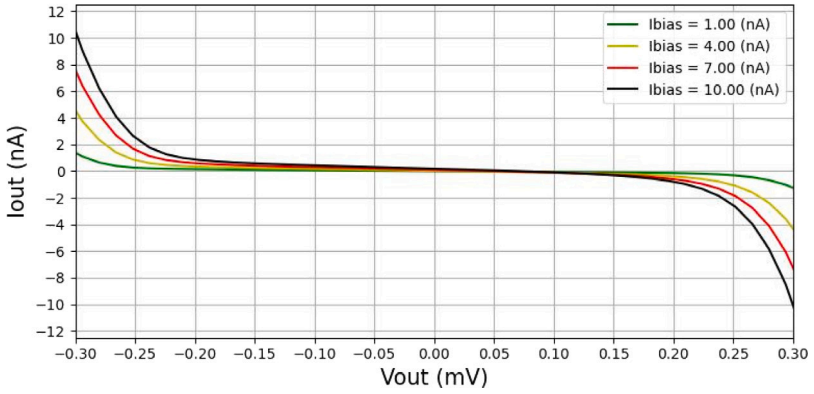
Considering that a FIS has been designed based on a specific pre-layout input space partitioning, the proposed architecture enables post-fabrication modifications also to fuzzy rules. Within the FI block, two




(a) OTA's output current $I_{out}$ for variations in $\Delta V_{in}$.




(b) OTA's transonductance $G_m$ for variations in $\Delta V_{in}$.




(c) OTA's output current $I_{out}$ for variations in $V_{out}$.

**Fig. 11.** In the subfigures (a) and (b), the output current $I_{out}$ and the transconductance $G_m$ of the OTA are depicted for different bias current values and variations in its differential voltage input $\Delta V_{in}$. The vertical dotted lines in the subfigure (b) indicate the range of the OTA's linear operation for the two extreme values of its bias current. Additionally, the output current $I_{out}$ of the OTA is illustrated in subfigure (c) for different bias current values and variations in its voltage output $V_{out}$. The proposed OTA presents a clear linear behavior of at least 220 mV differential input range and an independency from the voltage in its output of at least 400 mV range.

control signals are utilized; the first control input being a switch, and the second being a transmission gate. These control inputs determine whether the circuit will be ON or OFF, and whether the output current will be the MIN or the MAX for ANDed and ORed antecedents, respectively. As a result, there is always the capability to deactivate a FI circuit and apparently a FI block, but also modify the expression of an already implemented rule by adjusting the number of antecedents or their logic relationship. Fig. 13 illustrates the post-fabrication modifications in the high-level architecture of a FI block using these control signals to a pre-defined rule with 8 antecedents, which ultimately implements a rule with 5 of them.

To enhance the adaptability and energy efficiency of the proposed FIS, two additional attributes could be considered. Firstly, a multiplexer (MUX) integrated into the output of each FI block would allow for the selective routing of the FI's output current to the desired OTA based on a control signal. This would result in reduced power consumption by enabling multiple rules with the same consequent to share a single OTA, while deactivating the ones left. Moreover, the incorporation of a clock

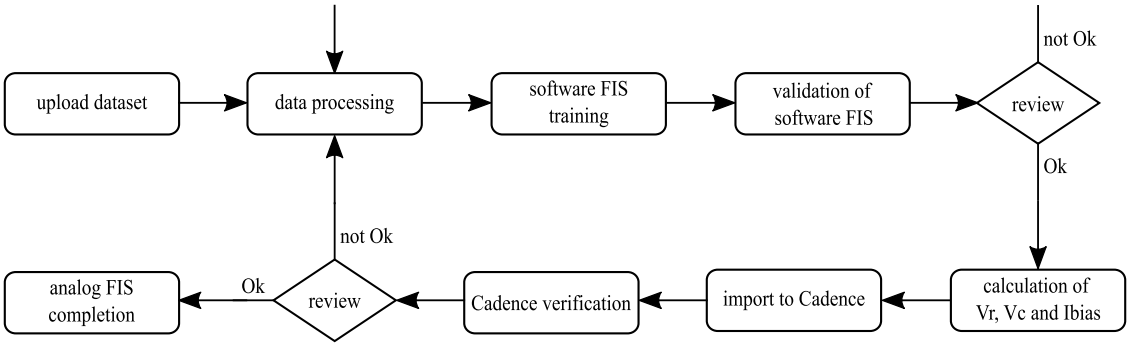



**Fig. 12.** Flowchart of the pre-fabrication procedure for the design of the proposed FIS.

***Rule*$_2$** : *If* ($V_{in1}$ *is* $A_2$ ***AND*** $V_{in2}$ *is* $B_2$) ***OR*** ($V_{in3}$ *is* $C_2$ ***AND*** $V_{in4}$ *is* $D_2$) ***AND*** (*Vin5 is E2*) *then ...*

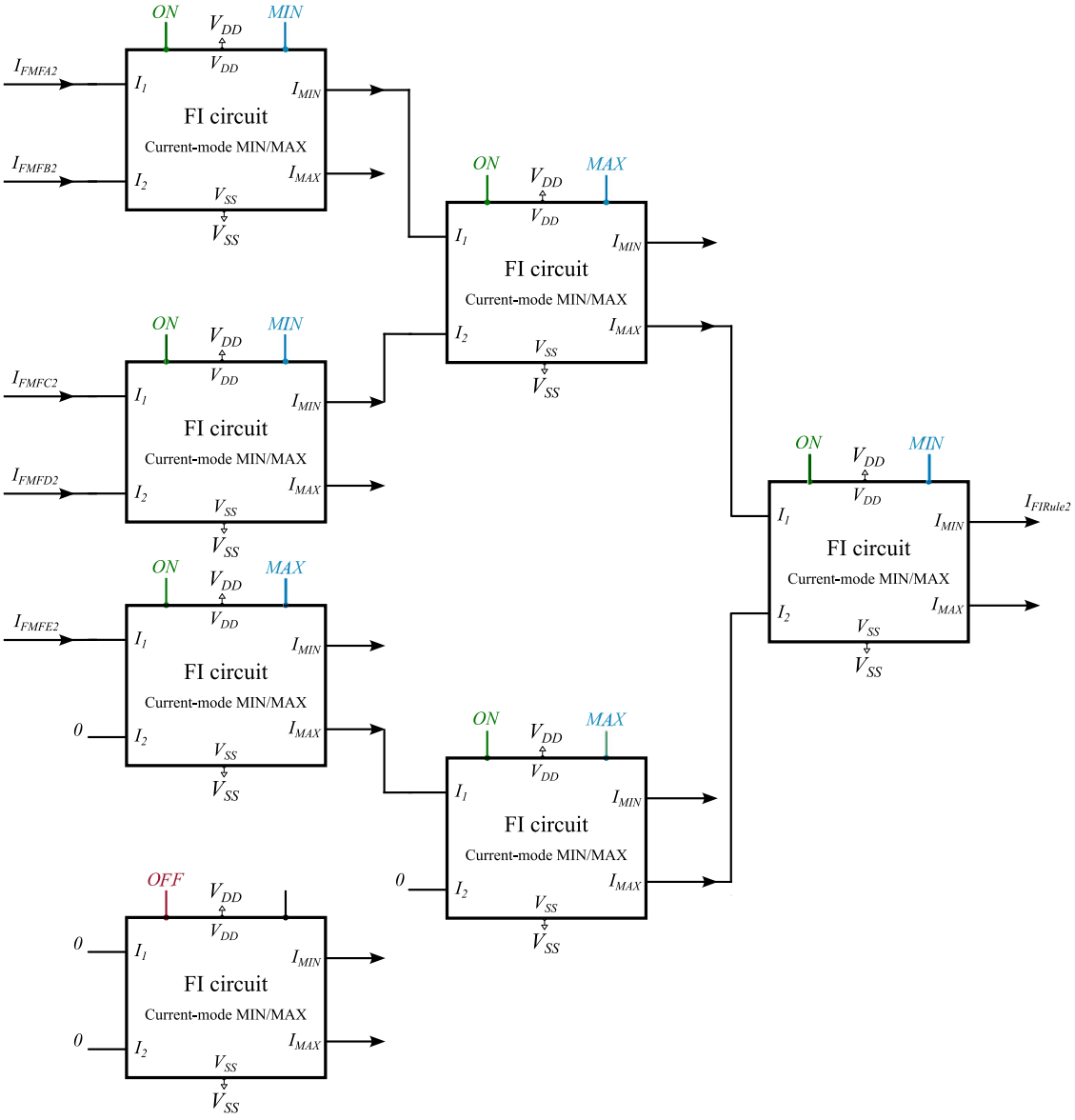



**Fig. 13.** Post-fabrication modifications in the high-level architecture of a FI block. For each FI circuit of the block a switch activates or deactivates the circuit and a transmission gate determines whether the output current of it will be the MIN or the MAX. $VDD = -VSS = 0.3$ V.

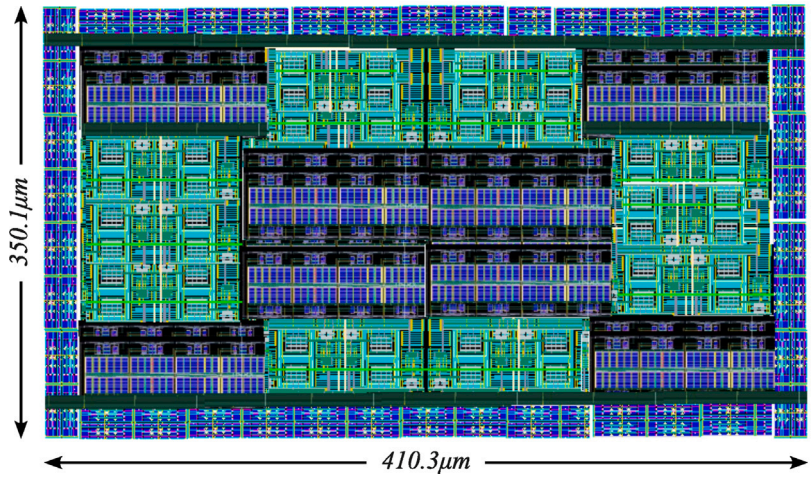



**Fig. 14.** Layout of the proposed FIS architecture based on the common-centroid technique (extra dummy transistors are used). The peripheral blue blocks symbolize the MIN/MAX circuits, while the internal green and purple-black blocks represent the Bump circuits and the OTAs, respectively. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

**Table 4**
Description of the breast cancer Wisconsin (original) dataset attributes.

| Attribute | Type | Values |
|---|---|---|
| Clump thickness | Numeric | 1–10 |
| Uniformity of cell size | Numeric | 1–10 |
| Uniformity of cell shape | Numeric | 1–10 |
| Marginal adhesion | Numeric | 1–10 |
| Single epithelial cell size | Numeric | 1–10 |
| Bare nuclei | Numeric | 1–10 |
| Bland chromatin | Numeric | 1–10 |
| Normal nucleoli | Numeric | 1–10 |
| Mitoses | Numeric | 1–10 |
| Class | Numeric | 2 (Benign), 4 (Malignant) |

**Table 5**
Accuracy results on the breast cancer Wisconsin (original) dataset (over 20 iterations).

| Method | Best (%) | Worst (%) | Mean (%) | Std. (%) |
|---|---|---|---|---|
| Software | 96.67 | 91.43 | 94.43 | 1.14 |
| Proposed | 97.14 | 91.43 | 94.71 | 1.45 |

**Table 6**
Dimensions of MOS transistors in the FMF circuit (Fig. 3).

| Differential pair | W/L (μm/μm) | Current correlator | W/L (μm/μm) |
|---|---|---|---|
| $M_{n1}$, $M_{n4}$ | 1.6/0.4 | $M_{p1}$, $M_{p2}$ | 0.4/1.6 |
| $M_{n2}$, $M_{n3}$ | 0.8/0.4 | $M_{p3} - M_{p6}$ | 0.4/1.6 |
| $M_{n5} - M_{n8}$ | 0.4/1.6 | – | – |
| $M_{n9}$, $M_{n10}$ | 2.0/1.6 | – | – |

into the FIS would enable time-based operation of the system, taking advantage of the sequential processing path from fuzzification block to FI and then defuzzification and thus lead to decreased power consumption. It should be noted that these attributes are not implemented in the proposed architecture.

## 6. Application example and simulation results

In this section, we design an analog fuzzy classifier based on the proposed architecture. A real-world dataset is used to construct the deep structure of the FIS and then verify the proposed classifier's operation, in terms of classification accuracy and circuit sensitivity, in comparison with the equivalent software model. Both the proposed architecture and the layouts were designed and simulated using the Cadence IC suite, in a TSMC 90 nm CMOS process.

The implemented layout that was utilized for the simulations is illustrated in Fig. 14. This layout adheres to the common-centroid technique [84], augmented with the inclusion of additional dummy transistors to mitigate mismatches that may arise during fabrication, thereby enhancing the overall robustness and reliability of the system. The periphery of the layout consists of blue blocks, symbolizing the MIN/MAX circuits (FI circuits). The central region of the layout encompasses scattered green blocks, representing the Bump circuits (FMF circuits), and purple-black blocks, indicating the OTAs. The distribution of the blocks within the layout is not entirely symmetrical due to the inherent complexity of the design, however their strategic placement enables efficient space utilization and promotes effective signal flow.

The processed data are acquired from the breast cancer Wisconsin (original) dataset [11] from the University of California, Irvine (UCI). This dataset is composed of 699 samples from breast cancer clinical cases. Each sample consists of 9 attributes (sample dimensions) associated with characteristics of the subject's clinical case derived from Dr. Wolberg's observations numbered on a scale of 10 and a value indicating its class (Benign or Malignant). Specifically, these 9 attributes relate to clump thickness, uniformity of cell size and shape, marginal adhesion, single epithelial cell size, bare nuclei, bland chromatin, normal nucleoli and mitoses. In this work each of them constitutes a linguistic variable composed of two linguistic terms, resulting in 18 antecedent MFs. The consequent MFs are the two existing classes that represent Benign breast cancer and Malignant breast cancer, as diagnosed by the expert physician. Table 4 summarizes the description of the features in the dataset.

The train–test set is constructed by considering a 70 – 30 random split. These data are used to train a software-based fuzzy classifier. Based on the selected input space partitioning, a fuzzy classifier with 2 rules of 9 antecedents and 1 consequent is constructed. Then its parameters are extracted into the hardware-based implementation. Both classifiers are verified using the same test set to ensure fair comparison of results. To reduce the random effects produced by the train–test split, the entire training and validation procedure is repeated 20 times.

The classification accuracy results for both implementations are summarized in Table 5, while the results for each separate iteration are depicted in a histogram in Fig. 15. The simulation results of the proposed classifier's hardware and software implementations are comparable with the hardware one being slightly more accurate (0.28% better mean accuracy). Initially this might seem strange, since analog inaccuracies usually lead to a reduction in accuracy. However, in our case (architecture and dataset) the inaccuracies that stem predominantly from the bell-shaped form of the analog Gaussian MFs, as

**Table 7**
Analog classifiers' comparison on the breast cancer Wisconsin (original) dataset.

| | Classifier | Min accuracy | Mean accuracy | Max accuracy | Power consumption | Processing speed | Energy per classification | Estimated area |
|---|---|---|---|---|---|---|---|---|
| This work | Fuzzy | 0.914 | **0.947** | 0.971 | **622.4 nW** | 4.55 K $\frac{\text{classifications}}{\text{s}}$ | $\frac{136.79\ \text{pJ}}{\text{classification}}$ | 0.144 $\text{mm}^2$ |
| [72] | GMM | 0.829 | 0.881 | 0.919 | 1.04 μW | 100 K $\frac{\text{classifications}}{\text{s}}$ | $\frac{10.4\ \text{pJ}}{\text{classification}}$ | 0.088 $\text{mm}^2$ |
| [85] | Bayes | 0.787 | 0.832 | 0.863 | 651 nW | 100 K $\frac{\text{classifications}}{\text{s}}$ | $\frac{6.51\ \text{pJ}}{\text{classification}}$ | 0.042 $\text{mm}^2$ |
| [86] | Threshold | 0.858 | 0.904 | 0.947 | 348.5 nW | 100 K $\frac{\text{classifications}}{\text{s}}$ | $\frac{10.4\ \text{pJ}}{\text{classification}}$ | 0.019 $\text{mm}^2$ |
| [87] | SVM | 0.834 | 0.868 | 0.883 | 58.1 μW | 140 K $\frac{\text{classifications}}{\text{s}}$ | $\frac{415\ \text{pJ}}{\text{classification}}$ | 0.32 $\text{mm}^2$ |
| [88] | Centroid | 0.918 | 0.946 | 0.979 | 2.2 μW | 100 K $\frac{\text{classifications}}{\text{s}}$ | $\frac{22\ \text{pJ}}{\text{classification}}$ | 0.051 $\text{mm}^2$ |

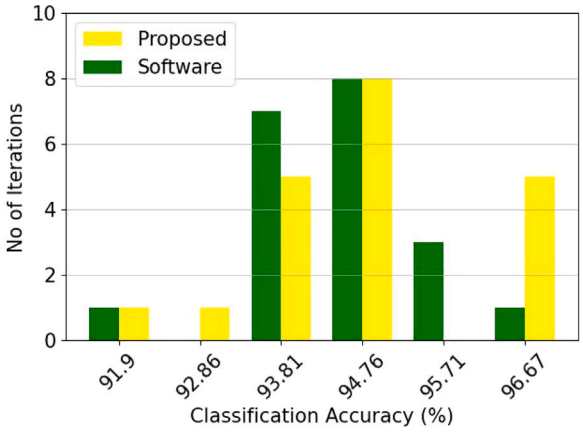



**Fig. 15.** Classification results of the proposed architecture (yellow) and the equivalent software model (green) on the breast cancer Wisconsin (original) dataset over 20 iterations. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

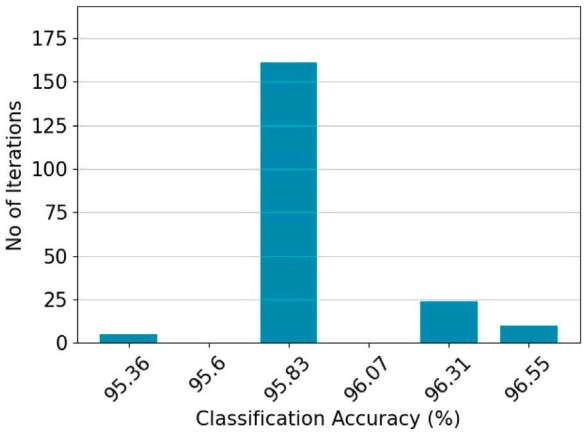



**Fig. 16.** Post-layout Monte-Carlo simulation results of the proposed architecture on the breast cancer Wisconsin (original) dataset for one of the previous iteration with 95.71% accuracy providing $\mu_M = 95.81\%$, $\sigma_M = 0.26\%$ with $max_M = 96.67\%$ and $min_M = 95.24\%$.

opposed to the more exact Gaussian functions utilized by software, actually lead to a small improvement to the classifier's performance.

The classifier is also verified in terms of circuit's sensitivity via the Monte-Carlo analysis. In this test, $N = 200$ runs are conducted with the parameters and the test set that were used in one of the previous 20 iterations that provided a performance of 95.71% accuracy. The Monte-Carlo analysis histogram is illustrated in Fig. 16 . Its mean value $\mu_M = 95.81\%$ and the standard deviation $\sigma_M = 0.26\%$ indicate good sensitivity characteristics and a robust operation.

## 7. Discussion and comparison

In the literature, most analog classifiers are designed for a specific application, hence an unbiased comparison between different implementations is impossible. However, since our team has designed a variety of classifiers based on different ML models, we can adjust them for the same application as the one tested in this work. Therefore, this section presents a comparison of all our previous works related to classifiers. Specifically, Table 7 provides a performance summary of a Gaussian mixture model (GMM) [72], a Bayesian [85], a threshold [86], a support vector machine (SVM) [87], and a centroid-based [88] classifier.

Analog classifiers usually suffer from lower accuracies, which may make them unsuitable for real-life applications in some cases. On the other hand, the fuzzy classifier can perform better against the non idealities and errors that are present in analog circuits. As shown in Table 7, the proposed fuzzy classifier demonstrates the optimal combination of ultra-low power and high accuracy performance in comparison with the other analog classifiers at the expense of lower processing speed and area efficiency. The centroid-based classifier [88] provides almost identical mean classification accuracy but consumes approximately 3.5 times more power than the proposed architecture. Moreover, although the threshold classifier [86] is a more power efficient solution (about 50% less power consumption), the proposed architecture outperforms it in terms of classification accuracy. It should be noted that for this particular application example, high classification speed is not a necessary requirement. Therefore, in the proposed architecture, the processing speed has been reduced. This leads to lower power consumption but also results in a higher energy per classification.

## 8. Conclusion

In this work, we introduced a novel ultra-low power analog integrated general-purpose type-2 FIS. It employs modified Bumps to generate Gaussian MFs, current-mode MIN/MAX circuits for the fuzzy reasoning and OTAs in a follower aggregation structure for the COG defuzzification. The FMF circuits are fully tunable allowing the shape and position of the Gaussian MFs to be controlled. Moreover, switches and transmission gates enable the post-fabrication programmability of the fuzzy reasoning process with external control signals. The proposed architecture was utilized in a fuzzy classifier design in a 90 nm TSMC technology which was then evaluated on a real-word breast cancer classification problem. The classifier was verified using the Cadence IC Suite providing an ultra-low power consumption of only 622.4 nW. Subsequently, we conducted two primary evaluations, including a comparison with the equivalent software fuzzy classifier and a Monte Carlo analysis, to confirm the correct and robust performance of the system concerning the precision of classification and susceptibility to variances and disparities, respectively. Finally, a comparison with other analog integrated classifiers evaluated on the same dataset indicated the predominance of the proposed classifier providing the optimal

combination of ultra-low power and high accuracy performance. All the above make the proposed design a very useful alternative as a type-2 hardware FIS for ultra-low power hardware fuzzy reasoning applications.

## Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

Data will be made available on request.

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## References

[1] Kumari U. Soft computing applications: A perspective view. In: 2017 2nd International conference on communication and electronics systems (ICCES). 2017, p. 787–9. http://dx.doi.org/10.1109/CESYS.2017.8321190.

[2] Ibrahim D. An overview of soft computing. Procedia Comput Sci 2016;102:34–8. http://dx.doi.org/10.1016/j.procs.2016.09.366, URL https://www.sciencedirect.com/science/article/pii/S1877050916325467, 12th International Conference on Application of Fuzzy Systems and Soft Computing, ICAFS 2016, 29-30 August 2016, Vienna, Austria.

[3] Ovaska S, Dote Y, Furuhashi T, Kamiya A, VanLandingham H. Fusion of soft computing and hard computing techniques: a review of applications. In: IEEE SMC'99 conference proceedings. 1999 IEEE international conference on systems, man, and cybernetics (Cat. No.99CH37028), vol. 1. 1999, p. 370–5. http://dx.doi.org/10.1109/ICSMC.1999.814119, vol.1.

[4] Jang H, Topal E. A review of soft computing technology applications in several mining problems. Appl Soft Comput 2014;22:638–51. http://dx.doi.org/10.1016/j.asoc.2014.05.019, URL https://www.sciencedirect.com/science/article/pii/S1568494614002464.

[5] Zadeh LA. Soft computing and fuzzy logic. IEEE Softw 1994;11(6):48–56.

[6] Jang J, Sun C, Mizutani E. Neuro-fuzzy and soft computing: A computational approach to learning and machine intelligence. MATLAB curriculum series, Prentice Hall; 1997, URL https://books.google.gr/books?id=vN5QAAAAMAAJ.

[7] Zadeh L. Fuzzy sets. Inf Control 1965;8(3):338–53. http://dx.doi.org/10.1016/S0019-9958(65)90241-X, URL https://www.sciencedirect.com/science/article/pii/S001999586590241X.

[8] Mead C. Analog VLSI and neural systems. NASA STI/Recon Techn Rep A 1989;90:16574.

[9] Smith EE, Medin DL, et al. Categories and concepts, vol. 9. Harvard University Press Cambridge, MA; 1981.

[10] Seger CA, Miller EK. Category learning in the brain. Annu Rev Neurosci 2010;33:203–19. http://dx.doi.org/10.1146/annurev.neuro.051508.135546.

[11] Mangasarian OL, Wolberg WH. Cancer diagnosis via linear programming. Tech. rep, University of Wisconsin-Madison Department of Computer Sciences; 1990.

[12] Jang J-S. ANFIS: adaptive-network-based fuzzy inference system. IEEE Trans Syst Man Cybern 1993;23(3):665–85. http://dx.doi.org/10.1109/21.256541.

[13] Jang J-S, Sun C-T. Neuro-fuzzy modeling and control. Proc IEEE 1995;83(3):378–406. http://dx.doi.org/10.1109/5.364486.

[14] Mamdani E, Assilian S. An experiment in linguistic synthesis with a fuzzy logic controller. Int J Man-Mach Stud 1975;7(1):1–13. http://dx.doi.org/10.1016/S0020-7373(75)80002-2, URL https://www.sciencedirect.com/science/article/pii/S0020737375800022.

[15] Tsukamoto Y. An approach to fuzzy reasoning method. In: Gupta MM, Ragade RK, Yager RR, editors. Adv Fuzzy Set Theory Appl 1979;3:137–49.

[16] Takagi T, Sugeno M. Derivation of fuzzy control rules from human operator's control actions. In: Proc. IFAC symp. fuzzy inform., knowledge representation and decision analysis. 1983, p. 55–60.

[17] Kar S, Das S, Ghosh PK. Applications of neuro fuzzy systems: A brief review and future outline. Appl Soft Comput 2014;15:243–59. http://dx.doi.org/10.1016/j.asoc.2013.10.014, URL https://www.sciencedirect.com/science/article/pii/S1568494613003487.

[18] Dote Y, Ovaska S. Industrial applications of soft computing: a review. Proc IEEE 2001;89(9):1243–65. http://dx.doi.org/10.1109/5.949483.

[19] Bosque G, del Campo I, Echanobe J. Fuzzy systems, neural networks and neuro-fuzzy systems: A vision on their hardware implementation and platforms over two decades. Eng Appl Artif Intell 2014;32:283–331. http://dx.doi.org/10.1016/j.engappai.2014.02.008, URL https://www.sciencedirect.com/science/article/pii/S0952197614000384.

[20] Monmasson E, Cirstea MN. FPGA design methodology for industrial control systems—A review. IEEE Trans Ind Electron 2007;54(4):1824–42. http://dx.doi.org/10.1109/TIE.2007.898281.

[21] Li T-H, Chang S-J, Chen Y-X. Implementation of human-like driving skills by autonomous fuzzy behavior control on an FPGA-based car-like mobile robot. IEEE Trans Ind Electron 2003;50(5):867–80. http://dx.doi.org/10.1109/TIE.2003.817490.

[22] Sanchez-Solano S, Cabrera AJ, Baturone I, Moreno-Velo FJ, Brox M. FPGA implementation of embedded fuzzy controllers for robotic applications. IEEE Trans Ind Electron 2007;54(4):1937–45. http://dx.doi.org/10.1109/TIE.2007.898292.

[23] Farah N, Talib MHN, Mohd Shah NS, Abdullah Q, Ibrahim Z, Lazi JBM, Jidin A. A novel self-tuning fuzzy logic controller based induction motor drive system: An experimental approach. IEEE Access 2019;7:68172–84. http://dx.doi.org/10.1109/ACCESS.2019.2916087.

[24] Zhang Z, He H, Deng X. An FPGA-implemented antinoise fuzzy recurrent neural network for motion planning of redundant robot manipulators. IEEE Trans Neural Netw Learn Syst 2023;1–13. http://dx.doi.org/10.1109/TNNLS.2023.3253801.

[25] de Souza GAF, dos Santos RB, de Abreu Faria L. Low-power current-mode interval type-2 fuzzy inference engine circuit. IEEE Trans Circuits Syst I Regul Pap 2019;66(7):2639–50. http://dx.doi.org/10.1109/TCSI.2019.2899505.

[26] Wang A, Calhoun BH, Chandrakasan AP. Sub-threshold design for ultra low-power systems, vol. 95. Springer; 2006.

[27] Bouras S, Kotronakis M, Suyama K, Tsividis Y. Mixed analog-digital fuzzy logic controller with continuous-amplitude fuzzy inferences and defuzzification. IEEE Trans Fuzzy Syst 1998;6(2):205–15. http://dx.doi.org/10.1109/91.669017.

[28] Ghasemzadeh M, Akbari A, Soltani A, Khoei A, Hadidi K. A novel mixed-signal digital CMOS fuzzy logic controller in current mode. In: 2014 Proceedings of the 21st international conference mixed design of integrated circuits and systems (MIXDES). 2014, p. 142–7. http://dx.doi.org/10.1109/MIXDES.2014.6872174.

[29] Ghasemzadeh M, Hadidi K. A new mixed-signal CMOS fuzzy logic controller in current mode. J Intell Fuzzy Systems 2020;38:1–12. http://dx.doi.org/10.3233/JIFS-191672.

[30] Merrikh-Bayat F, Bagheri Shouraki S. Memristive neuro-fuzzy system. IEEE Trans Cybern 2013;43(1):269–85. http://dx.doi.org/10.1109/TSMCB.2012.2205676.

[31] Zhang Y, Cui M, Shen L, Zeng Z. Memristive fuzzy deep learning systems. IEEE Trans Fuzzy Syst 2021;29(8):2224–38. http://dx.doi.org/10.1109/TFUZZ.2020.2995966.

[32] P AK, Azeem MF. A CMOS analog current-mode direct and complementary membership function circuit for fuzzy logic controller applications. In: 2015 3rd international conference on artificial intelligence, modelling and simulation (AIMS). 2015, p. 48–52. http://dx.doi.org/10.1109/AIMS.2015.18.

[33] Valizadeh Yaghmourali Y, Fathi A, Hassanzadazar M, Khoei A, Hadidi K. A low-power, fully programmable membership function generator using both transconductance and current modes. Fuzzy Sets and Systems 2018;337:128–42. http://dx.doi.org/10.1016/j.fss.2017.03.005, URL https://www.sciencedirect.com/science/article/pii/S0165011417301070, Theme: Applications.

[34] Fanelli de Souza G, Santos R, Rizol P, Oliveira D, Faria L. A novel fully-programmable analog fuzzifier architecture for interval type-2 fuzzy controllers using current steering mirrors. J Intell Fuzzy Syst 2017;34:1–10. http://dx.doi.org/10.3233/JIFS-171118.

[35] Kettner T, Heite C, Schumacher K. Analog CMOS realization of fuzzy logic membership functions. IEEE J Solid-State Circuits 1993;28(7):857–61. http://dx.doi.org/10.1109/4.222189.

[36] Ota Y, Wilamowski B. Cmos implementation of a voltage-mode fuzzy min-max controller. J Circuits Syst Comput 2011;06. http://dx.doi.org/10.1142/S0218126696000145.

[37] Ota Y, Wilamowski BM. Current-mode CMOS implementation of a fuzzy min-max network. 2000.

[38] Khayatzadeh R, Yazdani G, Khoie A, Hadidi K. A new structure of current mode min-max circuit using CMOS technology for fuzzy applications. In: 2014 22nd Iranian conference on electrical engineering (ICEE). 2014, p. 346–50. http://dx.doi.org/10.1109/IranianCEE.2014.6999562.

[39] Maundy B. Min/max circuit for analog convolutional decoders. IEEE Trans Circuits Syst II 2001;48(8):802–6. http://dx.doi.org/10.1109/82.959874.

[40] Kazeminia S, Khoei A, Hadidi K. High speed high precision voltage-mode MAX and MIN circuits. J Circuits Syst Comput 2007;16. http://dx.doi.org/10.1142/S0218126607003642.

[41] Sánchez Gaspariano L, Diaz-sanchez A. Cmos analog max/min operators: A qualitative comparison. 2005.

[42] Baturone I, Huertas J, Barriga A, Sánchez-Solano S. Current-mode multiple-input Max circuit. Electron Lett 1994;30:678–80. http://dx.doi.org/10.1049/el:19940510.

[43] Yildirim M. Correction to: Analog circuit architecture for max and min pooling methods on image. Analog Integr Circuits Signal Process 2022;110. http://dx.doi.org/10.1007/s10470-021-01973-1.

[44] Padash M, Khoei A, Hadidi K, Ghasemiyan H. A high precision high frequency VLSI multi-input min-max circuit based on WTA-LTA cells. In: 2011 International conference on electronic devices, systems and applications (ICEDSA). 2011, p. 152–6. http://dx.doi.org/10.1109/ICEDSA.2011.5959082.

[45] Alikhani A, Ahmadi A. A novel current-mode four-quadrant CMOS analog multiplier/divider. AEU - Int J Electr Commun 2012;66:581–6. http://dx.doi.org/10.1016/j.aeue.2011.11.012.

[46] Tanno K, Ishizuka O, Tang Z. Four-quadrant CMOS current-mode multiplier independent of device parameters. IEEE Trans Circuits Syst II 2000;47(5):473–7. http://dx.doi.org/10.1109/82.842116.

[47] Renge A, Tijare A, Dakhole P. CMOS current-mode analog multiplier. In: 2016 International conference on communication and signal processing (ICCSP). 2016, p. 0823–6. http://dx.doi.org/10.1109/ICCSP.2016.7754260.

[48] Soleimani M, Sheikhaei S. Low-voltage, low power, low area CMOS current-mode divider circuit. In: 2020 28th Iranian conference on electrical engineering (ICEE). 2020, p. 1–3. http://dx.doi.org/10.1109/ICEE50131.2020.9260610.

[49] Pirbazari M, Mesri A, Khoei A, Hadidi K. Power and area reduction in CMOS analog fuzzy logic controllers by using a new inference engine structure. J Intell Fuzzy Systems 2015;28:2863–74. http://dx.doi.org/10.3233/IFS-151565.

[50] Pirbazari MM, Khoei A, Hadidi K. Optimization of inference engine in CMOS analog fuzzy logic controllers. In: 2013 21st Iranian conference on electrical engineering (ICEE). 2013, p. 1–6. http://dx.doi.org/10.1109/IranianCEE.2013.6599654.

[51] Rocha P, Mesquita L, Botura Junior G. Design of an analog defuzzifier in CMOS tecnology. Rev CiÊncias Exatas 2006;12:129–37.

[52] Vittoz E. Analog VLSI for collective computation, vol. 2, 1998, http://dx.doi.org/10.1109/ICECS.1998.814808.

[53] Baturone I, Sánchez-Solano S, Barriga A, Huertas J. Implementation of inference/defuzzification methods via continuous-time analog circuits. 1998.

[54] Tokmakçi M. A novel CMOS defuzzification circuit employing current differencing buffered amplifier based current-mode multipliers. Inf MIDEM 2011;41:65–9.

[55] Azimi sm, Miar-Naimi H. Design an analog CMOS fuzzy logic controller for the inverted pendulum with novel triangular membership function. Sci Iranica 2018. http://dx.doi.org/10.24200/SCI.2018.5224.1153.

[56] Guo S, Peters L, Surmann H. Design and application of an analog fuzzy logic controller. IEEE Trans Fuzzy Syst 1996;4(4):429–38. http://dx.doi.org/10.1109/91.544303.

[57] Ghasemzadeh M, Akbari A, Soltani A, Khoei A, Hadidi K. A novel mixed-signal digital CMOS fuzzy logic controller in current mode. In: 2014 Proceedings of the 21st international conference mixed design of integrated circuits and systems (MIXDES). 2014, p. 142–7. http://dx.doi.org/10.1109/MIXDES.2014.6872174.

[58] Khosla M, Sarin R, Moin MM. Implementation of interval type-2 fuzzy systems with analog modules. 2012, http://dx.doi.org/10.1109/ICSGRC.2012.6287150.

[59] Ota Y, Wilamowski B. CMOS implementation of a voltage-mode fuzzy min-max controller. J Circuits Syst Comput 2011;06. http://dx.doi.org/10.1142/S0218126696000145.

[60] Khosla M, Sarin RK, Uddin M. Design of an analog CMOS based interval type-2 fuzzy logic controller chip. Int J Artif Intell Expert Syst 2011;2(4):167–83.

[61] Azeem MF, Abdulla KP. Design of an analog current mode CMOS based programmable interval Type-2 Fuzzy Inference System. In: 2016 IEEE international conference on fuzzy systems (FUZZ-IEEE). 2016, p. 2481–7. http://dx.doi.org/10.1109/FUZZ-IEEE.2016.7738005.

[62] zhi Wang W, ming Jin D. Neuro-fuzzy system with high-speed low-power analog blocks. Fuzzy Sets and Systems 2006;157(22):2974–82. http://dx.doi.org/10.1016/j.fss.2006.07.001, URL https://www.sciencedirect.com/science/article/pii/S0165011406002843.

[63] Castillo O. Introduction to type-2 fuzzy logic control. In: Type-2 fuzzy logic in intelligent control applications. Berlin, Heidelberg: Springer Berlin Heidelberg; 2012, p. 3–5. http://dx.doi.org/10.1007/978-3-642-24663-0_1.

[64] Wu D. Twelve considerations in choosing between Gaussian and trapezoidal membership functions in interval type-2 fuzzy logic controllers. In: 2012 IEEE international conference on fuzzy systems. 2012, p. 1–8. http://dx.doi.org/10.1109/FUZZ-IEEE.2012.6251210.

[65] Jang J-S, Sun C-T. Functional equivalence between radial basis function networks and fuzzy inference systems. IEEE Trans Neural Netw 1993;4(1):156–9. http://dx.doi.org/10.1109/72.182710.

[66] Nowak-Brzezińska A, Horyń C. Exploration of outliers in if-then rule-based knowledge bases. In: Entropy, vol. 22. Basel, Switzerland; 2020, http://dx.doi.org/10.3390/e22101096.

[67] van Krieken E, Acar E, van Harmelen F. Analyzing differentiable fuzzy logic operators. Artificial Intelligence 2022;302:103602. http://dx.doi.org/10.1016/j.artint.2021.103602, URL https://www.sciencedirect.com/science/article/pii/S0004370221001533.

[68] Siminski K. An outlier–robust neuro–fuzzy system for classification and regression. Int J Appl Math Comput Sci 2021;31(2):303–19.

[69] Van Broekhoven E, De Baets B. A comparison of three methods for computing the center of gravity defuzzification. In: 2004 IEEE international conference on fuzzy systems (IEEE Cat. No.04CH37542), vol. 3. 2004, p. 1537–42. http://dx.doi.org/10.1109/FUZZY.2004.1375403, vol.3.

[70] Kosko B. Neural networks and fuzzy systems: a dynamical systems approach to machine intelligence. 1991.

[71] Alimisis V, Gourdouparis M, Gennis G, Dimas C, Sotiriadis PP. Analog Gaussian function circuit: Architectures, operating principles and applications. Electronics 2021;10(20). http://dx.doi.org/10.3390/electronics10202530, URL https://www.mdpi.com/2079-9292/10/20/2530.

[72] Alimisis V, Gennis G, Touloupas K, Dimas C, Gourdouparis M, Sotiriadis PP. Gaussian Mixture Model classifier analog integrated low-power implementation with applications in fault management detection. Microelectron J 2022;126:105510. http://dx.doi.org/10.1016/j.mejo.2022.105510, URL https://www.sciencedirect.com/science/article/pii/S0026269222001410.

[73] Delbrueck T, Mead C. Bump circuits. In: Proceedings of international joint conference on neural networks, vol. 1. 1993, p. 475–9.

[74] Gourdouparis M, Alimisis V, Dimas C, Sotiriadis PP. An ultra-low power,±0.3 V supply, fully-tunable Gaussian function circuit architecture for radial-basis functions analog hardware implementation. AEU-Int J Electron Commun 2021;136:153755.

[75] Dualibe C, Verleysen M, Jespers P. Design of analog fuzzy logic controllers in CMOS technologies: Implementation, test and application. 2003, http://dx.doi.org/10.1007/b101857.

[76] Sánchez Gaspariano L, Diaz-sanchez A. Cmos analog max/min operators: A qualitative comparison. 2005.

[77] Alikhani A, Ahmadi A. A novel current-mode min–max circuit. Analog Integr Circuits Signal Process 2011;72:343–50. http://dx.doi.org/10.1007/s10470-012-9867-y.

[78] Baturone I, Solano SS, Barriga A, Huertas JL. Implementation of inference/defuzzification methods via continuous-time analog circuits. 1995.

[79] Daneshvar M, Aminifar S, Yosefi G. Design and analysis of current-mode CMOS analog defuzzification circuits for fuzzy controllers. 2011.

[80] Carpenter G, Grossberg S, Markuzon N, Reynolds J, Rosen D. Fuzzy ARTMAP: A neural network architecture for incremental supervised learning of analog multidimensional maps. IEEE Trans Neural Netw 1992;3(5):698–713. http://dx.doi.org/10.1109/72.159059.

[81] Farag W, Quintana V, Lambert-Torres G. A genetic-based neuro-fuzzy approach for modeling and control of dynamical systems. IEEE Trans Neural Netw 1998;9(5):756–67. http://dx.doi.org/10.1109/72.712150.

[82] Takagi T, Sugeno M. Fuzzy identification of systems and its applications to modeling and control. IEEE Trans Syst Man Cybern 1985;SMC-15(1):116–32. http://dx.doi.org/10.1109/TSMC.1985.6313399.

[83] Hock M, Hartel A, Schemmel J, Meier K. An analog dynamic memory array for neuromorphic hardware. In: 2013 European conference on circuit theory and design (ECCTD). IEEE; 2013, p. 1–4.

[84] Sharma AK, Madhusudan M, Burns SM, Mukherjee P, Yaldiz S, Harjani R, Sapatnekar SS. Common-centroid layouts for analog circuits: Advantages and limitations. In: 2021 Design, automation and test in europe conference and exhibition (DATE). 2021, p. 1224–9. http://dx.doi.org/10.23919/DATE51398.2021.9474244.

[85] Alimisis V, Gennis G, Dimas C, Sotiriadis PP. An analog Bayesian classifier implementation, for thyroid disease detection, based on a low-power, current-mode gaussian function circuit. In: 2021 International conference on microelectronics (ICM). IEEE; 2021, p. 153–6.

[86] Alimisis V, Gennis G, Tsouvalas E, Dimas C, Sotiriadis PP. An analog, low-power threshold classifier tested on a bank note authentication dataset. In: 2022 International conference on microelectronics (ICM). IEEE; 2022, p. 66–9.

[87] Alimisis V, Gennis G, Gourdouparis M, Dimas C, Sotiriadis PP. Low-power analog integrated implementation of the support vector machine algorithm with on chip learning tested on a bearing fault application. Sensors 2023;23(8):3978.

[88] Alimisis V, Mouzakis V, Gennis G, Tsouvalas E, Dimas C, Sotiriadis PP. A hand gesture recognition circuit utilizing an analog voting classifier. Electronics 2022;11(23):3915.