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Ultra-Low Power ($4nW$), $0.6V$ Fully-Tunable Bump Circuit operating in Sub-threshold regime

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***Abstract*—A compact, ultra-low power ($4nW$), low supply voltage ($0.6V$) Gaussian-bump circuit architecture for Radial Basis Functions implementation is presented. It consists of only ten transistors, all operating in sub-threshold. The Gaussians center, height and width are independently and electronically controlled. The proposed architecture is used as a building block to construct a $2-D$ Gaussian cascaded bump structure, demonstrating its dimensional scalability. Proper operation, sensitivity and accuracy are confirmed via theoretical analysis and simulation. The presented architectures were realized in TSMC $90nm$ CMOS process and were simulated using the Cadence IC Suite.**

***Index Terms*—Bump circuit, ultra-low power design, bulk-controlled circuits, fully tunable implementation, sub-threshold design**

I. Introduction

Analog integrated circuits are widely used in various applications in Internet of Things (IoT) and Machine Learning (ML) fields because they provide the ability for low power information processing [1]–[4]. The implementation of circuits for analog ML and analog computing enables the development of low power electronic systems interfacing with sensors [1]–[4] and extracting useful information from their measurements. Moreover, ultra-low power and low area analog circuits are an interesting candidate for edge computing because they address the requirement for high speed, long battery life and processing ability away from data centers [5].

Data classification and regression problems are solved by ML methods, many of which are based on Gaussian functions as activation functions. These functions can be easily implemented in hardware by analog circuits which are well-known in literature as Bump circuits or Gaussian circuits. The first analog bump circuit architecture was presented by Delbruck [6]. In literature, it is referred to Simple Bump (SB) and it is a simple and compact architecture because it consists of only 8 transistors. The Gaussian function is produced by the current correlator's [6] output current I_{out} and shows the similarity between the differential pair's output currents I_1 and I_2. These two subcircuits (current correlator and differential pair) constitute the SB circuit. Our work is based on a modification of the SB.

Bump circuits are widely used in the domain of analog ML. Classifiers, Neural Networks (NN), neuromorphic circuits and sensor applications are implemented by analog integrated circuits which use Gaussian circuits as basic building blocks [7]–[17]. Tunable Bump circuit's ability of width update is an important factor for the implementation of Radial Basis Functions (RBFs) or tunable kernels [7]. Moreover, due to the fact that bump circuits have low power consumption and they are compact topologies, multivarate kernels and RBF NN can be easily designed [8], [9] (many layers which consist of many neurons). Also, there are certain implementations, in which Support Vector Machine (SVM) algorithm [10]–[12] is developed by tunable kernels (tunable bump circuits). In neuromorphic computing, Gaussian circuits are used either for the "stop learning" case [13], [14] or as part of the weight update mechanism [15]. Unsupervised anomaly detection [16] and image edge detection [17] are some of the sensor applications, in which Bump circuits are used.

Gaussian Functions are implemented by different versions of bump circuits. A simple structure which consists of only 4 transistors but lacks tunability is presented in [18] and it is a modification of the Gilbert Gaussian (GG) circuit [11]. Also, there are many bump circuits which achieve the width tunability by altering the dimensions of the transistors [6], [8]. Except from the SB, translinear (TRL.) circuits and exponential (EXP.) circuits are used for the implementation of low power fully tunable Gaussian functions [19], [20]. The increased circuit's complexity provides the appropriate tunability in parameters. Also, there are implementations which use extra stages such as Digital to Analog Converters (DAC) [11], operational transcoductance amplifiers [21] and pseudo-differential transcoductors [22]. Moreover, complicated bump circuits are implemented by adding prescaling circuits which consist of floating gate (FG) transistors [7]. Alternative implementations are based on bulk-controlled transistors [13], [23]. The alteration in the transistors bulks' voltage provides independent adjustment of parameters (width tunability). This is a main characteristic of the proposed bump circuit too.

This paper is organized as follows: the proposed circuit architecture and theoretical mathematical analysis are presented in Section II. The behavior of the proposed bump circuit is evaluated in Section III, in TSMC $90nm$ CMOS process. Moreover, in Section IV performance summary and

comparison with literature are discussed. Section V concludes the paper.

II. Proposed Architecture and Analysis

In this section, the proposed architecture and its mathematical analysis are presented. The implemented bump circuit is an alteration of the original Delbruck's SB [6]. This modification achieves ultra low power consumption ($4nW$), low voltage power supply ($V_{DD} = -V_{SS} = 0.3V$) and electronically controllable height, width and center of the produced Gaussian curve.

The proposed bump circuit is shown in Fig. 1 and its output current is a Gaussian function in relation to the input voltage (V_{in}) as shown in Fig. 2. Our architecture is composed of two subcircuits. In this work a modified current correlator (non-symmetric implementation) is used, and the differential pair of Delbruck's SB is substituted by a NMOS bulk-controlled block ($M_{n1} - M_{n4}$ and M_{n6}) [6]. Tunability is achieved with the use of three circuit's parameters. Parameter voltage V_c, which is connected to the bulks of transistors $M_{n1} - M_{n2}$, adjusts the width of the Gaussian curve, while parameter voltage V_m tunes its center. All other NMOS have their bulks connected to V_{SS} whereas the bulks of all PMOS are connected to V_{DD}. Furthermore, bias current I_{bias} sets the height of the Gaussian function. The tunability of these three characteristics (width, height, center) is further explained via Mathematical Analysis and Simulation Results. All transistors operate in the sub-threshold region and their dimensions are summarized in Table I.

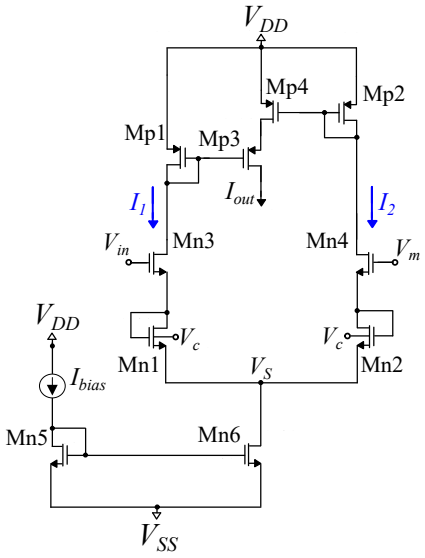

Fig. 1: Proposed Bump circuit.

The mathematical analysis of the proposed bump circuit is presented below. The MOS model in [24] is used to describe the operation of the circuit's transistors in the sub-threshold region according to the following equations for PMOS and NMOS respectively:

$$I_{pmos} = I_{o_p} e^{\kappa_p (V_w - V_G)/V_T} \left(e^{(V_S - V_w)/V_T} - e^{(V_D - V_w)/V_T} \right) \quad (1)$$

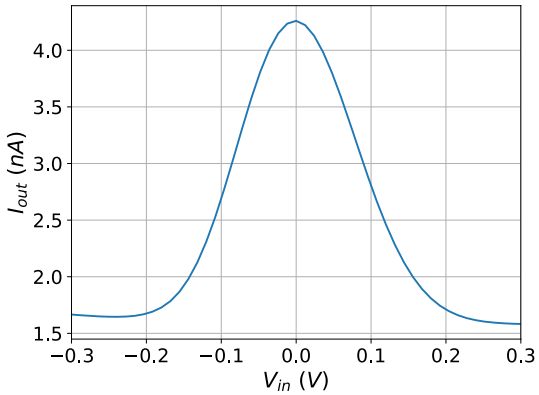

Fig. 2: Output current of Bump circuit for $I_{bias} = 5nA$, $V_c = -300mV$ and $V_m = 0mV$.

TABLE I: MOS Transistors Dimensions.

Block	W/L (µm/µm)	Current Correlator	W/L (µm/µm)
M_{n1}-M_{n2}	1.0/0.1	M_{p1},M_{p3}	0.8/0.1
M_{n3},M_{n4}	1.0/1.6	M_{p2}	0.8/0.4
M_{n5},M_{n6}	0.2/1.6	M_{p4}	2.4/0.4

$$I_{nmos} = I_{o_n} e^{\kappa_n (V_G - V_w)/V_T} \left(e^{(V_w - V_S)/V_T} - e^{(V_w - V_D)/V_T} \right) \quad (2)$$

where: I_{o_p} and I_{o_n} are the pre-exponential currents ,while κ_p and κ_n are the slope factors for PMOS and NMOS transistors respectively, V_w, V_G, V_S and V_D are the bulk voltage, gate voltage, source voltage and drain voltage respectively and V_T is the thermal voltage [24]. We consider the I_{o_p} and I_{o_n} values of reference for PMOS and NMOS transistors respectively. For every transistor we consider, we use a scaling factor (m), i.e. mI_{o_p} or mI_{o_n}, to capture the relative W/L value according to Table I.

A. Modified Current Correlator Analysis

Transistors' M_{p1} and M_{p2} currents which operate in saturation region are given by:

$$I_1 = I_{M_{p1}} = 4I_{o_p} e^{\kappa_p (V_{DD} - V_{D_{Mp1}})/V_T} \quad (3)$$

$$I_2 = I_{M_{p2}} = I_{o_p} e^{\kappa_p (V_{DD} - V_{D_{Mp2}})/V_T} \quad (4)$$

where $V_{D_{Mp1}}$ and $V_{D_{Mp2}}$ are the drain voltages of transistors M_{p1} and M_{p2} respectively. Assuming the drain voltage of M_{p3}, is sufficiently low to guarantee saturation of the transistor, the drain current is:

$$I_{out} = I_{M_{p3}} = 4I_{o_p} e^{((\kappa_p - 1)V_{DD} - \kappa_p V_{D_{Mp1}} + V_{D_{Mp4}})/V_T} \quad (5)$$

where $V_{D_{Mp4}}$ is the drain voltage of transistor M_{p4}. Unlike transistors M_{p1}, M_{p2}, M_{p3}, transistor M_{p4} operates in triode region and its drain current is:

$$I_{M_{p4}} = 3I_{o_p} e^{\kappa_p (V_{DD} - V_{D_{Mp2}})/V_T} \left(1 - e^{(V_{D_{Mp4}} - V_{DD})/V_T} \right) \quad (6)$$

Combining (3)-(6) and using $I_{M_{p4}} = I_{out}$ we conclude:

$$I_{out} = \frac{3I_1 I_2}{I_1 + 3I_2} \quad (7)$$

B. NMOS Bulk-Controlled Block Analysis

$M_{n1}-M_{n4}$ and M_{n6} are the NMOS bulk-controlled block's transistors. Transistors M_{n1} and M_{n2} have the same characteristics. They operate in sub-threshold triode region and their bulks are connected to a voltage V_c. Their triode currents are given by:

$$I_1 = 16I_{o_n} e^{\kappa_n (V_{S_{Mn3}} - V_c)/V_T} (e^{(V_c - V_S)/V_T} - e^{(V_c - V_{S_{Mn3}})/V_T}) \tag{8}$$

$$I_2 = 16I_{o_n} e^{\kappa_n (V_{S_{Mn4}} - V_c)/V_T} (e^{(V_c - V_S)/V_T} - e^{(V_c - V_{S_{Mn4}})/V_T}) \tag{9}$$

where $V_{S_{Mn3}}$ and $V_{S_{Mn4}}$ are the source voltages of transistors M_{n3} and M_{n4}. Transistors M_{n3} and M_{n4} operate in saturation region and their currents are given by:

$$I_1 = I_{o_n} e^{(\kappa_n V_{in} + (1-\kappa_n)V_{SS} - V_{S_{Mn3}})/V_T} \tag{10}$$

$$I_2 = I_{o_n} e^{(\kappa_n V_m + (1-\kappa_n)V_{SS} - V_{S_{Mn4}})/V_T} \tag{11}$$

In this step, we combine eqs. (8) and (10). The current I_1 is given by:

$$I_1^{(\kappa_n+1)} + I_{x1} \frac{I_1}{I_{o_n}} e^{((\kappa_n - 1)V_{SS} - \kappa_n V_{in})/V_T} = I_{x1} e^{-V_S/V_T} \tag{12}$$

We combine eqs. (9) and (11). The current I_2 is given by:

$$I_2^{(\kappa_n+1)} + I_{x2} \frac{I_2}{I_{o_n}} e^{((\kappa_n - 1)V_{SS} - \kappa_n V_m)/V_T} = I_{x2} e^{-V_S/V_T} \tag{13}$$

The parameter term I_{x1} which depends on the input voltage V_{in} and parameter voltage V_c is given by the following expression:

$$I_{x1} = 16 I_{o_n}^{(\kappa_n+1)} e^{(\kappa_n^2 V_{in} + (1-\kappa_n)V_c + (\kappa_n - \kappa_n^2)V_{SS})/V_T} \tag{14}$$

The parameter term I_{x2} which depends on the parameter voltage V_m and parameter voltage V_c is given by the following expression:

$$I_{x2} = 16 I_{o_n}^{(\kappa_n+1)} e^{(\kappa_n^2 V_m + (1-\kappa_n)V_c + (\kappa_n - \kappa_n^2)V_{SS})/V_T} \tag{15}$$

With M_{n6} operating in triode, the voltage V_S in (12) and (13) is such that:

$$e^{-V_S/V_T} = \frac{-I_1 - I_2 + I_{bias}}{I_{bias} e^{V_{SS}/V_T}} \tag{16}$$

Substitution of (16) into (12) and (13) leads to the following non-linear system of equations with unknown I_1 and I_2:

$$I_1^{(\kappa_n+1)} + I_1 \left(\frac{I_{x1}}{I_{bias} e^{V_{SS}/V_T}} + \frac{I_{x1}}{I_{o_n}} e^{((\kappa_n - 1)V_{SS} - \kappa_n V_{in})/V_T} \right) = I_{x1} \frac{I_{bias} - I_2}{I_{bias} e^{V_{SS}/V_T}} \tag{17}$$

$$I_2^{(\kappa_n+1)} + I_2 \left(\frac{I_{x2}}{I_{bias} e^{V_{SS}/V_T}} + \frac{I_{x2}}{I_{o_n}} e^{((\kappa_n - 1)V_{SS} - \kappa_n V_m)/V_T} \right) = I_{x2} \frac{I_{bias} - I_1}{I_{bias} e^{V_{SS}/V_T}} \tag{18}$$

C. Theoretical Behavior of the Bump Circuit

The behavior of the proposed bump circuit is evaluated via the numerical solution of the non-linear system (17) and (18). The solution is reached with the aid of MATLAB's fsolve function. The theoretical output current of (7) is depicted in Figs. 3 and 4. In Fig. 3, all the circuit's parameters are constant except from parameter voltage V_c, which tunes the width of the Gaussian function. In Fig. 4, parameter voltage V_m alters independently the center of the Gaussian curve. In both cases, the proposed circuit's theoretical analysis demonstrates its appropriate behavior and performance.

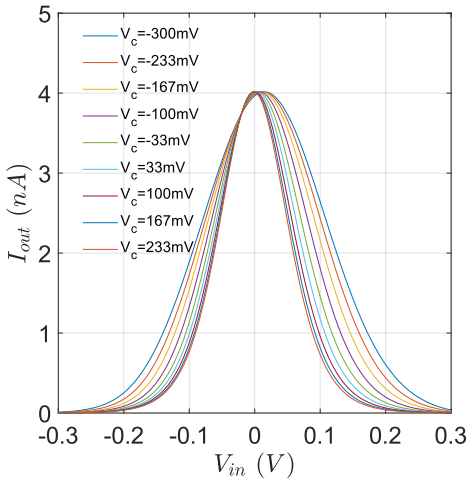

Fig. 3: Width tuning in Theoretical Output current of Bump circuit, for $I_{bias} = 5nA$ and $V_m = 0mV$.

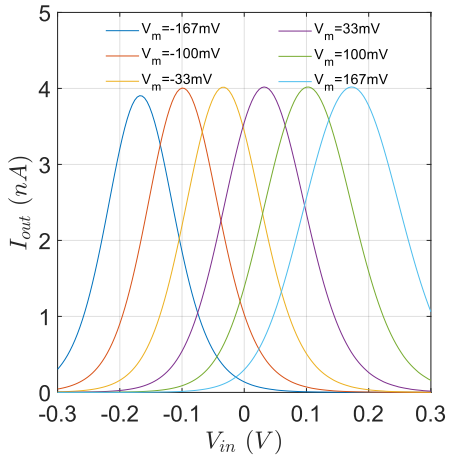

Fig. 4: Center adjustment in Theoretical Output current of Bump circuit, for $I_{bias} = 5nA$ and $V_c = -300mV$.

D. Cascaded 2-D Implemenation

The previous subsections analyze the $1-D$ bump circuit's architecture and mathematical analysis. However, the bump circuit's architecture is scalable, extending to more dimensions. Multivariate RBFs are implemented by cascaded bump circuits. These are formed by two or more bump circuits, in

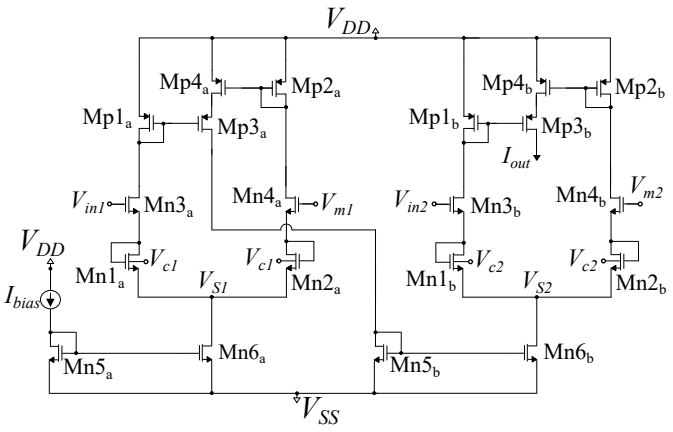

Fig. 5: $2-D$ Implementation schematic.

which the output current of each bump cell is used as the next bump cell's bias current. Different input voltage and circuit's parameters (V_m, V_c) are used in each cascaded bump circuit's stage. A $2-D$ implementation which uses two bump circuits is shown in Fig. 5.

III. Simulations Results

The proposed ultra-low power ($4nW$), low voltage power supply rails ($V_{DD} = -V_{SS} = 0.3V$), fully-tunable bump circuit has been designed and evaluated in TSMC $90nm$ CMOS process, using the Cadence IC design suite. All transistors operate in the sub-threshold region and the minimum bias current is $I_{bias,min} = 3nA$. In theoretical analysis, we prove that width and center depend on parameter voltages V_c and V_m respectively. In this Section, simulations and results are presented and analyzed in order to confirm the expected theoretical behavior.

A. 1-D Simulation Results

The Gaussian curve's width is controlled via parameter V_c. In Fig. 1 the $M_{n1} - M_{n2}$ transistors' bulks (operating as diodes) are connected to the voltage V_c. The value of V_c affects the transistors' transconductance g_m, thus altering the slope of the differential block's currents I_1 and I_2, as demonstrated in Figs. 6 and 7. As a result, an independent tuning of width is achieved (without affecting the height and center) by altering the bulks' voltage V_c as shown in Fig. 8. The scaling of the Gaussian Function's height is achieved by adjusting the bias current (I_{bias}) as shown in Fig. 9. An increase in the bias current results in a growth in the Gaussian curve's height. Moreover, parameter voltage V_m adjusts the center of the Gaussian curve, as shown in Fig. 10. The output current's value is maximized when the input voltage V_{in} of the bump circuit matches the parameter voltage V_m ($V_{in} = V_m$).

B. 2-D Simulation Results

The previous figures analyze the behavior of $1-D$ bump circuit. In this step, $2-D$ Gaussian Functions are shown in three dimensional space. The output current of the cascaded

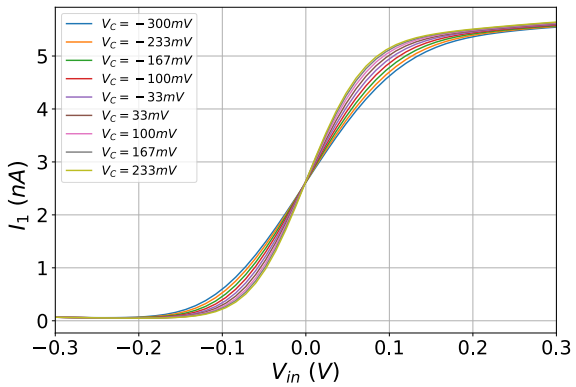

Fig. 6: Tuning of NMOS bulk-controlled block's current I_1 via parameter voltage V_c, for $I_{bias} = 5nA$ and $V_m = 0mV$.

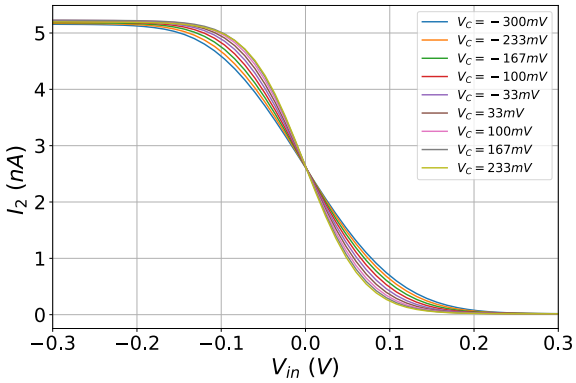

Fig. 7: Tuning of NMOS bulk-controlled block's current I_2 via parameter voltage V_c, for $I_{bias} = 5nA$ and $V_m = 0mV$.

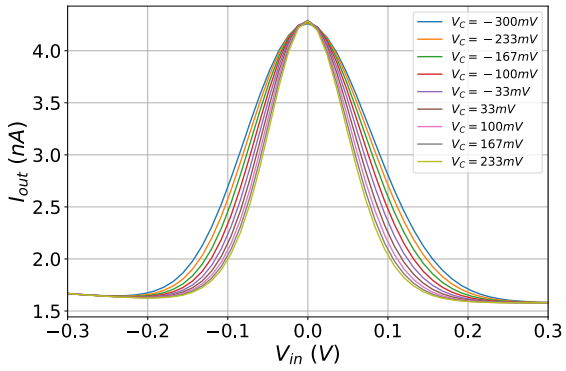

Fig. 8: Width tuning of the output current with control voltage V_c, for $I_{bias} = 5nA$ and $V_m = 0mV$.

bump implementation is shown in Fig. 11. We bias the first bump circuit with $I_{bias} = 10nA$. Both Gaussian circuits' bulks are biased with $V_c = 300mV$ and parameter voltage V_m is kept constant at $0V$. In Fig. 12, we increase the bias current's value ($I_{bias} = 30nA$), while the other parameters are kept constant. In Fig.13 we use the same bias current ($I_{bias} = 30nA$), but the bulks are biased with $V_c = -300mV$, which increases the Gaussian curve's width, in comparison with the results in Fig. 12.

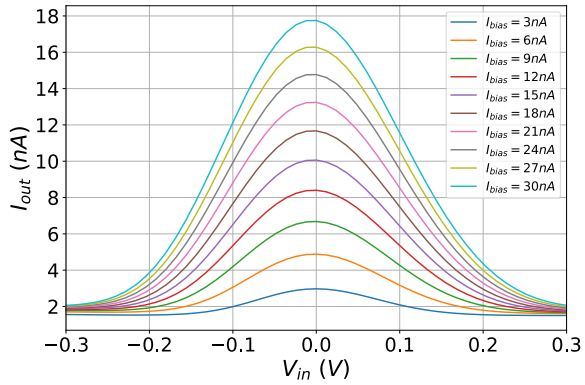

Fig. 9: Height scaling with bias current I_{bias}, for $V_c = -300mV$ and $V_m = 0mV$.

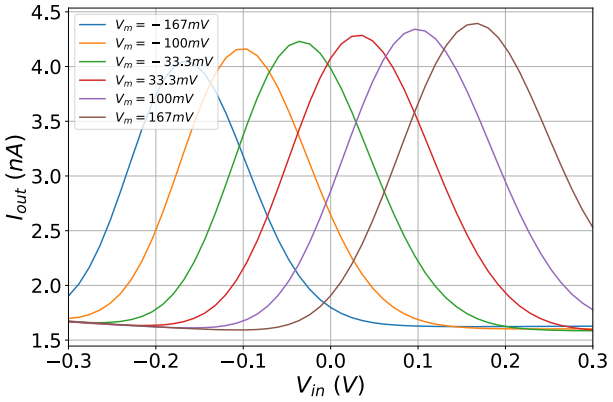

Fig. 10: Center adjustment with programmable voltage V_m, for $I_{bias} = 5nA$ and $V_c = -300mV$.

The sensitivity behavior has been evaluated using the Monte-Carlo analysis tool for $N = 100$ runs. The corresponding histogram for the bump circuit's center of voltage is shown in Fig. 14. The mean value of the voltage is $V_{mean} = 2.3mV$, and the standard deviation is $\sigma_V = 5.6mV$. It confirms the correct performance and accuracy of the proposed circuit.

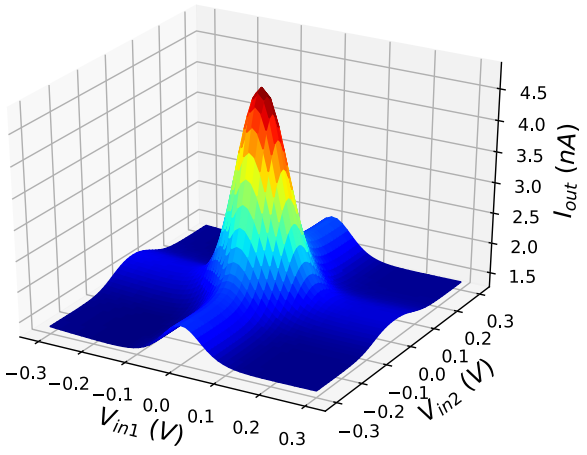

Fig. 11: A $2-D$ Gaussian Function with bias current $I_{bias} = 10nA$ and $V_c = 300mV$.

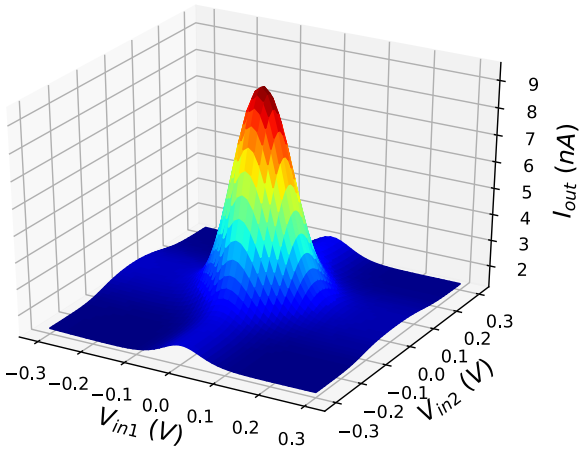

Fig. 12: A scaled height $2-D$ Gaussian Function with $I_{bias} = 30nA$ and $V_c = 300mV$.

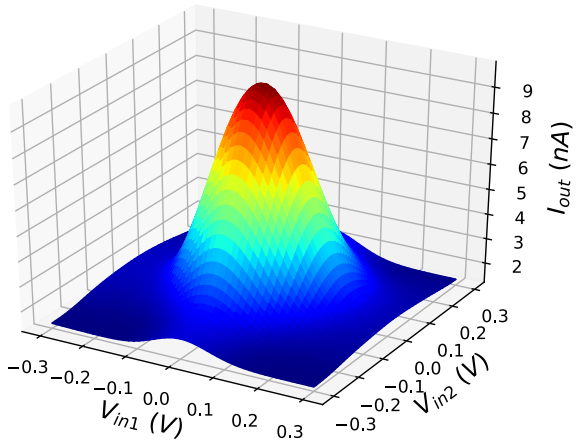

Fig. 13: A scaled height and width $2-D$ Gaussian Function with $I_{bias} = 30nA$ and $V_c = -300mV$.

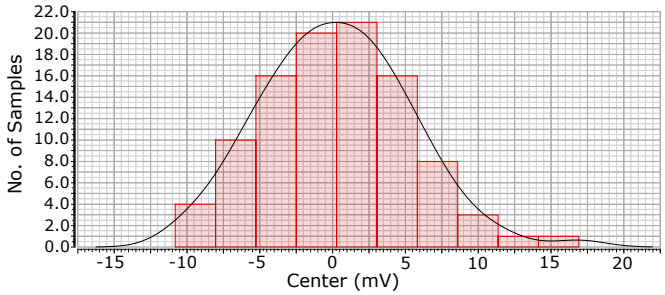

Fig. 14: Center value sensitivity via Monte-Carlo simulation.

IV. Literature Comparison

The comparison in performance and circuit's characteristics between previous works and our implementation is presented in Table II. The proposed bump circuit consumes $4nW$, which is a great improvement in comparison with literature. Also, an ultra-low power bump circuit, is presented in [8], which consumes $13.5nW$. While in previous works the lowest power

TABLE II: Performance Summary and Comparison.

	This work	**[8]**	**[9]**	**[18]**	**[19]**	**[20]**	**[22]**	**[23]**
Technology	$90nm$	$180nm$	$16nm$	$180nm$	$180nm$	$180nm$	$130nm$	ALD
Power Consumption	$4nW$	$13.5nW$	$4.1\mu W$	-	$350nW$	-	$18.9nW$	-
Power Supply	$0.6V$	$0.9V$	$0.7V$	$1.3-2V$	0.7	$1.8V$	$3V$	$5V$
Minimum I_{bias}	$3nA$	$40nA$	$1\mu A$	-	$50nA$	$50nA$	$1nA$	$2nA$
No of Transistors	10	9	22	4	31	14	14	10
Ind. Param. Tun.	YES	NO	YES	NO	YES	YES	YES	YES

supply voltage is $0.7V$ [9], [19], in the proposed bump circuit, a power supply voltage of $0.6V$ is used. Our implementation has the ability to operate with bias current I_{bias} down to $3nA$, which is close to the minimum bias current used in [22] (only $1nA$). The minimum number of transistors is presented in [18], only 4 transistors which results in very low circuit area, but with absence of tunability in width. The proposed bump circuit is electronically adjustable. Moreover, it is compact because it is composed of only 10 transistors. Except from the use of CMOS architectures, in [9] LTSpice with 16nm PTM transistor models and MS memristor model and in [23] quad MOS transistor arrays ALD1106 and ALD1107, which are manufactured by Advanced Linear Devices (ALD) are used.

V. Conclusion

A compact, ultra-low power, low voltage, 10 transistors adjustable bump circuit was presented in this work. The theoretical analysis explains the proposed circuit's behavior. The $1-D$ simulations results confirm the programmability of the output current's width, height and center via three circuit's parameters. Also, the $2-D$ simulations and results verify the scalability of the proposed bump circuit, which makes it an interesting candidate for the implementation of multivariate Radial Basis Functions with low power and low circuit area.

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