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# Multi-Objective Optimization Methods for CMOS LC-VCO Design

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***Abstract*—This work addresses the use of Electronic Design Automation (EDA) tools for topology selection and optimal sizing of Voltage Controlled Oscillator (VCO) Integrated Circuits (ICs). Instead of relying on empirical data and closed form equations to select device sizes, a simulation-based approach is adopted for better accuracy. By using an optimization method based on Evolutionary Algorithms (EAs) in combination with a tool for parametrized schematic simulations, we are able to asses the attainable performance trade-offs for different topologies and oscillation frequencies. We use Cadence Spectre for simulations and demonstrate our approach on two cross-coupled LC-VCO topologies by providing with Pareto optimal Fronts.**

## I. Introduction

The continuous advancements in CMOS Integrated Circuits (ICs) have led to complex electronic systems dominating the technological industry. This results in increased demands for miniaturized systems with low power consumption and increased capabilities. In particular, applications such as Internet-of-Things (IoT) require the development of complex wireless communication systems with ultra low power consumption. With the scaling of transistor lengths, however, circuit design is becoming increasingly cumbersome, which in turn results in error-prone designs and prolonged design-to-tape-out time. To shorten the design cycle, software tools that increase the designer's productivity may provide with a solution. However, analog and RF circuit design has not yet reached the automation levels of digital design, where synthesis tools exist. Therefore, the development and the adoption of automated design tools for RF systems is an open topic that needs to be addressed [1].

RF circuit design is usually based on expert knowledge and a set of approximate closed form equations to select topology and the device sizes. The system specifications that drive the design procedure depend on each target application and usually include competing trade-offs between circuit-block performances. For instance, in the case of the Voltage Controlled Oscillators (VCOs), which are the study of this work, Phase Noise and power dissipation are two competing performances that ought to be minimized simultaneously. VCOs are important components of wireless communication circuits such as transceivers and their design automation has been the study of many works [1], [2]. In this work, we address the problem of finding the optimal trade-off between competing trade-offs of two VCO topologies for given oscillation frequencies.

While formulas for Phase Noise such as the LTV model [3] and Figure-of-Merit definitions [4] can be used to drive a particular design to promising solutions, exploring the whole design space could be very difficult even for an expert designer. In addition, methods that provide a structured heuristic way for LC-VCO optimization or make use of semi-empirical models may prove to be inaccurate. To this end, we adopt a simulation based sizing approach that guarantees accuracy since it uses PDK models and commercial simulators. Parametrized testbenches are simulated in iterations to provide with high-quality estimates for the optimal trade-offs that a particular topology can provide in a given technology node.

By using a software tool that interfaces the Cadence Spectre simulator, we are able to access the simulation results from different testbenches and use them to guide an optimization algorithm. To address the trade-off exploration of different topologies, we argue that a Multi-Objective approach provides with better understanding and quantative results than using FoM definitions. In our case, the popular NSGA-II [5] algorithm was used to find the optimal trade-offs of two LC-VCO topologies for different oscillation frequencies.

The paper is structured as follows. Section II provides an overview of two LC-VCO topologies employed in this work and highlights the difficulties encountered during their design. Section III demonstrates the optimization problem and the automatic sizing procedure. Finally, section IV concludes the paper.

## II. VCO Topology

VCO design, even after selecting a specific topology, is usually time consuming, since there exist many competing specifications. Besides Phase Noise and power consumption, metrics such as tuning range and voltage swing must be carefully considered. With the transistor scaling and as the supply voltages grow smaller, optimal LC-tank design to achieve a high quality factor $Q_{tank}$ is becoming difficult to accomplish. In particular, the use of integrated coils that provide with relatively low $Q_{tank}$ brings about the degradation of Phase Noise or increased power consumption [6].

For example, in cases where low power consumption is the most important specification for a particular application, transistors are biased with relatively small currents. However, this strategy can increase the parasitic elements of MOS devices, thereby degrading the circuit's Phase Noise performance. On the other hand, in cases where low Phase noise is


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the most important design aspect, one should look to achieve high output voltage swings. This, however, results in higher power consumption. Therefore, finding a balance between the specifications of a LC-VCO topology would require extensive design space exploration.

In this paper we address the automatic sizing of two different LC-VCO topologies. These are shown in Figures 1 and 2 and depict a nMOS cross-coupled and a complementary nMOS-pMOS cross-coupled LC-VCO respectively. Both topologies consist of two sub-circuits; an LC tank that determines the oscillation frequency $\omega_0$ and an active sub-circuit that provides with the necessary negative conductivity to compensate for the LC tank losses. In the circuit of Fig. 1, the nMOS pair is responsible for the the negative conductivity, whereas in the one shown in in Fig. 2, the complementary nMOS-pMOS pair compensate the tank losses.

Denoting as $C_{tank}$ and $g_{tank}$ the capacitance and conductivity of the VCO tank, two fundamental equations describe the VCO operation. It is noted that the varactor's capacitance, the parasitic capacitances of the active elements and the capacitive load are included in $C_{tank}$. The frequency of oscillation $\omega_0$ is given by [4]

$$\omega_0 = \frac{1}{\sqrt{L_{tank}C_{tank}}} \tag{1}$$

and describes the frequency of the output differential signal at nodes $V_{outp}$, $V_{outn}$. To achieve oscillation, it must hold [4]

$$g_{active} \geq a \cdot g_{tank}, \tag{2}$$

where $a \in [1.5, 3]$ is a safety margin factor securing the start-up condition. The term $g_{active}$ represents the conductivity of the active sub-circuit. In the case of the nMOS-only LC-VCO, it holds $g_{active} = g_{mn}/2$, whereas in the case of the complementary one $g_{active}$ is equal to $g_{mn}/2 + g_{mp}/2$. Similarly, the conductance of the LC-tank, $g_{tank}$, is computed using the inductor and varactor conductances and is given by

$$g_{tank} = \begin{cases} g_L + g_{var} + \frac{g_{ds,n}}{2}, & \text{nMOS} \\ g_L + g_{var} + \frac{g_{ds,p}}{2} + \frac{g_{ds,n}}{2}, & \text{nMOS-pMOS} \end{cases}.$$

An important characteristic for the VCO is its output signal's spectral purity near the frequency $\omega_0$. Phase Noise is a measure for this quantity. By defining a frequency shift $\Delta\omega$ around the $\omega_0$, one can determine the Phase Noise through [3]

$$\mathcal{L}\{\Delta\omega\} = 10\log\left[\frac{1}{4\Delta^2\omega}\cdot\frac{L_{tank}^2(\omega_0)^4}{V_{tank}^2}\cdot 2K_BT\left(g_L + g_{var} + \gamma\cdot g_{d0}\right)\right]$$

where $g_{d0}$ is the transconductance of drain when $V_{ds} = 0$ , $K_B$ is the Boltzamann constant, T the temperature at Kelvin and $\gamma$ is the excess noise factor.

Both of the topologies handled in this work are complemented using a notch filter [7] to enhance their Phase Noise performance. The objective is to reduce the noise components stemming from the tail current, by cutting-off their second harmonic. In both circuits, $L_{filter}$ and $C_{filter}$ are connected in parallel at the drain of the current source and they are tuned to resonate at $2\omega_0$. In addition, we add a capacitor $C_T$ in parallel with the current source to short high frequency noise components [7].

This modification was implemented in both circuits with a small difference in nMOS VCO, where top biasing is used to lower the common mode voltage at the output node to $V_{DD}/2$ and improve the varactor's tuning range. In addition, another pair of $L_{filter}$, $C_{filter}$ was added to the sources of the nMOS transistors. This is because it provides with high impedance at the source of the cross-coupled transistors and restricts them from loading the tank when in triode region [8].

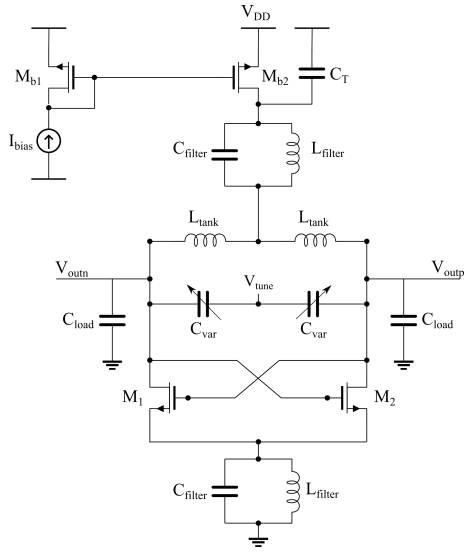


Fig. 1. nMOS cross-coupled LC-VCO

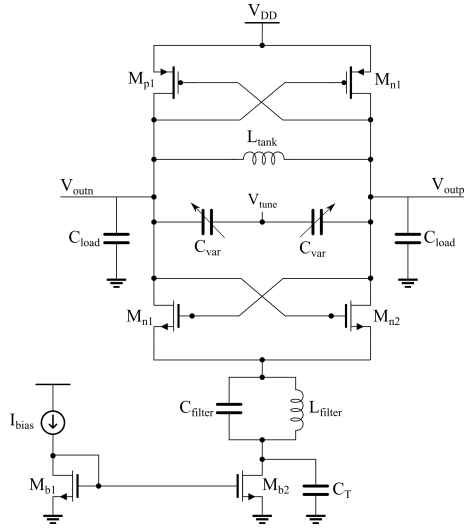


Fig. 2. Complementary nMOS-pMOS cross-coupled LC-VCO

## III. VCO Optimization

In this section we provide with the optimization procedure for both LC-VCO schematics. We consider the general case where the Phase Noise and power consumption of the schematics are equally important.

The sizing of a circuit schematic can be cast as a constrained optimization problem:

$$\begin{aligned} \min \quad & F(\mathbf{x}), \quad \mathbf{x} = [x_1, x_2, \ldots, x_d] \\ \text{s.t.} \quad & g_j(\mathbf{x}) \leq 0, \quad j = 1, \ldots, l \\ & L_i \leq x_i \leq U_i, \quad i = 1, \ldots, d \end{aligned} \tag{3}$$

where vector $\mathbf{x}$ contains the design variables, $L_i$ and $U_i$ are the lower and upper bounds of the $i$-th variable, $\mathbb{S} = \prod_{i=1}^{d}[L_i, U_i]$ is the variable space, $F$ is the objective (fitness) function and $g_j$ is the $j$-th constraint. In our case, the design variables are the transistor widths and lengths, the widths and number of turns of the integrated inductors etc.

To account for both Phase Noise and power consumption, we resort to multi-objective optimization. Here, $F$ is a vector of 2 conflicting functions $F(\mathbf{x}) = [f_1(\mathbf{x}), f_2(\mathbf{x})]$, that correspond to the Phase Noise and power dissipation of the circuit. Minimizing $F$ results in multiple solutions that constitute a Pareto Set (PS). Their mapping to the objective space is called Pareto Front (PF). It should be noted that besides the optimal PS, there exist multiple levels of pareto dominance that can be assigned to a set of candidate vectors $P = [\mathbf{x}_i]_{i=1}^{N}$. By defining the first one to be the optimal PS, the second one is found by removing PS from $P$ and determining the optimal non-dominated solutions from the resulting set. The process is repeated until all samples in $P$ are assigned to a dominance level.

In reality, a fundamental design constraint for a VCO is its output signal oscillation frequency. In our case therefore, the only constraint that applies is $g_1(\mathbf{x}) \leq 0$ and corresponds to the deviation of the output signal's frequency from the desired $\omega_0$. In particular, $g_1(\mathbf{x}) = |\omega_0 - \omega_{osc,output}| - \epsilon$, where $\epsilon \geq 0$ is a relaxation term that depends on the desired $\omega_0$ and $\omega_{osc,output}$ represents the actual output signal frequency of the parametrized VCO schematic.

To solve the multi-objective optimization problem, we use the popular Non-dominated Sorting Genetic Algorithm (NSGA-II) [5]. This is a stochastic, population based method for black-box optimization problems. It uses a set of variable vectors, referred as individuals, to explore the design space and yield pareto optimal solutions. The optimization starts from an initial set of individuals (parents) that are randomly sampled from the variable space $\mathbb{S}$ using Latin Hypercube Sampling (LHS). These variable vectors are simulated and then, a new set of individuals are generated by using stochastic crossover and mutation operators. These operators are responsible for the variation of the individuals and the exploration of the design space. The resulting individuals, which are referred as offspring, are simulated to acquire their fitness and constraint function values. Finally, NSGA-II proceeds with an exploitation step by selecting among the combined groups of offspring and parents using non-dominated sorting. This involves ranking the offspring and parent individuals according to their pareto dominance level. Individuals that belong in the same level are sorted according to their crowding distance [5], which is a metric for the variety that they provide in the objective space. The aforementioned process is repeated for a predefined number of iterations and the individuals of the last one constitute the PS estimate of the algorithm. Fig. 3 provides an illustration of the NSGA-II operation.

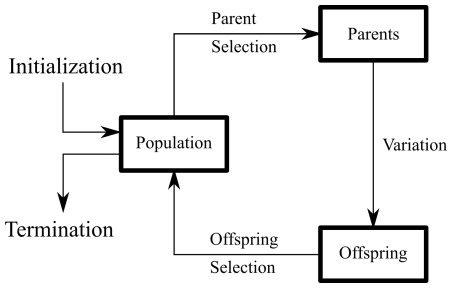


Fig. 3. A graphical depiction of the NSGA-II operation

To obtain the simulation results that will be used as the constraint and fitness values for the NSGA-II individuals, we use an in-house tool written in Python. This tool provides an interface to the Spectre simulator and allows the user to define measurements on schematics that are already designed in Cadence Virtuoso. In addition, batched and parallel simulator calls can be run, allowing for more information to be processed in the same time-frame. This is very important in our case, since NSGA-II is a population-based approach, i.e. it requires many simulations to converge to optimal solutions.

Both schematics are designed using a TSMC 90nm PDK. For each one of them, a single testbench is used to acquire Phase Noise, oscillation frequency and power dissipation outputs. The allowable ranges for the design variables, which are identical for both topologies, are given in Table I.

First, we set the desired $\omega_0$ to be $2\pi \cdot 5$GHz. For the NSGA-II algorithm, the population count is $100$ and the generations are $150$. On an $8$ core machine, the optimization tool approximately 1.5 hours to complete for each circuit. The resulting PFs are shown in Fig. 4.

As expected, higher power consumption provides better Phase Noise performance for both circuits. By comparing the PFs, it is seen that the complementary cross-coupled topology achieves better Phase Noise and power consumption trade-off for relatively low biasing currents. When higher current consumption is acceptable, the nMOS-only topology is preferable. In fact, nMOS-only topologies provide with larger output voltage swings compared to the complementary ones, leading to better Phase Noise performance, when enough current is available [9]. Using Fig. 4, we are able to determine $5$mA as the minimum current threshold for using nMOS-only topology.

The above experiment is repeated once more, for the case of $\omega_0 = 2\pi \cdot 2.4$GHz. The NSGA-II hyperparameters are the same as before, and the allowable parameter ranges remain as

TABLE I
SPECIFICATIONS FOR THREE STAGE AMPLIFIER

| Design Variable | Units | Range |
|---|---|---|
| $W_{nmos}$ | um | $[2, 80]$ |
| $L_{nmos}$ | nm | $[100, 200]$ |
| $I_{bias}$ | mA | $[1, 10]$ |
| $W_{tail}$ | um | $[2, 80]$ |
| $L_{tail}$ | nm | $[100, 200]$ |
| $C_T$ | pF | $[0.5, 6]$ |
| $C_{filter}$ | pF | $[0.15, 1]$ |
| $L_{filter}$ Inner Radius | um | $[1, 80]$ |
| $L_{tank}$ Inner Radius | um | $[10, 60]$ |
| $L_{filter}$ Num of turns | – | $[1, 5]$ |
| $L_{tank}$ Num of turns | – | $[1, 5]$ |
| $C_{var}$ Num of fingers | – | $[2, 32]$ |
| $C_{var}$ Num of groups | – | $[1, 5]$ |

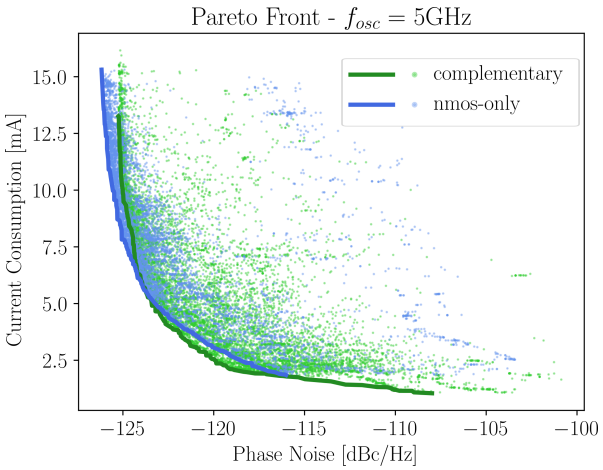


Fig. 4. Acquired Pareto Fronts for both LC-VCO topologies, with $f_{osc}$ = 5GHz

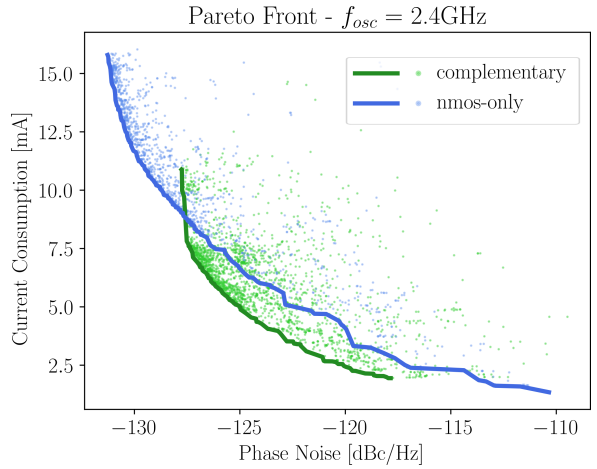


Fig. 5. Acquired Pareto Fronts for both LC-VCO topologies, with $f_{osc}$ = 2.4GHz

given in Table I. The optimization took 1.5 hours to complete and the resulting PFs are given in Fig. 5.

In this case, the difference between the two topologies is more evident, with the complementary one being even more preferable. Qualitatively, this can be explained as follows; in lower oscillation frequencies, the inductance and capacitance of the tank for a given biasing current need to increase. This requires higher negative impedance from the active sub-circuit to achieve oscillation, which is more easily attainable from the complementary topology. Quantitatively, using the optimization results from Fig. 5, the complementary topology is preferred for current consumption below 9mA. It is worth noting that the above results hold for the PDK used in this study, and the actual PFs may differ from one technological node to another.

## IV. CONCLUSION

In this work, the use of optimization algorithms for trade-off exploration and automatic sizing between two LC-VCO topologies was given. By using a tool that enables running simulations on parametrized testbenches and accessing their outcomes, the attainable performances of the topologies studied were discovered and quantitative comparisons were made.

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