Design of CMOS Low-Power, Low-Noise, Chopper Stabilized, Low Dropout Voltage Regulator and Bandgap Reference

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***Abstract*—This work presents a low-power, low-noise capacitor-less low dropout regulator targeting noise sensitive integrated circuit applications. Designed and simulated in TSMC 90 nm CMOS technology, it supports an operating voltage range of $1.8-3.3$ V $\pm 5\%$ and features a programmable output voltage range of $0.9-1.5$ V. Capable of delivering 1 mA, it achieves a worst case PSRR of 25 dB at high frequencies, while its output noise, with the help of a chopper-stabilized error amplifier, does not exceed $-112\ dBV/\sqrt{Hz}$ at 1 mHz, and $-145\ dBV/\sqrt{Hz}$ at 10 Hz, while consuming only $70\ \mu$A. A bandgap reference is also designed achieving a reference of 700 mV with only $21.67 ppm/^oC$.**

***Index Terms*—low-noise LDO, current mirror amplifier, current-mode bandgap reference, chopping, PSRR, CTAT, PTAT**

I. Introduction

With the rapid development of integrated circuits (ICs) more and more systems are integrated in the same chip. For example, noisy circuits such as digital have to coexist with other sensitive circuits like LNAs without the former interfering with the desired operation of the latter. Therefore, each subsystem has to be isolated as much as possible from the common power supply. This can be achieved by the use of local voltage supplies, which in the field of ICs, predominantly, are provided from low dropout voltage regulators (LDO). Many LDO architectures have been developed for increasing the Power Supply Rejection Ratio (PSRR) such as Q-reduction, feed-forward ripple-cancellation, etc [1], [2]. However, the continuous scaling of devices in modern fabrication processes allows the use of lower supply voltages. This results in the reduction of the signal-to-noise ratio. In some applications such as RF-circuits the lowest possible noise of the LDO is just as important as the PSRR [3]. Therefore, the need for designing low-noise LDOs arises.

In this work, a low-power, low-noise LDO along with a bandgap reference (BGR) are implemented in TSMC 90 nm CMOS technology, using an external supply that ranges between 1.8 V to 3.3 V$\pm 5\%$. The LDO features a programmable regulated output of: 0.9 V, 1.1 V, 1.3 V and 1.5 V, while using 700 mV as a reference.

This paper is organized as follows. The internal structure of the LDO is presented in section II, while the bandgap voltage reference is described in section III. Section IV presents the combined simulation results of both circuits followed by our conclusions in section V.

II. LDO

A simplified block diagram of the proposed LDO is shown in Fig.(1). It consists of a NMOS pass-device, a voltage-reference, a resistive feedback-network and an error amplifier (EA) [4], [1]. The pass device is a native NMOS as it provides high PSRR at high frequencies without requiring large gate-to-source voltages. As a result the LDO can achieve a lower dropout voltage and thus greater efficiency in comparison with one using a conventional NMOS pass device. An LDO constitutes a closed-loop system with series-shunt feedback configuration [4], [5]. In order to stabilize the system a compensation capacitor is added. This results in the formation of two poles in the system (assuming the EA is a first order system), with the dominant pole being defined by the RC time constant found at the EA's output, while the second pole from the RC time constant located at the LDO's output.

A. Feedback-Network

The feedback network is a voltage divider which along with the voltage reference determines the regulated output voltage:

$$V_{out} = (1 + \frac{R_2}{R_1}) \cdot Vref. \tag{1}$$

In order to control the regulated voltage resistor R_1 is made adjustable. This is implemented by splitting R_1 into several smaller segments. NMOS switches are inserted between certain intermediate nodes of R_1 and ground. When each switch is activated a corresponding portion of R_1 is shorted to ground and hence, its total resistance is varied. To support four different output voltages three switches are used, which are controlled digitally from three bits, respectively.

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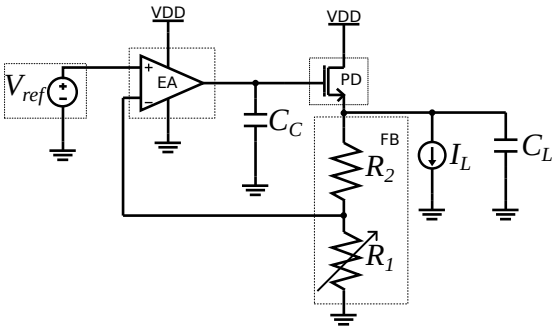

Fig. 1. Architecture of the designed LDO.

B. Error Amplifier

The internal structure of the error amplifier (EA) is presented in Fig.(2). It is a single stage amplifier, which is desirable in terms of simplicity and system dynamics. Moreover it consists of a current mirror operational transconductance amplifier (OTA), employing wide swing cascode current mirrors to achieve high output impedance, while using minimum voltage headroom. This ensures adequate low frequency gain and hence, satisfactory PSRR [4]. The differential pair is implemented with PMOS transistors in order for the OTA to accommodate a reference of 700 mV at its input. The output impedance of the OTA is given by:

$$R_{out} = R_{op}||R_{on}, \tag{2}$$

where $R_{on} = (1 + g_{m10} \cdot rds_6) \cdot rds_{10}$, $R_{op} = (1 + gm_{14} \cdot rds_{12}) \cdot rds_{14}$ and its DC gain is given by [4]:

$$A_v = g_{m1} \cdot R_{out}. \tag{3}$$

To achieve a thermal noise of only $-145\ \frac{dBV}{\sqrt{Hz}}$ at the LDO's output, the quiescent current of each branch is set to 10 μA, while current consumption of the resistive feedback network is 40 μA when the output voltage is 1.5 V. It is worth noting that the cascode impedances R_{op} and R_{on} at the OTA's output form a voltage divider with respect to the small signal noise present at the supply rail. This R_{op} has to be greater than the R_{on} in order to attenuate the signal at the output of the opamp and thus improve the PSRR. However, if R_{on} is much smaller than the R_{op} then the smaller resistance dominates the parallel combination and thus the DC gain and the PSRR are reduced.

The EA along with the voltage reference has the most noise contribution [1]. In order to eliminate any low frequency errors of the OTA, such as flicker noise and offset drift, a current-mode chopping technique is implemented inside the OTA design as it is shown in Fig.(2). The implementation is done with the use of three polarity reversing switches, also known as choppers. Since the input common mode voltage level of the OTA is 700 mV (coming from the bandgap reference), the input chopper CH1 is implemented with transmission gate switches. However, the remaining two choppers CH2 and CH3, are implemented with PMOS and NMOS switches respectively [3], [6]. It is worth noting that in these choppers two dummy-switches, half the size of the main switches have been placed in series before and after the main switches in order to minimize charge-injection [7], [6], [4], [8]. Current-mode chopping is preferable due to the fact that the OTA has high effective gain at the chopping frequency and it also allows the use of a single-ended output. The $1/f$ corner frequency is found close to 90 kHz. In order to modulate all of the flicker noise content the chopping frequency is set to 100 kHz [6]. Furthermore, the dominant pole at the amplifier's output acts as a low-pass filter, which helps to suppress the chopping ripple.

TABLE I
PSRR VALUES OF THE LDO FOR DIFFERENT OUTPUT IMPEDANCES OF THE ERROR AMPLIFIER.

R_{op} (MΩ)	R_{on} (MΩ)	DC PSRR (dB)
252.6	107.3	73
257	163.8	75
258	257	78.65
172.6	279.1	76.7
621.5	422.9	84.57

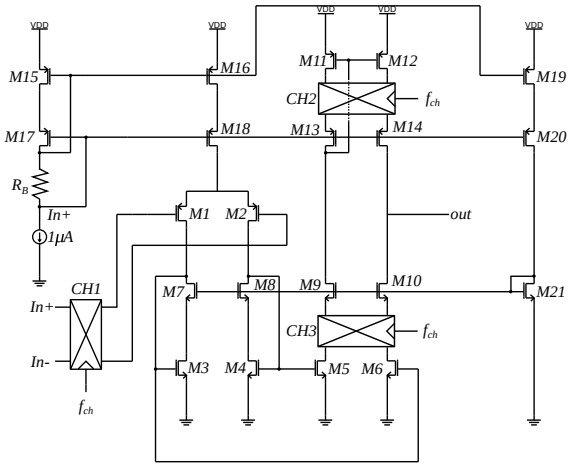

Fig. 2. Schematic of the designed current-mirror OTA.

III. BANDGAP REFERENCE

A. Design

The design of the bandgap reference (BGR), which is shown in Fig.(3) is based on the "Banba" architecture [9] or namely current-mode BGR. The choice of this topology allows reference voltages of less than 1 V to be generated. The operating principal of this circuit is as follows. Resistor R_2 implements a CTAT current, which is given by the following equation [5], [9]:

$$I_{2b} = \frac{V_{BE1}}{R_2}, \tag{4}$$

where $R_1 = R_2$, V_{BE1} is the absolute value of the emitter-base voltage of PNP transistor Q1. On the contrary resistor R_3 implements a PTAT current, that can be derived as follows:

$$I_{2\alpha} = \frac{V_T ln(N)}{R_3}, \tag{5}$$

where V_T is the thermal voltage and N is the size ratio of transistors Q_1 & Q_2. These two currents are added together

resulting in a 8 μA current, which remains constant with respect to temperature. This current is then copied by transistor $M3$ and finally generates a voltage drop of 700 mV across resistor R_4; the required reference voltage. The BGR's output can be described by the following expression [5]:

$$V_{REF} = \frac{R_4}{R_2} \cdot V_{BE1} + \frac{R_4}{R_3} \cdot V_T \cdot ln(N). \quad (6)$$

The bjt transistors have a size ratio of $N = 24$ for lower noise [10]. Furthermore, a start-up circuit is required to ensure the BGR does not remain in the undesirable zero-current state during startup. The same EA as in the LDO case is used due to its low noise. Usually a low-pass RC filter is connected at the output of a BGR in order to reduce its integrated noise. However, a large resistor placed in series with the output would introduce additional thermal noise. Therefore, it is preferable to use only a capacitor at the output. This capacitor filters out the chopping ripple, while at the same time improves the high-frequency PSRR of the BGR. Moreover the combination of this capacitor (C_L) and R_4 forms a low-pass filter and thus the total output noise is reduced.

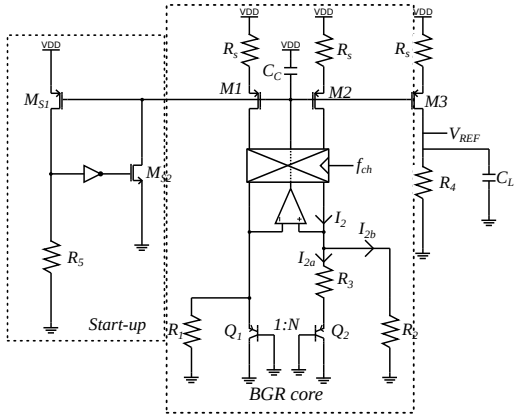

Fig. 3. Schematic of the designed low-voltage bandgap reference.

B. Noise Reduction

When pairing the BGR core with our low noise EA, it is observed that the EA has negligible contribution on the overall noise of the BGR, regardless of whether chopping in the EA is enabled or not. This indicates that the main noise contributors are the current-sources M1, M2 and M3. A series of different approaches are examined and combined in an attempt to reduce their impact. Initially the length of the current sources is increased to 4 μm (see V2 in Fig.(8)) and source-degeneration resistors are added to further reduce their effective transconductance (see V3 in Fig.(8)). Last but not least a chopper is introduced, to chop the currents of M1 and M2 (see Fig.(3)) to further suppress their noise.

IV. Simulated Results

A. LDO

The LDO is simulated across all possible process corners Typical, Slow, Fast, for each device, at the lowest supply voltage 1.8 V $\pm 5\%$ and at three different temperature points : -50^oC , 27^oC and 150^oC . Furthermore, three different current loads are considered : zero-load, 100 μA, 1 mA, and three different bypass capacitances : 50 pF, 100 pF, 200 pF. The noise reduction achieved through chopping is illustrated in Fig.(4). Overall, at 1 mHz the output referred spot noise does not exceed -112 $dBV/\sqrt{Hz}$, while at higher frequencies, white noise is -145 $dBV/\sqrt{Hz}$. At the typical case a DC PSRR of 84 dB is measured while at 1 MHz it decreases to 26 dB. The PSRR results across selected corners are illustrated in Fig.(5). The behavior of the LDO during line and load transients is presented in Fig.(6). In this simulation, the supply voltage initially rises to 2.5V and then is abruptly increased and decreased by 30% in 0.5 μs, while the load current is varied, initially from 0 to 100 μA and then from 100 μA to 1 mA in 1 μs. Output voltage spikes do not exceed 31 mV, considering the lowest bypass capacitance value of 50 pF. At the lowest supply voltage of 1.71 V, for a regulated output of 1.5 V and at maximum load of 1 mA, the LDO's current consumption is less than 70 μA, which translates to an efficiency factor of 81%. A results summary is provided in table II.

B. Bandgap Reference

The BGR is simulated under the same PVT conditions as the LDO. It produces a stable reference of 700 mV achieving a temperature coefficient of 21.67 $ppm/^oC$, while consuming only 68.06 μA. Its temperature dependency is illustrated in Fig.(7). Additional performance metrics, are reported in table III.

TABLE II
Results summary of the LDO across PVT

Parameter	Min	Max
Regulated Voltage	1.297 V	1.3 V
Current Consumption	69.82 μA	69.94 μA
PSRR @ 1 Hz	76.04 dB	86.99 dB
PSRR @ 1 MHz	25.39 dB	27.89 dB
Noise @ 1 mHz ($dBV/\sqrt{Hz}$)	-127.7	-111.8
Noise @ 1 Hz ($dBV/\sqrt{Hz}$)	-145.6	-141.6
Noise @ 100 kHz ($dBV/\sqrt{Hz}$)	-147.3	-143.2

TABLE III
Results summary of the Bandgap Reference across PVT

Parameter	Min	Max
Current Consumption	52.28 μA	72 μA
PSRR @ 1 Hz	65.06 dB	85.2 dB
PSRR @ 1 MHz	41.72 dB	52.96 dB
Noise @ 1 mHz ($dBV/\sqrt{Hz}$)	-71.84	-71.12
Noise @ 1 Hz ($dBV/\sqrt{Hz}$)	-107.7	-106.9
Noise @ 100 kHz ($dBV/\sqrt{Hz}$)	-138.6	-135.4

V. Conclusions

A low-power, low-noise LDO and a sub-1V BGR are designed and simulated. Also, a chopped OTA is designed and evaluated, which is used as an EA in both circuits. When

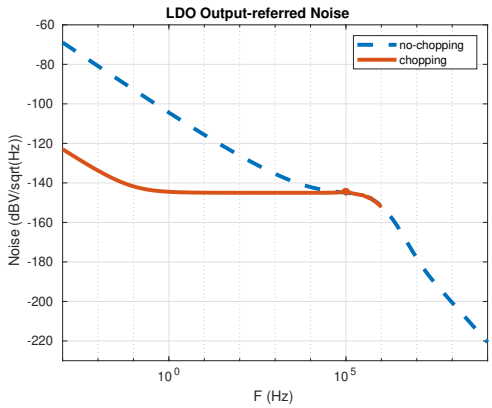

Fig. 4. Typical output noise spectral density with and without chopping. Conditions : 1.71 V supply voltage, 1.3 V regulated output voltage and 1 mA load current.

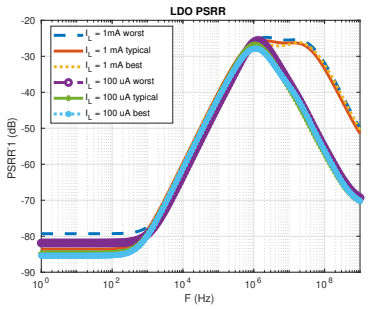

Fig. 5. $PSRR^{-1}$ graphs of the LDO. Conditions: 1.71 V supply voltage. Two different scenarios are examined: maximum load (1 mA) & $C_L = 50$ pF and minimum load (100 μA) & $C_L = 200$ pF.

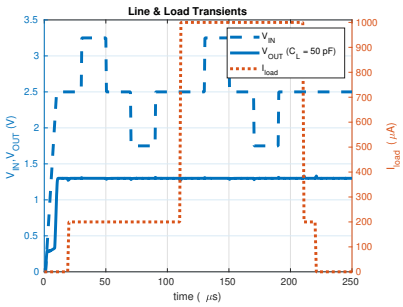

Fig. 6. LDO line and load transient simulation for the typical case at 27^{o}C.

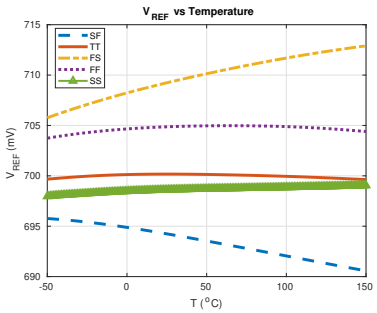

Fig. 7. BGR output voltage in function with temperature.

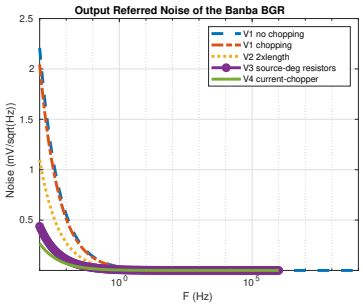

Fig. 8. BGR's output referred noise for each modification.

chopping is employed, a significant reduction in noise is observed at the LDO's output. However, in the case of the BGR, the EA is not the main noise contributor. Therefore, additional circuit modifications and design approaches, such as Gm-reduction, source degeneration and current source chopping are implemented and examined with each one presenting incremental improvements. The designed LDO is appropriate for low-noise applications such as RF, high precision ADCs and biomedical front-ends.

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REFERENCES

[1] J. Torres, M. El-Nozahi, A. Amer, S. Gopalraju, R. Abdullah, K. Entesari, and E. Sanchez-Sinencio, "Low drop-out voltage regulators: Capacitor-less architecture comparison," *IEEE Circuits and Systems Magazine*, vol. 14, no. 2, pp. 6–26, 2014.

[2] E. Sánchez-Sinencio, "Low drop-out (LDO) linear regulators: design considerations and trends for high power-supply rejection (PSR)," *Texas A & M University*, 2010.

[3] W. Oh, B. Bakkaloglu, C. Wang, and S. K. Hoon, "A CMOS Low Noise, Chopper Stabilized Low-Dropout Regulator With Current-Mode Feedback Error Amplifier," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 3006–3015, 2008.

[4] K. W. M. Tony Chan Carusone, David A. Johns, *Analog Integrated Circuit Design*. John Wiley & Sons, 2012.

[5] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. McGraw-Hill, 2017.

[6] K. A. A. M. Rong Wu, Johan H. Huijsing, *Precision Instrumentation Amplifiers and Read-Out Integrated Circuits*. New York Heidelberg Dordrecht London: Springer, 2013.

[7] Mingliang Liu, *Demystifying Switched Capacitor Circuits*. 30 Corporate Drive Suite 400 Burlington MA 01803 USA Linacre House Jordan Hill Oxford OX2 8DP UK: Elsevier, 2006.

[8] Johan Huijsing, *Operational Amplifiers Theory and Design*. Springer International Publishing Switcherland 2017: Springer, 2017.

[9] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A cmos bandgap reference circuit with sub-1-v operation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, 1999.

[10] R. Nagulapalli, R. K. Palani, and S. Bhagavatula, "A 24.4 ppm/°c Voltage Mode Bandgap Reference With a 1.05V Supply," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 4, pp. 1088–1092, 2021.