Implementation of Multi-Step Look-Ahead Sigma-Delta Modulators Using IC Technology

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***Abstract*—A hardware implementation of Multi-Step Look-Ahead Sigma-Delta Modulators (MSLA SDMs) in IC technology is presented. MSLA SDMs offer superior performance than conventional single-bit SDMs for a multitude of applications relying on single-bit signal representation. However, traditional look-ahead SDMs have very high algorithmic complexity. MSLA SDMs overcome this problem by transforming the minimization problem associated with traditional look-ahead SDMs. A proof-of-concept IC implementation of a specific MSLA SDM is discussed and compared to a conventional single-bit SDM in terms of performance and hardware complexity. It is demonstrated that MSLA SDMs are a viable alternative to conventional single-bit SDMs when better performance with moderate additional hardware complexity are required.**

***Index Terms*—Sigma-delta, noise shaping, single-bit quantization, modulator, all-digital, look-ahead, IC**

I. Introduction

Sigma-Delta modulators (SDMs) convert analog or digital multi-bit signals to few-bit or single-bit ones using oversampling to shape the quantization noise outside the useful signal frequency band [1]. They are an important component of many electronic systems. Single-bit quantization is required by a number of applications such as all-digital frequency synthesizers and transmitters [2], [3]. Furthermore, single-bit signal representation is inherently linear, since there can be only gain and offset errors. However, single-bit SDMs are less stable than multi-bit ones, leading to lower in-band signal-to-noise-and-distortion ratio (SNDR).

Look-ahead SDMs [4] allow for improved SNDR while retaining single-bit quantization. The main drawback of look-ahead SDMs is their increased hardware complexity in comparison with conventional SDMs. Multi-Step Look-Ahead (MSLA) SDMs have been proposed to overcome this problem and enable realtime operation.

II. The MSLA SDM

The MSLA SDM principle of operation is based on the minimization of a cost function, which is a measure of the in-band quantization error of the current and k future outputs. The frequency band within which the quantization error is minimized is determined by the comparison filter G. It is related to the NTF via $G(z) = \big(1-NTF(z)\big)/NTF(z) = \sum_{i=1}^{\ell} b_i z^{-i} / \big(1+\sum_{i=1}^{m} a_i z^{-i}\big)$, where b_i, a_i are the filter coefficients. The cost function is $D(\mathbf{v}) = \sum_{j=0}^{k} |x_{n+j} + e_{n+j} - v_j|^2$, where $\mathbf{v} = [v_0 \ v_1 \ \cdots \ v_k]$, $v_j \in \{\pm 1\}$ is the minimizing variable vector, x_n and e_n are the input and comparison filter output samples respectively at discrete time instant n. The output of the modulator at time instant n is the first element v_0 of the sequence $\mathbf{v}$ that results in the least cost, i.e.

$$y_n = \underset{v_0 \in \{\pm 1\}}{\arg\min} \left(\min_{v_1, v_2, \ldots, v_k \in \{\pm 1\}} D_n(\mathbf{v}) \right). \tag{1}$$

Using (1) requires an exponential increase in the number of operations for the determination of each output sample as k grows. In [5] it is shown that an equivalent MSLA SDM system description exists. The corresponding equation giving the MSLA SDM output is $y_n = f(u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n})$, where

$$f(\mathbf{u}) = \underset{v_0 \in \{\pm 1\}}{\arg\min} \left(\min_{\substack{v_1, v_2, \ldots, v_k \in \\ \{\pm 1\}}} \sum_{j=0}^{k} \left| u_{j,n} - \sum_{i=0}^{j} c_{j,i} v_{j-i} \right|^2 \right), \tag{2}$$

$\mathbf{u} = [u_{,n} \ u_{k-r+1,n} \ \cdots \ u_{k,n}]$ and $u_{j,n} = \sum_{i=0}^{j} c_{j,i} x_{n+j-i} + \sum_{i=j+1}^{j+\ell-1} c_{j,i} \left(x_{n+j-i} - y_{n+j-i}\right) + \sum_{i=0}^{m-1} d_{j,i} e_{n-i}$, $k-r \leq j \leq k$. Here, $u_{j,n}$ are the loop filter outputs, e_n is the comparison filter output and $f(\mathbf{u})$ is the multi-input quantizer function. Coefficients $c_{j,i}$ and $d_{j,i}$ are constant and depend on the comparison filter G. The equations giving their values are found in [5].

The important fact is that (2) does not depend on discrete time n. So, in an MSLA SDM hardware implementation it can be pre-calculated and stored in a look-up table (LUT). Therefore, only the loop filter outputs $u_{j,n}$ need to be calculated in real-time.

III. IC Implementation of MSLA SDMs

We propose a hardware architecture for MSLA SDMs and a proof-of-concept implementation in TSMC 90nm 1.0V low Vt IC technology. A band-pass MSLA SDM with $k = 3$ look-ahead steps and an 8-th order NTF with 128 oversampling ratio (OSR) is considered. The proposed architecture is comprised of blocks that calculate the loop filter outputs (Fig. 1) and a block implementing the quantizer as a LUT (Fig. 2).

The LUT complexity depends on the bit width its inputs. Significant complexity reduction is possible by observing that when some inputs are greater or less than certain values, the output of the quantizer remains the same. So, these input values do not need to be stored in the LUT. Furthermore, since (2) is an odd function, LUT size is reduced by a factor of 2.

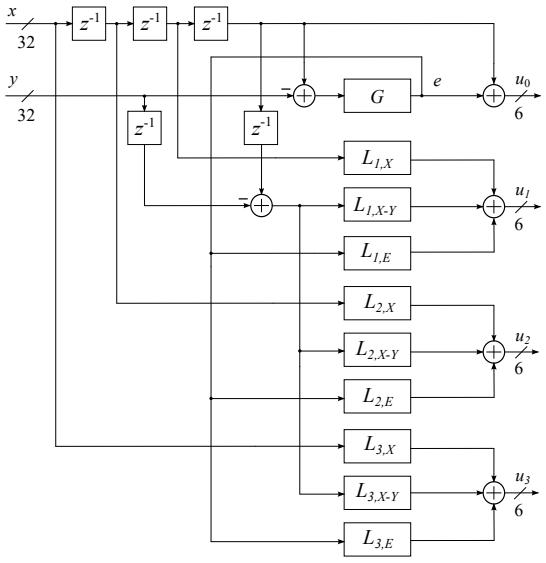

Fig. 1. The designed MSLA SDM loop filter architecture.

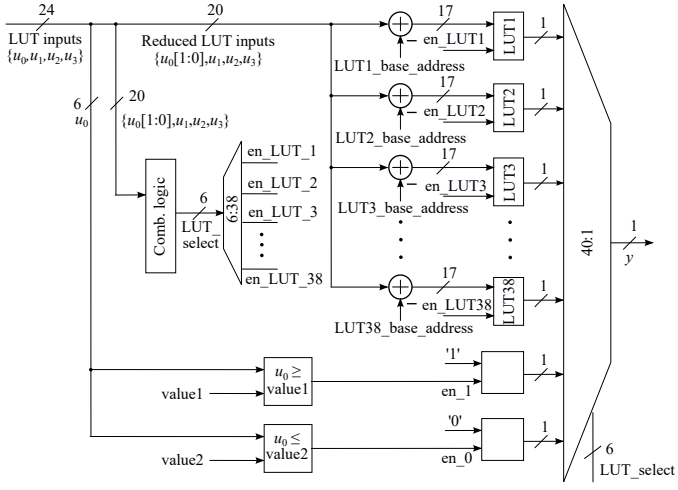

Fig. 2. The designed MSLA SDM LUT architecture.

From extensive simulations it is concluded that typically 6-7 bits are enough for the representation of each of the quantizer inputs [2]. The LUTs are partitioned into 38 sub-LUTs, reducing the initial 24 address bits to 17 for each sub-LUT. This facilitates routing and optimizes power consumption since only one sub-LUT is enabled at any moment.

The 4 loop filters are implemented using 32-bit fixed-point arithmetic. Each loop filter except for the one corresponding to $j = 0$ consists of 3 FIR (finite impulse response) filters with orders j, $\ell - 2$ and $m - 1$. An additional IIR (infinite impulse response) filter is used to calculate e_n. Careful selection of the bitwidth used for the IIR filter is needed to avoid instability due to quantization error accumulation.

For comparison, we also designed a conventional single-bit SDM with the same OSR and NTF order. Its NTF needs to have lower out-of-band gain to maintain stability. The performance advantage of the designed MSLA SDM is demonstrated

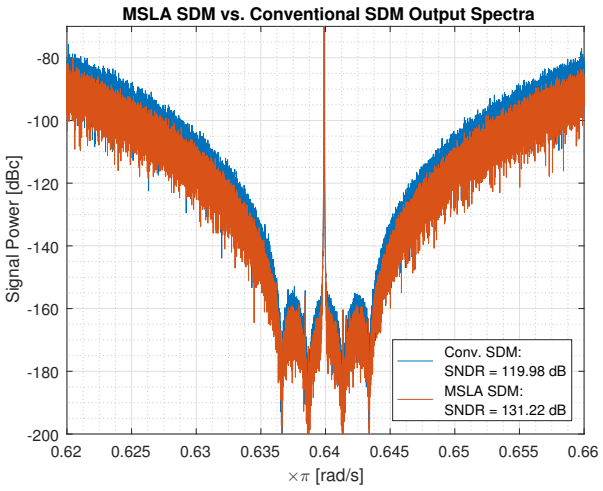

Fig. 3. MSLA SDM vs. conventional single-bit SDM output power spectra.

TABLE I
MSLA SDM VS. CONV. SDM IC IMPLEMENTATION DETAILS

	MSLA SDM	**Conv. SDM**
Max. output rate [Msamples/s]	75.8	500.0
Standard cells [# number]	123,610	30,157
Area (core) [μm^2]	953,543.6	206,310.5
Power (@ Max. rate) [mW]	117.31	115.4

in Fig. 3, which shows the output power spectra of both modulators. The input is a sinusoidal signal with amplitude 0.25 and frequency $f = (2621/2^{13})f_{\text{clk}}$, generated by a 24-bit output direct digital synthesizer (DDS). The MSLA SDM has an in-band SNDR of 131.22 dB compared to 119.98 dB for the conventional SDM.

Table I summarizes the results of the MSLA and conventional SDM IC implementations including the DDS after place and route. The designed MSLA SDM generates its output at a rate of 75.8 Msamples/s. The MSLA SDM core occupies an area of 953,543.6 μm^2, whereas the conventional SDM core occupies 206,310.5 μm^2. At their highest possible output rate both modulators exhibit similar power consumption. These results show that the MSLA SDM hardware complexity is not significantly higher than that of the conventional SDM and allows for realtime operation.

REFERENCES

[1] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, S. V. Kartalopoulos, Ed. John Wiley & Sons, Inc., 2005.

[2] C. Basetas, N. Temenos, and P. P. Sotiriadis, "Wide-band frequency synthesis using hardware-efficient band-pass single-bit multi-step look-ahead sigma-delta modulators," in *IEEE Int. Freq. Control Symp. (IFCS) & Europ. Freq. and Time Forum (EFTF)*, Jul. 10–13, 2017.

[3] R.-C. Marin, A. Frappe, and A. Kaiser, "Digital complex delta-sigma modulators with highly configurable notches for multi-standard coexistence in wireless transmitters," *IEEE Trans. Circuits Syst. I*, Jun. 2017.

[4] E. Janssen and A. van Roermund, *Look-Ahead Based Sigma-Delta Modulation*. Springer, 2011.

[5] C. Basetas, T. Orfanos, and P. P. Sotiriadis, "A class of 1-bit multi-step look-ahead Σ-Δ modulators," *IEEE Trans. Circuits Syst. I*, Oct. 2016.