Comparison of two All-Digital Frequency Synthesizers with a Jitter Removal Circuit

Nikos Temenos, Charis Basetas, and Paul P. Sotiriadis
Department of Electrical and Computer Engineering
National Technical University of Athens, Greece
E-mail: ntemenos@gmail.com, chbasetas@gmail.com, pps@ieee.org

***Abstract*—Digital frequency synthesizers are key components in wireless communication systems. Their single-bit output can be achieved by a Sigma Delta Modulator (SDM) which improves the noise shaping characteristics as well as the performance in terms of Signal-to-Noise-and-Distortion Ratio (SNDR). However, hardware implementation in FPGAs limits their overall performance due to undesired jitter effect introduced by the FPGA, which is translated into phase noise. In this work we present the hardware implementation of two all-digital frequency synthesizers based on SDMs which are afterwards corrected by a laboratory circuit for suppressing the jitter effect introduced by the clock reference of the FPGA. Comparison of the Quadrature Homodyne Filter (QHF) and Multiplier-Free QHF (MFQHF) SDM architectures in terms of digital synthesis results, SNDR, sampling rate and jitter-free spectrums are provided to demonstrate their capabilities in order to consider them as viable choice for digital frequency synthesis.**

***Index Terms*—Direct digital synthesizer, frequency synthesis, all-digital transmitter, sigma-delta modulation, noise shaping, single-bit quantization, jitter,**

I. Introduction

Modern – day electronic applications tend to completely eliminate analog and mixed – signal parts due to operating disadvantages. In contrast, digital circuits offer smaller area, immunity to process, voltage and temperature variations (PVT), portability, scalability, reconfigurability and faster redesign cycle among many more. In addition, digital frequency synthesizers offer digital accuracy, high resolution frequency control and fast frequency hopping.

Digital to Analog Converting (DAC) is an essential operation for digital systems, including pure digital frequency synthesizers. Multi-bit DACs require analog components and therefore must be avoided when considering digital implementations. Traditional methods for frequency synthesis such as the Pulse Direct Digital Synthesizer (PDDS) as well as the Flying Adder (FA) [1], suffer from spurious tones, high deterministic jitter and high noise floor when dither effects are added [2], [3].

By nature, a Direct Digital Synthesizer (DDS) [4], is a multi-bit processing element and thus requires a multi-bit DAC for the output. However, a single-bit Sigma Delta Modulator (SDM) combined with a DDS, shapes the quantization noise out of the frequency band and provides an efficient solution for single-bit output representation [5]. Furthermore, Single-bit DACs are inherently linear and subject only to gain and offset errors, which can be easily corrected [5].

Field Programmable Gate Arrays (FPGAs) offer a successful solution when hardware implementation of digital systems is required. However, the digital signal at the FPGA output suffers from jitter effect when the carrier frequency becomes considerably high with respect to the frequency of the clock [6]. This effect is translated into phase noise in the analog domain and thus the quality of the signal is slightly reduced. A method to overcome this issue it to apply a jitter removal circuit after the FPGA output, in occasions where noiseless outputs are mandatory, in order to achieve optimum signal performance [6].

In this work, we present two SDM architectures, the Quadrature Homodyne Filter (QHF) and the Multiplier-Free QHF. Both architectures can work as a replacement for conventional SDMs due to their ability to provide overall better maximum output sampling rate as well as Signal-to-Noise-and-Distortion Ratio (SNDR). In addition, our architectures are capable of amplitude, frequency and phase modulation. All the aforementioned properties are significantly important for digital synthesizers and thus both topologies are investigated in detail.

In the next section, the two aforementioned SDM architectures are described and analyzed. In section III, the jitter removal circuit operation is briefly explained. Section IV, provides FPGA synthesis results as well as a spectrum comparison between the simulated output and the spectrum analyzer jitter-free output. Finally, the conclusion is included.

II. All-Digital Frequency Synthesizer Architectures

In Fig. 1 the general architecture of the all-digital frequency synthesizers is shown. The DDS consists of an accumulator and a cosine Look-UP Table (LUT). The accumulator provides phase to the cosine LUT with a value, w, namely the Frequency Control Word (FCW), which also determines the output frequency to be generated by the relation $f_{\mathrm{synth}} = (w/2^n)f_{\mathrm{ref}}$, where f_{ref} is the external reference clock. Afterwards the single-bit SDM shapes the quantization noise of the LUT. Moreover, in our proposed architectures, frequency and/or phase modulation is achieved by adding a modulating signal to the cosine LUT input, while amplitude modulation is possible when the cosine LUT output is multiplied with a modulating signal.

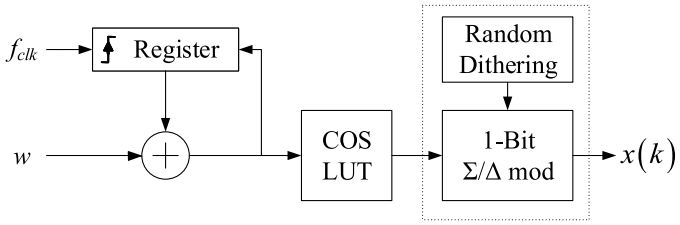

Fig. 1. Pulse DDS (PDDS) with sigma-delta noise shaping.

A. Quadrature Homodyne Filter SDM Architecture

The single-bit SDM mentioned in previous section is depicted in Fig. 2. The signal transfer function (stf) is given by $stf\,(z) = F\,(z)/\big(1 + F\,(z)\big)$. The quantizer is replaced by an additive noise source, where the noise and dither transfer functions (ntf and dtf) are $dtf\,(z) = ntf\,(z) = 1/\big(1 + F\,(z)\big)$. The filter $F(z)$ is band-pass filter. An optional amplified feedback g may be used, but is not necessary in the current work.

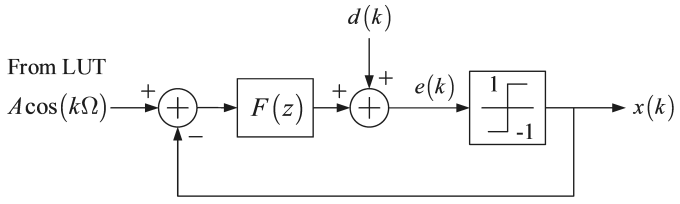

Fig. 2. The single-bit band-pass Σ/Δ modulator.

The band-pass SDM limits the frequency range, meaning that frequencies to be generated are expected to be inside the SDM passband. In the case where a different frequency is desired, the digital filter $F(z)$ coefficients must change. Therefore, filter optimizations used for a specific frequency range are impossible to be applied to another one. The Quadrature Homodyne Filter (QHF) architecture we propose, Fig. 3, addresses this issue.

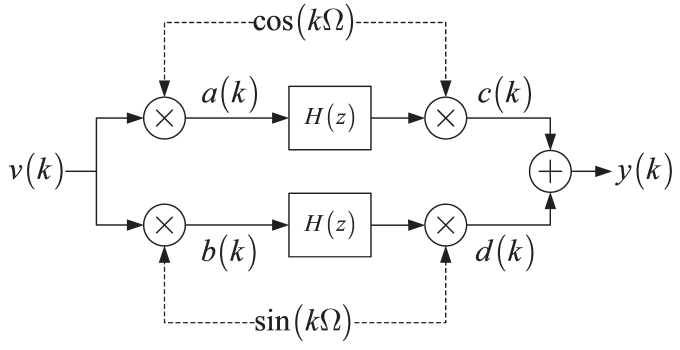

Fig. 3. The Quadrature Homodyne Filter architecture.

The band-pass filter $F(z)$ is implemented by using two identical low-pass filters $H(z)$, while quadrature homodyne down- and up-conversion is used to achieve band-pass frequency response centered at the carrier angular frequency Ω. As a result, apart from filters $H(z)$, the QHF architecture requires four multiplications, an addition and two low-pass filters $H(z)$.

B. Multiplier-Free Quadrature Homodyne Filter Architecture

In order to reduce hardware complexity, the two low-pass filters $H(z)$ can be conveniently chosen to be in powers of 2 or sums of two or three powers of 2. The associated multiplications can be eliminated and replaced by additions and shift operations [7], [8]. The other four multiplications can be eliminated by exploiting first-order approximation of the QHF input and 3-level quantization of the sine and cosine signals as shown in Figs. 3. The Multiplier-Free QHF (MFQHF) architecture is depicted in Fig. 4.

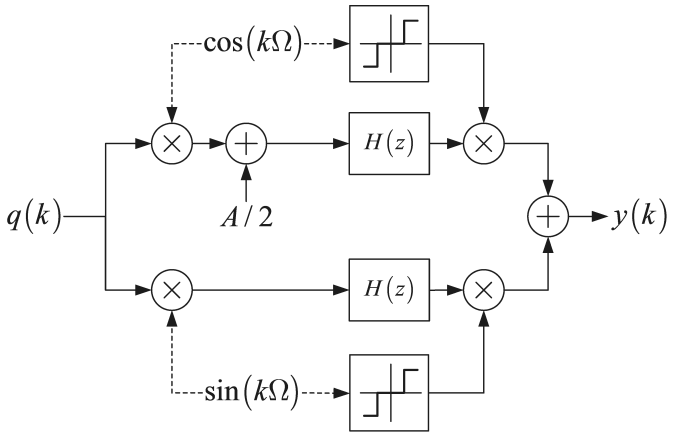

Fig. 4. Quadrature Homodyne Filter Multiplier-Free architecture.

III. Jitter Operation and Laboratory Circuit

In digital design, the abstract RTL design I/Os are translated into D Flip-Flops in the FPGA physical domain. It is expected that the phase noise of the FPGA internal clock signal that triggers the D Flip-Flops, as well as the D Flip-Flop itself as analog component, will both introduce noise [6]. Moreover, in combination with the rest of the FPGA's clock tree, namely fanout buffers and transmission lines, a degradation on the quality of the output signal is certainly evident. Thus, a jitter removal circuit may reduce the above effects, but not completely eliminate them [6].

The complete system architecture is presented in Fig. 5. The components inside the dashed line are referred to the jitter circuit. The clock distributor is fed with an external reference sinusoidal signal that generates two low-jitter clock signals; one responsible for clocking the FPGA and one for triggering the circuit's D Flip-Flop. Frequency and phase of each clock can be configured by programming the clock distributor with an embedded microcontroller. Afterwards, the signal is fed differentially into a buffer which is transformed into single-ended output via a balun.

It should be noted that the jitter circuit should share the same clock reference with the FPGA. Otherwise, the timing between the clock signal and the D Flip-Flop on the circuit

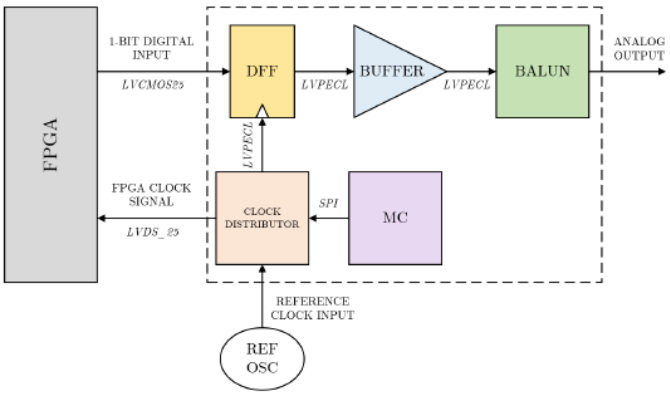

Fig. 5. FPGA and Jitter circuit connection

becomes a mandatory issue. By sampling the data signal near its transition point may lead to sampling error. Therefore, the signal must be sampled at a time where the bit value is not affected by time fluctuations, which is roughly at the middle of the unit interval. Fig. 6 shows the introduced mismatch in the clock.

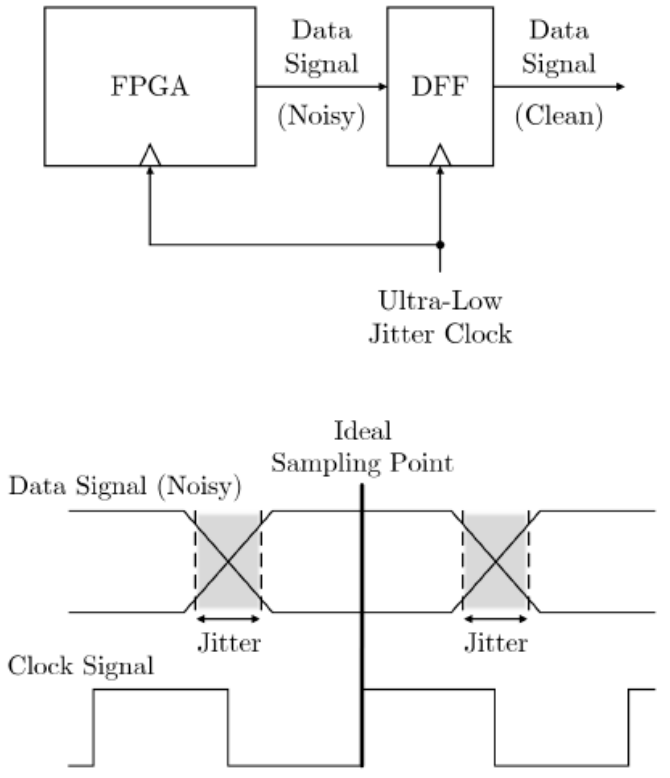

Fig. 6. Reclocking the single-bit data signal

The laboratory jitter circuit is designed to be compatible with the Kintex-7 FPGA KC705 Evaluation Board and is capable of dividing the reference frequency up to 4 times. From technical perspective, the clock signal is provided differentially to the FPGA User SMA Clock Input using LVDS 25. Moreover, the single-bit digital signal is obtained single-ended from a KC705's GPIO SMA Connector and is fed into the D flip-flop using LVCMOS25 signaling. Fig. 7 shows the jitter removal circuit. For additional information about the electronic parts as well as the complete circuit operation, the reader is referred to [6].

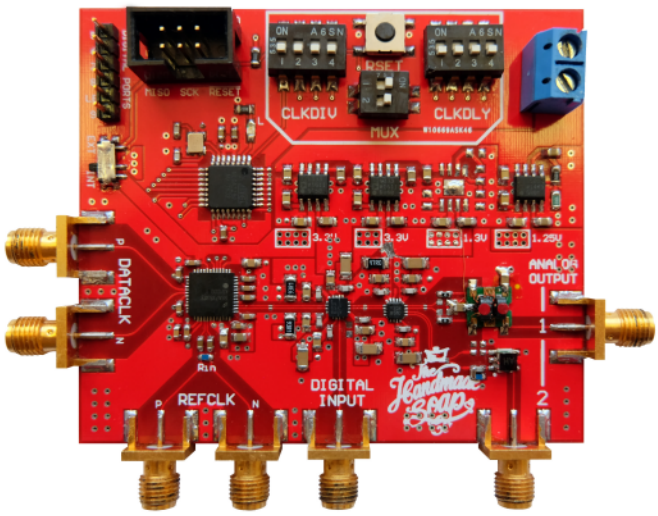

Fig. 7. Laboratory Jitter circuit

IV. Setup, Simulation and Jitter Free Spectrum Results

In order to investigate the performance of the proposed all-digital synthesizers, we developed FPGA implementation for each architecture. As aforementioned, both architectures are capable of direct phase/frequency and amplitude modulation. Reminding that, the FPGA used for implementation is a Xilinx Kintex-7 KC705 Evaluation Board. The parameters that will be mentioned in the next paragraph, apply for both SDM architectures in order to compare their performance.

The selected oversampling ratio (OSR) is 128, with 8-th order NTFs and center frequency of $\omega_0 = 2\pi \cdot 0.64$. Regarding the system input, a DDS was designed with a 13-bit accumulator and a 24-bit output cosine LUT. The reference input signal used in the reclocking jitter removal circuit, is generated by a reference oscillator and has frequency of $f_{ref} = 100MHz$, which is below the operating threshold of the specific FPGA, namely $200MHz$, and an amplitude of 6dBm. As aforementioned, the jitter circuit is capable of dividing the input signal by 4. However, in this case the frequency is divided by 2 and thus the final frequency is given by $F_{out} = (f_{ref}/2) * 0.32 = 16MHz$.

In Table I, the complete utilization of the resources is presented. A quick summary shows that the QHF architecture achieves max output rate of 45.64 MSamples/s with SNR oif 37.66 dB, while the MFQHF achieves 60.26 MSamples/s with SNR of 37.26 dB. Although the overall utilization is slightly reduced in the case of MFQHF SDM, it also provides higher max output rate due to the absence of the multipliers, which is translated into 0 DSP blocks for the FPGA.

TABLE I
QHF AND MFQHF SDM HARDWARE RESOURCES

	QHF SDM	**MFQHF SDM**
Max. output rate [Msamples/s]	45.64	60.26
Slice LUTs [Used / Util.]	6,602 / 3.24%	6,763 / 3.32%
Slice Registers [Used / Util.]	482 / 0.12%	484 / 0.12%
F7 Muxes [Used / Util.]	2,546 / 2.50%	2,546 / 2.50%
F8 Muxes [Used / Util.]	1,154 / 2.26%	1,154 / 2.26%
DSP Blocks [Used / Util.]	10 / 1.19%	0 / 0.00%
Average FPGA Util.	1.86%	1.64%

In order to prove the functionality of the jitter removal circuit, we synthesized both SDM architectures and afterwards we connected the outputs with our laboratory spectrum analyzer. In the next two figures, Fig. 8 and Fig. 9, the synthesized outputs compared to the jitter-free outputs for the MFQHF and QHF architectures respectively are shown.

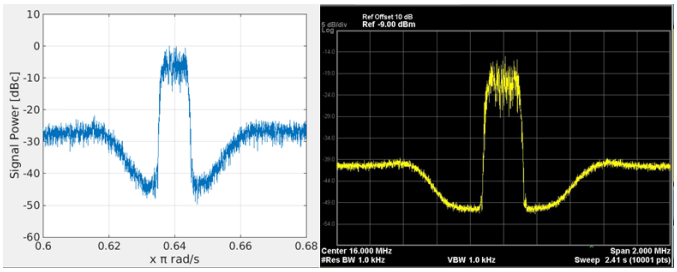

Fig. 8. Left: Digital MFQHF simulated output Right: Digital Jitter-Free output

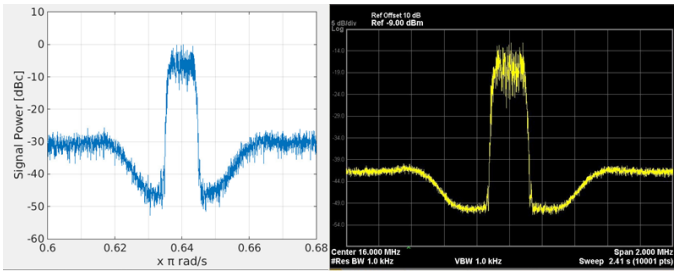

Fig. 9. Left: Digital QHF simulated output Right:Digital Jitter-Free output

V. CONCLUSION

In this work two SDM architectures were introduced and their principal operation was briefly discussed. These topologies provide better noise shaping characteristics than conventional SDMs which is justified by their performance results that are shown as well in detail. Consequently, a laboratory circuit capable of removing the jitter effect, introduced by the clock tree of the FPGA, was implemented and its operation was analyzed. Afterwards, a connection of the jitter circuit with the FPGA output was tested in order to show the necessity for jitter elimination. Finally, it is proven that QHF and MFQHF SDMs, can be essential design techniques and replace traditional SDMs with reduced performance.

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