An Efficient Hardware Architecture for the Implementation of Multi-Step Look-Ahead Sigma-Delta Modulators

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***Abstract*—A hardware architecture for the implementation of Multi-Step Look-Ahead Sigma-Delta Modulators (MSLA SDMs) is presented. MSLA SDMs offer superior performance than conventional single-bit SDMs for a multitude of applications relying on single-bit signal representation. However, traditional look-ahead SDMs have very high algorithmic complexity and their hardware implementation does not allow for real-time operation. MSLA SDMs overcome this problem by transforming the minimization problem associated with traditional look-ahead SDMs. A proof-of-concept FPGA implementation of a specific MSLA SDM is discussed and compared to a conventional single-bit SDM in terms of performance and hardware complexity. It is demonstrated that MSLA SDMs are a viable alternative to conventional single-bit SDMs when better performance with moderate additional hardware complexity are required.**

***Index Terms*—Sigma-delta, noise shaping, single-bit quantization, modulator, all-digital, minimization algorithm, look-ahead**

I. Introduction

Sigma-Delta modulators (SDMs) are used to convert an analog or digital multi-bit signal to a few-bit or single-bit one by exploiting oversampling to shape the quantization noise outside the signal frequency band [1]. They are an important component in many electronic systems, such as data converters (ADCs and DACs) [2], [3], all-digital frequency synthesizers and transmitters [4]–[6], fractional-N PLLs [7], as well as for the generation of the driving signal of switch-mode power amplifiers [8], [9].

A significant portion of the aforementioned systems rely on digital single-bit SDMs. Signal representation with single-bit quantization is inherently linear since there are only two signal levels. Therefore, no errors related to unequal quantization step size due to device mismatches are introduced. There can only be gain and offset errors, which are linear and do not degrade the quality of the signal. However, single-bit quantization has its own limitations. An SDM with a single-bit quantizer is less stable than one with a multi-bit quantizer [1]. This means that the noise transfer function (NTF) of a single-bit SDM should have lower out-of-band gain to remain stable, which translates to lower in-band signal-to-noise-and-distortion ratio (SNDR).

Look-ahead SDMs [10] have been proposed to improve the performance of conventional single-bit SDMs. They achieve that by taking into account future input and output samples for the minimization of the quantization error. This does not imply that future samples are predicted. Instead, the decision on the next output is delayed by the number of look-ahead samples. However, the performance improvement provided by look-ahead SDMs comes at the cost of increased algorithmic and thus hardware implementation complexity. Therefore, traditional look-ahead SDMs do not allow for real-time modulation. To overcome the hardware complexity problems of look-ahead SDMs, Multi-Step Look-Ahead SDMs (MSLA SDMs) were introduced in [11].

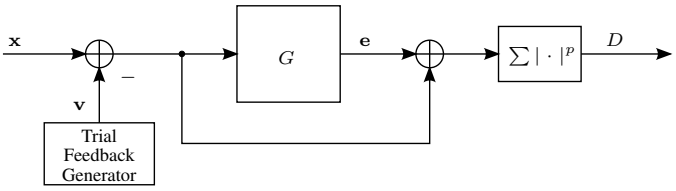

Fig. 1. The MSLA modulator optimization algorithm system diagram.

In the next section a brief introduction to MSLA SDMs is presented, followed in section III by the proposed hardware architecture for the implementation of MSLA SDMs. An FPGA implementation of a specific MSLA SDM based on the proposed architecture is also discussed and compared to a conventional single-bit SDM in terms of performance and hardware complexity. Finally, section IV summarizes the conclusions of the previous sections.

II. The MSLA SDM

MSLA SDMs build upon the quantization error minimization algorithms of typical look-ahead SDMs. In the next subsection the minimization algorithm of MSLA SDMs is described and its design parameters are analyzed.

A. MSLA SDM Quantization Error Minimization Algorithm

The operation of MSLA SDMs is based on an optimization algorithm that minimizes a cost function which is related to the quantization error. The system description of this algorithm is depicted in Fig. 1. As seen in the figure, there are the input sequence $\mathbf{x} = [x_n \; x_{n+1} \; \cdots \; x_{n+k}]$, the trial feedback sequence $\mathbf{v} = [v_0 \; v_1 \; \cdots \; v_k]$, the filter output sequence

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$\mathbf{e} = [e_n \; e_{n+1} \; \cdots \; e_{n+k}]$ and cost D. Variable n is the discrete-time index since the algorithm is repeatedly executed for the determination of each MSLA SDM output y_n. The number of look-ahead steps k is the most important parameter regarding the performance improvement and the hardware complexity. It defines how many input and output samples are considered for the minimization of the quantization error. The elements of the trial feedback sequence $\mathbf{v}$ are either 1 or -1. Filter G is known as the comparison filter and defines the NTF of the modulator through the relation

$$G(z) = \frac{1 - NTF(z)}{NTF(z)} = \frac{\sum_{i=1}^{\ell} b_i z^{-i}}{1 + \sum_{i=1}^{m} a_i z^{-i}}, \tag{1}$$

where ℓ, m are the orders of the numerator and the denominator polynomials respectively.

Cost D is the sum of the partial costs associated with the quantization error of each sample under consideration, i.e.

$$D(\mathbf{v}) = \sum_{j=k-r}^{k} |x_{n+j} + e_{n+j} - v_j|^p \,. \tag{2}$$

Two new parameters are introduced in (2), namely r and p. The first one, r, denotes the number of partial costs that are taken into account for the determination of the total cost. For best performance $r = k$ should be selected [11]. Lower values of r result in inferior performance but allow for less complex hardware implementations. The other parameter, p, determines the norm used for the quantization error cost. The typical coice is $p = 2$ which corresponds to Euclidean distance norm and yields the least quantization error power. However, a value of $p = 1$ can also be used, corresponding to Manhattan distance norm and giving least quantization error absolute value sum. The lower SNDR obtained with $p = 1$ is balanced by the less complex multi-input quantizer implementation associated with selecting $p = 1$.

At each time instance n, 2^{k+1} costs $D_n(\mathbf{v})$ are calculated, one for each possible trial feedback sequence $\mathbf{v}$, $v_i \in \{\pm 1\}$. The output of the modulator at time n is the first element v_0 of the sequence $\mathbf{v}$ that results in the least cost, i.e.

$$y_n = \underset{v_0 \in \{\pm 1\}}{\arg\min} \left(\min_{v_1, v_2, \ldots, v_k \in \{\pm 1\}} D_n(\mathbf{v}) \right). \tag{3}$$

From (3) it is evident that the algorithmic complexity grows exponentially with the number of look-ahead steps k. However, in the next subsection a less complex way to compute y_n is described.

B. The Efficient Form of the MSLA SDM Algorithm

An equivalent system description of MSLA SDMs is the one shown in Fig. 2. The details of how the structure in Fig. 1 is transformed to the one in Fig. 2 are provided in [11]. In this form the modulator is comprised of $r+1$ two-input loop filters and a multi-input single-bit-output quantizer. Now, output y_n

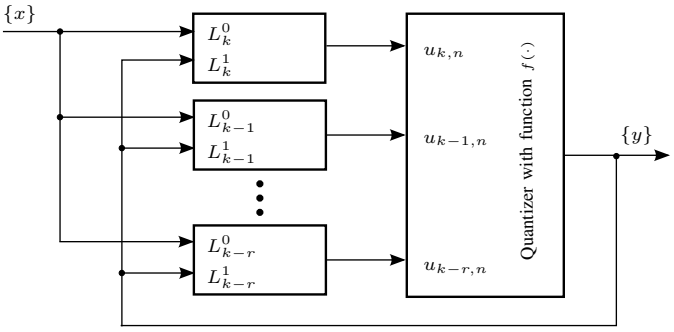

Fig. 2. The MSLA modulator efficient form system diagram.

can be calculated via $y_n = f(u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n})$, where

$$u_{j,n} = \sum_{i=0}^{j} c_{j,i} x_{n+j-i} + \sum_{i=j+1}^{j+\ell-1} c_{j,i} \left(x_{n+j-i} - y_{n+j-i} \right) + \sum_{i=0}^{m-1} d_{j,i} e_{n-i}, \; k-r \le j \le k \tag{4}$$

are the loop filter outputs, $e_n = \sum_{i=1}^{\ell} b_i (x_{n-i} - y_{n-i}) - \sum_{i=1}^{m} a_i e_{n-i}$ is the comparison filter output and $f(\mathbf{u})$, $\mathbf{u} = [u_{k-r,n} \; u_{k-r+1,n} \; \cdots \; u_{k,n}]$ is the quantizer function. Coefficients $c_{j,i}$ and $d_{j,i}$ are constant and depend on filter G or equivalently on the NTF. The equations giving their values are not provided here due to space constraints, but they can be found in [11].

The quantizer function $f(\mathbf{u})$ is described by the minimization problem

$$f(\mathbf{u}) = \underset{v_0 \in \{\pm 1\}}{\arg\min} \left(\min_{\substack{v_1, v_2, \ldots, v_k \in \\ \{\pm 1\}}} \sum_{j=k-r}^{k} \left| u_{j,n} - \sum_{i=0}^{j} c_{j,i} v_{j-i} \right|^p \right). \tag{5}$$

The quantizer output is thus determined by the least p-norm of the quantizer input vector $\mathbf{u}$ from a set of points which depend on the coefficients $c_{j,i}$. Their coordinates in u_j axes are given by $\sum_{i=0}^{j} c_{j,i} v_{j-i}$ for all possible trial feedback sequences $\mathbf{v}$, resulting in a total of 2^{k+1} points in $(r+1)$-dimensional space. For a more thorough analysis the reader is referred to [11].

This method of calculating the MSLA SDM output requires much less arithmetic operations than using (3), resulting in more efficient hardware implementations of MSLA SDMs compared to other look-ahead SDMs. Of course a conventional single-bit SDM remains less complex than an MSLA SDM, but the performance advantages of the latter justify the addtiotional hardware complexity in many applications.

III. Hardware Implementation of MSLA SDMs

Based on the efficient form of MSLA SDMs, we propose a hardware architecture for their implementation. As a proof-of-concept, an example FPGA implementation of a specific MSLA SDM is also presented.

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A. MSLA SDM Hardware Architecture

The hardware architecture of MSLA SDMs is based on the system diagram shown in Fig. 2. The implementation of the $r+1$ loop filters is straightforward and high-level design methods can be used to generate synthesizable HDL code. The multi-input single-bit-output quantizer can be implemented as a look-up table (LUT) for moderate values of look-ahead steps k. This is possible since (5) is a static function in the sense that it does not change with discrete time n. So, the value of $f(\mathbf{u})$ can be precalculated for all possible input values and stored in a LUT.

The LUT complexity depends on the number of bits used for all of its inputs. Significant complexity reduction is possible by observing that when some inputs are greater or less than certain values, the output of the quantizer remains the same. So, these input values do not need to be stored in the LUT. These input value thresholds depend on the parameters of the specific MSLA SDM to be implemented, namely k, r and the NTF. Another observation leading to a reduction of the LUT size by a factor of 2 is that (5) is an odd function. From extensive simulations it has been concluded that 3-4 fractional bits are enough for the representation of each of the quantizer inputs [5]. Typically 2-3 more bits are required for the sign and the integer part of each input.

The other possibility is to implement the quantizer by calculating in real-time the least distance of the input vector from the 2^{k+1} points described at the end of section II. The LUT approach results in minimal delay for the quantizer output generation, allowing for high operation frequencies which is critical for many applications. However, a LUT-based implementation requires more area compared to the least distance calculation approach.

B. MSLA SDM FPGA Implementation Details

As a test-case we have designed an MSLA SDM and implemented it for a Xilinx Kintex-7 KC705 Evaluation Kit target device. The designed band-pass MSLA SDM has an 8-th order NTF with central frequency $0.32f_{\text{clk}}$, uses $k=3$ look-ahead steps with $r=3$ and an OSR of 128. The NTF is designed using the Delta Sigma Toolbox [12] with the maximum possible out-of-band gain that allows stable operation for sinusoidal input signals with amplitude up to 0.4. For our case it is 1.73. Based on system-level simulations we decided to use 3 integer bits (including the sign bit) and 3 fractional bits for the representation of the quantizer inputs with fixed-point arithmetic. This is the lowest number of bits that does not affect the modulator performance.

The 4 loop filters calculate (4) for $0 \leq j \leq 3$ and are implemented using 32-bit fixed-point arithmetic with the RTL code generated by Simulink. The architecture is depicted in Fig. 3. Each loop filter except for the one corresponding to $j=0$ consists of 3 FIR (finite impulse response) filters with orders j, $\ell-2$ and $m-1$. An additional IIR (infinite impulse response) filter is used to calculate e_n. Careful selection of the bitwidth used for the representation of the signals related to the IIR filter is needed since in IIR filters quantization errors

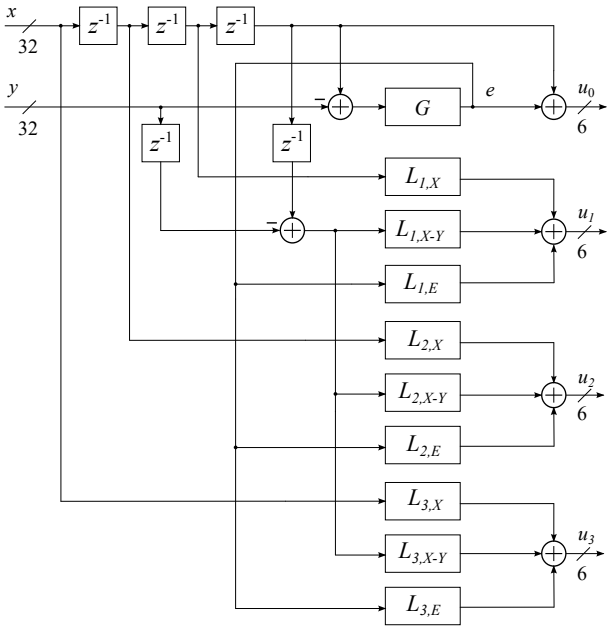

Fig. 3. The designed MSLA SDM loop filter architecture.

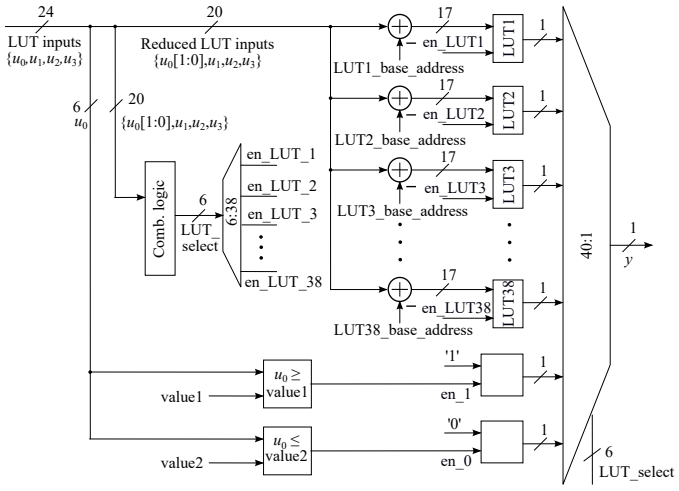

Fig. 4. The designed MSLA SDM LUT architecture.

are accumulated over time, leading to instability if they are large enough [13].

The 4-input single-bit-output quantizer is implemented as a LUT. The LUT entries are calculated using Matlab and the optimizations mentioned in the previous subsection are exploited. The LUTs are partitioned in 38 sub-LUTs to reduce the required address bits for each sub-LUT. This facilitates routing and optimizes power consumption since only one sub-LUT is utilized for the generation of an output sample. Thus, the initial 24 address bits are reduced to 17 for each sub-LUT. The LUT partitioning scheme is shown in Fig. 4. Notice the multiplexers that generate the required enable signals that select only one sub-LUT at each clock period to minimize power consumption. Two more enable signals are used to completely bypass the LUTs when the LUT inputs satisfy

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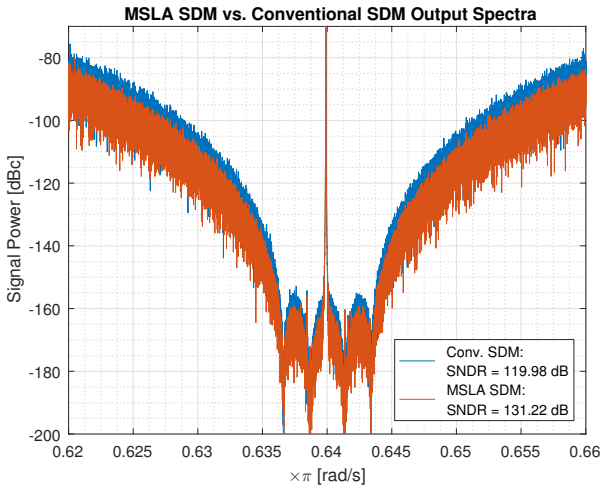

Fig. 5. MSLA SDM vs. conventional single-bit SDM output power spectra with respect to the carrier derived from digital simulation.

certain conditions that guarantee that the output has a definite value.

C. Simulation and Synthesis Results

To the best of our knowledge, there is no other hardware implementation of look-ahead SDMs since only software implementations have been proposed [10]. Therefore, comparison with other look-ahead SDM hardware implementations is not possible. A comparison of the MSLA SDM with other look-ahead SDMs in terms of algorithmic complexity and performance is available in [11]. To quantify the performance advantage and the additional hardware complexity of the designed MSLA SDM, we designed a conventional single-bit SDM with the same OSR and NTF order and central frequency. However, its NTF needs to have lower out-of-band gain to maintain stability.

1) Simulation Results: The performance advantage of the designed MSLA SDM over the single-bit conventional one is demonstrated in Fig. 5, which shows the output power spectrum with respect to the carrier of both modulators. The plot is derived from digital simulation data after place and route, i.e. the actual digital output generated by the FPGA. A 24-bit output direct digital synthesizer (DDS) generates a sinusoidal signal with amplitude 0.25 and frequency $f = (2621/2^{13})f_{\text{clk}}$ which is used as the input for the generation of 4,000,000 output samples. A time averaging of 2 has also been used to smooth the resulting power spectra. The MSLA SDM exhibits about 6 dB higher dynamic range than the conventional SDM. This translates to a SNDR of 131.22 dB compared to 119.98 dB for the conventional SDM.

2) Synthesis Results: The better performance of the MSLA SDM comes at the cost of increased hardware complexity. Table I summarizes the synthesis results of the MSLA and the conventional SDM implementations including the DDS. The designed MSLA SDM generates its output at a rate of 13.3 Msamples/s, which is about 5.9 times lower than that

TABLE I
MSLA SDM VS. CONV. SDM HARDWARE RESOURCES

	MSLA SDM	**Conv. SDM**
Max. output rate [Msamples/s]	13.3	78.7
Slice LUTs [Used / Util.]	23,342 / 11.45%	2,627 / 1.29%
Slice Registers [Used / Util.]	1,665 / 0.41%	391 / 0.10%
F7 Muxes [Used / Util.]	2,331 / 2.29%	973 / 0.95%
F8 Muxes [Used / Util.]	650 / 1.28%	423 / 0.83%
DSP Blocks [Used / Util.]	205 / 24.40%	30 / 3.57%

of the conventional SDM. As far as hardware resources are concerned, the MSLA SDM utilizes on average 5.9 times more FPGA resources than those used by the conventional SDM. Excluding the DSP blocks, about half of the MSLA SDM resources are used for the implementation of the quantizer. These results show that although the MSLA SDM hardware complexity is higher than that of the conventional SDM, it allows for real-time operation.

We are aware that the FIR and IIR filter implementations, especially the multipliers, can be further optimized for increased speed and we are currently working on such optimizations. Nevertheless, the comparison between the MSLA and the conventional SDM is not affected, since any optimizations should affect almost equally both of them.

The results are similar for a low-pass MSLA SDM hardware implementation. More specifically, the SNDR improvement over conventional single-bit SDMs for the same number of look-ahead steps k is roughly the same for both band-pass and low-pass modulators [14]. As far as hardware complexity is concerned, a low-pass MSLA SDM hardware implementation exhibits roughly the same complexity increase over a single-bit conventional low-pass SDM as its band-pass counterpart over a single-bit conventional band-pass SDM.

IV. CONCLUSION

MSLA SDMs have been proposed as an alternative to conventional single-bit SDMs improving on their SNDR and stability characteristics. The basic principles of their operation were presented and a hardware architecture for their implementation was proposed. The performance and hardware requirements of a proof-of-concept MSLA SDM FPGA implementation were compared to those of a conventional single-bit SDM implementation. The additional hardware overhead is not prohibitive for real-time operation, rendering MSLA SDMs a viable choice in applications requiring single-bit quantization with higher SNDR than possible with conventional single-bit SDMs. Furthermore, the look-ahead steps of MSLA SDMs can be adjusted to achieve a good balance between additional hardware complexity and performance improvement.

ACKNOWLEDGMENT

The authors acknowledge financial support from Weasic Microelectronics S.A. for covering traveling and conference attendance expenses.

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