# Comparison of Recently Developed Single-Bit All-Digital Frequency Synthesizers in Terms of Hardware Complexity and Performance

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***Abstract*—Internet of Things growth requires the development of low power and low cost wireless transceivers. Here, we present three recently developed all-digital frequency synthesizer architectures which can be used as transmitters for Internet of Things applications. These all-digital transmitters are based on different sigma-delta modulator architectures, varying in performance and hardware complexity. The operation principles of the three proposed architectures are described. Then, proof-of-concept FPGA implementations of these architectures are presented and compared in terms of hardware resources and speed. Their performance is tested using 32-QAM modulated signals. Finally, conclusions are drawn to help the reader select the most suitable architecture for a given application.**

***Index Terms*—Direct digital synthesizer, frequency synthesis, all-digital transmitter, modulation, noise shaping, single-bit quantization, sigma-delta, look-ahead, Internet of Things**

## I. Introduction

The development of low power and low cost wireless transceivers is key to the success of Internet of Things (IoT) [1]. Therefore, new transceiver architectures for IoT applications constitute a very active and important area of research. In this context we present a number of all-digital transmitter architectures varying in hardware complexity and performance.

Since the proposed architectures are based on digital circuits, they inherit all the advantages associated with digital circuit design. Namely they are immune to process, voltage and temperature variations (PVT), they are scalable and reconfigurable and they have a much shorter concept-to-market time than analog or mixed-signal circuits due to the availability of advanced design and verification tools. Furthermore, digital frequency synthesizer and transmitter architectures, offer instantaneous frequency hopping and very high frequency accuracy and resolution.

Single-bit signal representation is essential for all-digital transmitter architectures, allowing for the elimination of multi-bit DACs which are challenging and power hungrey mixed-signal circuits [2]. Moreover, single-bit DACs are inherently linear and subject only to gain and offset errors which can be easily corrected [3]. However, traditional single-bit synthesizer architectures such as the pulse direct digital synthesizer (PDDS) as well as the Flying-Adder (FA) [4], suffer from high deterministic jitter, spurious tones or a high noise floor due to dithering [5].

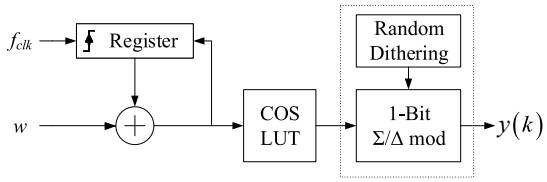


Fig. 1. Pulse DDS (PDDS) with sigma-delta noise shaping.

A solution to the aforementioned problems is the exploit of noise shaping techniques, which remove the quantization noise out of a certain frequency band [6]. The most common way to achieve this is to use Sigma-Delta modulators (SDMs) [6]. In this work, three frequency synthesizer architectures with direct amplitude and phase/frequency modulation based on different SDMs are presented, namely the Multi-Step Look-Ahead (MSLA) SDM based synthesizer [7], the Quadrature Homodyne Filter (QHF) SDM based synthesizer and the Multiplier-Free QHF (MFQHF) SDM based synthesizer [8].

In the following section, the three architectures are introduced and the basics of their operation are discussed. Section III provides simulation and FPGA implementation synthesis results that compare the performance and hardware complexity of the proposed architectures. Finally, section IV presents the conclusions and gives future research orientations.

## II. All-Digital Frequency Synthesizer Architectures

The general architecture of the proposed all-digital frequency synthesizers is shown in Fig. 1. An $n$-bit accumulator is used to provide the phase to a cosine Look-Up Table (LUT). The accumulator and the cosine LUT form a Direct Digital Synthesizer (DDS). The phase increase rate, i.e. the frequency, is controlled by the value of the Frequency Control Word (FCW) $w$ through the relation $f = (w/2^n)f_s$, where $f_s$ is the output sampling rate. The quantization noise of the LUT output is shaped by a single-bit output SDM. Random dithering may be added to remove undesirable frequency spurs. Moreover, frequency or phase modulation can be achieved by adding a modulating signal to the cosine LUT input,

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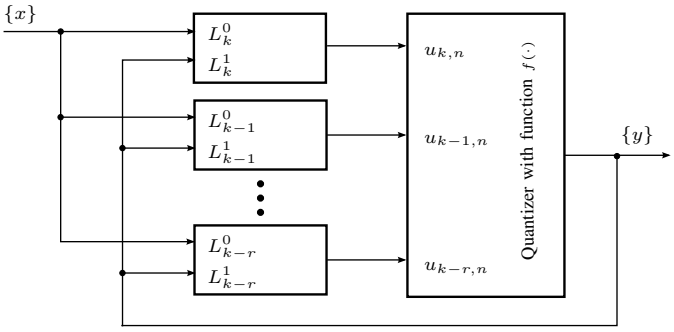


Fig. 2. The MSLA SDM system diagram.

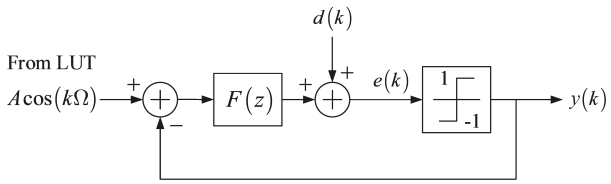


Fig. 3. The single-bit band-pass Σ/Δ modulator.

while amplitude modulation is possible by multiplying the cosine LUT ouptut with a modulating signal. The following subsections focus on a brief explanation of the various types of SDMs that are used to convert the multi-bit cosine LUT output to single-bit.

### A. Multi-Step Look-Ahead SDM Architecture

MSLA SDMs are a class of single-bit "look-ahead" SDMs, which offer increased performance and noise shaping characteristics over conventional single-bit SDMs by taking into account both current and future quantization errors [9]. This is accomplished by minimizing a properly formulated cost function. The number of future quantization errors taken into account in the the cost function is known as look-ahead steps $k$.

In Fig. 2 the MSLA SDM system diagram is shown. The system is composed of $(r+1)$ two-input digital filters $(L_j^0, L_j^1)$, whose outputs are fed to a $(r+1)$-input single-bit-output quantizer. Parameter $r$ is the number of partial costs involved in the cost function and for optimal performance it is $r = k$ [9]. The digital filter coefficients are determined by the desirable noise transfer function $(ntf)$ and the number of look-ahead steps used [6].

### B. Quadrature Homodyne Filter Architecture

In Fig. 3 a single-bit band-pass SDM is depicted. The signal transfer function $(stf)$ is given by $stf(z) = F(z)/\big(1+F(z)\big)$. Replacing the quantizer by an additive noise source, the noise and dither transfer functions ($ntf$ and $dtf$) are $dtf(z) = ntf(z) = 1/\big(1+F(z)\big)$. Filter $F(z)$ is band-pass.

Using a band-pass SDM as part of the all-digital synthesizer architecture depicted in Fig. 1 means that only frequencies within the SDM passband can be generated in practice. When a different frequency range has to be generated, the digital filter $F(z)$ coefficients must change. Therefore, any filter optimization used for a specific frequency range cannot be directly applied to another one. The Quadrature Homodyne Filter (QHF) architecture shown in Fig. 4 has been proposed to address this issue [8].

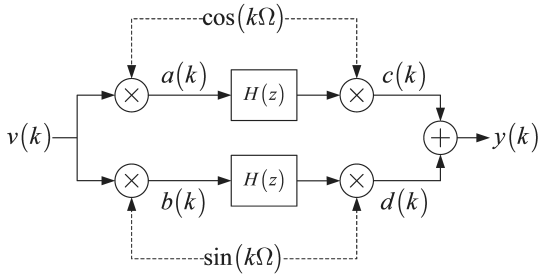


Fig. 4. The quadrature homodyne filter architecture for the implementation of $F(z)$.

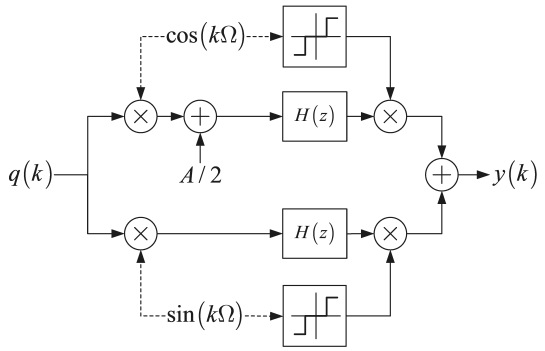


Fig. 5. The quadrature homodyne filter multiplier-free architecture.

The band-pass filter $F(z)$ is implemented by using two identical low-pass filters $H(z)$ and quadrature homodyne down- and up-conversion to achieve band-pass frequency response centered at the carrier angular frequency $\Omega$. As a result, apart from filters $H(z)$, the QHF architecture requires four multiplications, one addition and two low-pass filters $H(z)$.

### C. Multiplier-Free Quadrature Homodyne Filter Architecture

The four additional multiplications in the QHF architecture in Fig. 4 can be eliminated resulting in the Multiplier-Free QHF architecture shown in Fig. 5. Note first that the signal entering the QHF $F(z)$ is $Acos(kW) \pm 1$. Assuming the low-pass filter $H(z)$ is sufficiently narrow, then $Acos(kW)$ at the input can be replaced by the addition of A/2 after the multiplication with the $cos(kW)$ as shown in Fig. 5. Moreover, the multiplication of the quadrature carriers $Acos(kW)$ and $Asin(kW)$ with $\pm 1$ is trivial. This eliminates the two multiplications on the left. Also, it can be shown that quantizing the quadrature carriers in three-levels (0, ±h, where typically h=1/2) before entering the two multiplications on the right does not alter the output spectrum significantly [8], [10]. This makes the two multiplications on the right of Fig. 5 trivial as well.

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## III. FPGA Implementation and Digital Simulation Results

To investigate the performance and the required hardware resources of all-digital synthesizers based on the different SDM architectures presented in the previous sections, we have developed FPGA implementations of each architecture. All implementations are capable of direct phase/frequency and amplitude modulation. In the following subsection we present the synthesis results and the resources required for each architecture. Then, we provide simulation results of a 32-QAM modulation scheme and compare the performance of the different all-digital synthesizer architectures when used as all-digital transmitters.

### A. Hardware Implementation Details

The proposed all-digital synthesizer architectures consist of the same DDS followed by the three different SDMs that where presented in the previous section. The DDS has a 13-bit accumulator $n$ and a cosine LUT with 24-bit output. Thus it has a frequency resolution of $(1/2^n)f_s$. All SDMs are band-pass with center frequency $\omega_0 = 2\pi{\cdot}0.64$, 8-th order NTFs and an oversampling ratio of 128. Let us now discuss the hardware implementations of the various SDMs.

*1) MSLA SDM:* The implemented MSLA SDM has $k = r = 3$ look-ahead steps and therefore has 4 loop filters as shown in the system diagram of Fig. 2. The 4 loop filters can be composed of 1 IIR filter and 9 FIR filters. For the implementation of the FIR filters 32-bit fixed-point arithmetic is used, while the IIR filters require 64-bit fixed-point arithmetic for stability reasons due to the accumulation of quantization errors [11]. The multi-input single-bit-output quantizer is implemented as a family of LUTs. After optimization it is concluded that using 20 bits for all the quantizer inputs is sufficient for the correct operation of the MSLA SDM [12].

*2) QHF SDM:* The implemented QHF SDM follows the system-level description in Fig. 3, where filter $F(z)$ is implemented as shown in Fig. 4. The sine and cosine signals are already available from the DDS cosine LUT. Filters $H(z)$ are implemented using 32-bit fixed-point arithmetic and do not require multipliers since their coefficients are sums of at most 3 powers of two. Therefore, multiplications are reduced to a number of addition and shift operations.

*3) MFQHF SDM:* The MFQHF hardware implementation is based on the system-level description in Fig. 3, where filter $F(z)$ is implemented as shown in Fig. 5. Notice that essentially no multipliers are required as all multiplications are either by 1, 0 or $-1$. The implementation of filters $H(z)$ is the same as in the case of the QHF SDM. It should also be noted that in contrast to the two previously anayzed SDMs, in the case of the MFQHF SDM amplitude modulation does not need multiplication of the cosine LUT output with a modulating signal. Instead, the modulating signal amplitude $A/2$ is directly added to the cosine homodyne filter path as seen in Fig. 5, eliminating the need for a multiplier.

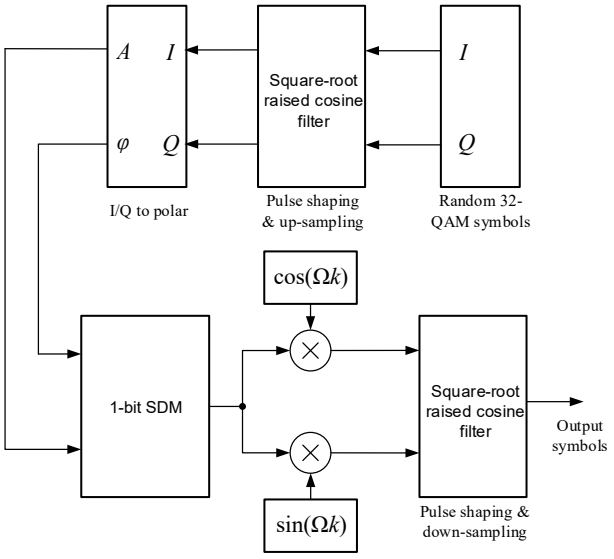


Fig. 6. The 32-QAM modulation-demodulation setup.

### B. FPGA Implementation Synthesis Results

The all-digital frequency synthesizer architectures analyzed in the previous subsection were described in Verilog RTL models and were synthesized and implemented for a Xilinx Kintex-7 KC705 Evaluation Kit target device. The hardware resources required by each architecture, as well as other parameters are summarized in Table I.

The MSLA SDM based synthesizer has an average FPGA resource utilization 9.13%, which is the highest among the proposed architectures. It also achieves the lowest output sampling rate at 14.34 Msamples/s. On the other hand the MFQHF SDM based synthesizer uses the least FPGA hardware resources (1.64% average utilization) and exhibits the highest output sampling rate at 102.05 Msamples/s. The QHF SDM based synthesizer stands in-between the two aforementioned synthesizers in terms of hardware resources and output sampling rate.

As it is shown in the next subsection, the increased hardware complexity of the MSLA SDM based synthesizer is balanced by its superior performance. Finally, it is worth noting that preliminary synthesis results using TSMC 65nm IC technology suggest that the output sampling rates are increased at least by a factor of 5.28, reaching 75.8 Msamples/s for the MSLA SDM based synthesizer.

### C. 32-QAM Modulation Performance Results

The performance of the proposed all-digital synthesizers with phase/frequency and amplitude modulation capability is quantified using random 32-QAM modulated signals [8]. These signals are encoded in single-bit representation using the proposed all-digital synthesizers. Then they are demodulated and used to calculate the error vector magnitude (EVM) and signal-to-noise ratio (SNR) achieved by each architecture. The modulation-demodulation setup used is shown in Fig. 6.

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TABLE I
ALL-DIGITAL SYNTHESIZER HARDWARE RESOURCES

| | MSLA SDM | QHF SDM | MFQHF SDM |
|---|---|---|---|
| Max. output rate [Msamples/s] | 14.34 | 76.47 | 102.05 |
| Slice LUTs [Used / Util.] | 23,775 / 11.67% | 6,602 / 3.24% | 6,763 / 3.32% |
| Slice Registers [Used / Util.] | 1,541 / 0.38% | 482 / 0.12% | 484 / 0.12% |
| F7 Muxes [Used / Util.] | 2,502 / 2.46% | 2,546 / 2.50% | 2,546 / 2.50% |
| F8 Muxes [Used / Util.] | 753 / 1.48% | 1,154 / 2.26% | 1,154 / 2.26% |
| DSP Blocks [Used / Util.] | 249 / 29.64% | 10 / 1.19% | 0 / 0.00% |
| **Average FPGA Util.** | 9.13% | 1.86% | 1.64% |

TABLE II
32-QAM MODULATION PERFORMANCE

| | MSLA SDM | QHF SDM | MFQHF SDM |
|---|---|---|---|
| RMS EVM [%] | 0.96 | 1.31 | 1.37 |
| Max. EVM [%] | 2.58 | 8.88 | 11.33 |
| SNR [dB] | 40.38 | 37.66 | 37.26 |

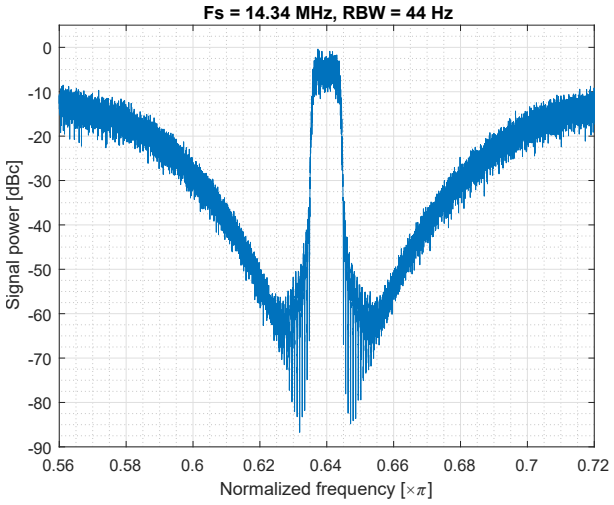


Fig. 7. MSLA SDM based synthesizer spectrum for 32-QAM modulated input signal.

Table II displays the performance results obtained from the modulation and demodulation of 10,000 symbols. The pulse shaping raised cosine filter used for inter-symbol interference (ISI) reduction also increases the sampling rate of the signal by a factor of 256. Since we use 32-QAM modulation, i.e. 5 bits/symbol, these symbols correspond to 50 Kbits of data. Notice that the synthesizers with the highest hardware complexity also exhibit the best performance. The MSLA SDM based synthesizer outperforms the other two synthesizers in terms of SNR and EVM. More specifically, the maximum EVM observed for the MSLA SDM based synthesizer is only 1.31%, while it is 8.88% and 11.33% for the QHF and MFQHF based synthesizers respectively. Depending on the application the least complex synthesizer satisfying the performance specifications can be used.

The MSLA SDM based synthesizer output spectrum is plotted in Fig. 7 and the resulting constellation diagram is shown in Fig. 8. It should be noted that the bandwidth of the upsampled baseband signal is lower than that of the MSLA SDM and therefore out-of-band noise does not reduce the quality of the transmitted signal.

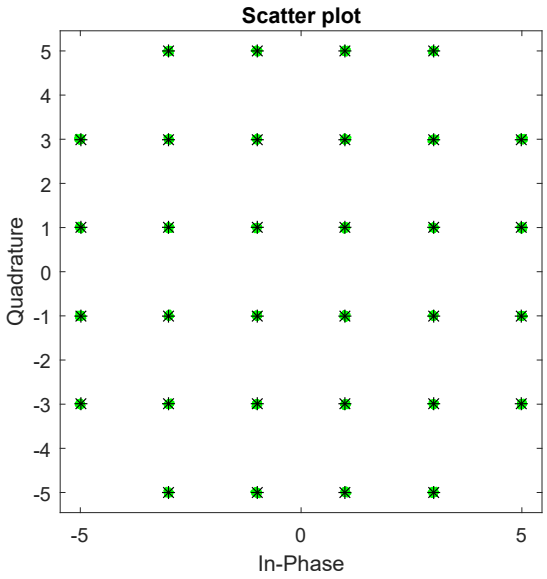


Fig. 8. MSLA SDM based synthesizer constellation diagram for 32-QAM modulation.

## IV. CONCLUSION

Three all-digital frequency synthesizer architectures with phase/frequency and amplitude modulation capability were presented. Each architecture targets different performance levels and hardware complexity. All the proposed synthesizers were implemented in FPGA and their hardware requirements and output sampling rates were quantified. Their performance in terms of EVM and SNR in a 32-QAM modulation scheme was also investigated. It is shown that each of the proposed synthesizers is suited to different application requirements. We are currently working towards further optimizing the proposed synthesizer architectures and developing all-digital transmitters based on these architectures that are compatible with many popular wireless protocols used in IoT applications.

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