Laboratory Jitter Removal Circuit for Single-bit All-Digital Frequency Synthesis

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Abstract—All-digital frequency synthesizers based on sigma- direct mo

delta modulation with single-bit output can have exceptionally high dynamic range and spurs-free dynamic range, in simulation. The performance of their FPGA implementations however is significantly limited by the jitter introduced by the FPGA and its clock reference, which is translated to phase noise. This paper introduces a laboratory circuit architecture for suppressing the FPGA and reference jitter in order to achieve spectrally cleaner single-bit output sequences and demonstrate the achievable performance of the all-digital frequency synthesizers. The proposed architecture is based on a 1-Bit DAC re-clocking the singlebit digital output of the FPGA using one of the two low-jitter clocks generated by a low phase noise reference oscillator. The second clock is used to clock the FPGA after passing through a programmable delay line and a small-value frequency divider. The implementation of the circuit's architecture is presented discussing the design challenges. Phase noise measurements demonstrate the performance of the circuit. Spectral measurements illustrate the effectiveness of jitter removal in the case of a sigma-delta modulator single-bit output.

Keywords—Single-bit, all-digital, frequency synthesis, sigmadelta, DAC, phase noise, jitter attenuation, reclocking, clock generation, programmable delay

I. INTRODUCTION

A huge amount of effort has been dedicated over the past decades in making circuits purely digital. This effort has been motivated by the numerous advantages of digital circuits such as noise and temperature immunity, low sensitivity to power supply variations and straightforward migration to newer integration technologies. All-digital frequency synthesizers with single-bit output exhibit all the above advantages while keeping the advantages of direct digital synthesizers (DDS) like very high frequency resolution, fast frequency hopping and



Fig. 1. Single-bit all-digital frequency synthesizer.

direct modulation. Furthermore, they have no need for multibit DACs which are sensitive to component mismatches and suffer from complex nonlinearities. Instead they use singlebit DACs which are inherently linear. This allows all-digital frequency synthesizers with single-bit output to achieve higher dynamic range and SFDR than those of the standard DDS.

All-digital frequency synthesizers with single-bit output are used in many modern applications including audio DACs and all-digital transmitters. In the laboratory the digital blocks are usually implemented on FPGAs. If the single-bit output is passed through a low-pass or band-pass reconstruction filter (depending on the application) ideally we get the corresponding analog signal. In reality this is unfortunately not the case since the digital signal at the FPGA output suffers from jitter. The problem arises when the carrier frequency becomes considerably high with respect to the frequency of the clock. The jitter of the digital signal appears as phase noise in the analog domain. Phase noise deteriorates the quality of the signal, increases the noise floor and limits the dynamic range of the system. Therefore, the excessive jitter at the output of a FPGA creates the need for jitter removal circuits.

In the next section the effects of jitter are briefly described and the architecture of the jitter removal circuit is introduced. The circuit implementation follows in section III, where the components and the main attributes of the circuit are described. Section IV provides phase noise measurements of the implemented circuit. The performance of the circuit is also demonstrated with a 2nd order low-pass sigma-delta modulator (SDM). Finally, section V concludes the discussion.

II. JITTER REMOVAL

An all-digital frequency synthesizer using two low-pass single-bit Multi-Step Look-Ahead sigma-delta modulators (MSLA SDMs) [1], in order to generate the I and Q components, is shown in Figure 1.

In an FPGA implementation of this system, the singlebit digital output y_{RF} is clocked using a D flip-flop in the FPGA's I/O bank. This can be viewed as a sampling process, i.e., a multiplication of the input signal and the clock in the time domain. Therefore, the spectrum of the clock signal is convolved with the spectrum of the input signal [2] and the phase noise of the clock appears around the carrier (Figure 2).

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Fig. 2. Effect of clock phase noise in the frequency domain.

This corrupts the spectrum near the carrier working against the noise suppression achieved by the noise shaping of the SDM.

While the phase noise of the clock signal is responsible for the "close-in" noise, the D flip-flop's intrinsic noise mainly affects the "far-out" noise (noise floor) of the output. The "far-out" phase noise causes a degradation of the overall SNR which is given by the following equation, where f_o is the frequency of the carrier [3]:

$$SNR_{Jitter} = -20 \log_{10}(2\pi \times f_o \times t_{Jitter}) .$$
 (1)

Therefore, the jitter of the output signal can be a limiting factor of the system's performance, especially in the case of high frequency carrier. Since jitter can never be fully removed from the signal, the challenge is to reduce it as much as possible.

A. System Architecture

The total jitter at the output of a D flip-flop depends on two factors: the time uncertainty of the clock signal that triggers the D flip-flop and the additive noise of the D flip-flop itself. Both of these factors are very poor in the case of the FPGA. The idea is to use an external low noise D flip-flop which is triggered by an ultra-low jitter clock signal.

One may wonder whether the external D flip-flop is really necessary. Why not clocking the FPGA's internal D flip-flop with an external low jitter clock instead? The answer lies inside the FPGA. The phase noise of the clock signal triggering the internal D flip-flop results from the phase noise of the clock generation modules (oscillators, PLLs) combined with the noise of the clock distribution network (fanout buffers, transmission lines) forming FPGA's clock tree. So even if the clock signal fed to the FPGA has very low phase noise, the additive noise of the clock distribution network will degrade its quality. This is why we need an external D flip-flop along with an ultra-low jitter clock generator. We refer to this external circuit as the "1-Bit DAC" since its output can be treated as an analog signal.

The 1-Bit DAC reclocking the digital signal should share the same clock reference with the FPGA (Figure 3). An important issue is the timing between the clock signal and the 1-Bit



Fig. 3. Reclocking the single-bit data signal.

signal at the D flip-flop input. Sampling the data signal near its transition points can lead to sampling error. Therefore the signal must be sampled roughly at the middle of the unit interval where the bit value is not affected by time fluctuations (Figure 3).

The signals are transfered between the FPGA and the 1-Bit DAC through coaxial cables. A coaxial cable introduces a phase shift to the signal proportional to its electrical length. In addition to that, the clock distribution network of the FPGA introduces a delay as well. Therefore, in order to achieve the desirable timing, regardless of the physical length of the coaxial cables or the FPGA delay, we must be able to control the phase of the clock signal delivered to either the D flip-flop or the FPGA. These timing issues increase the complexity of the basic architecture in Figure 3.



Fig. 4. Block diagram of the 1-Bit DAC.

The block diagram of the 1-Bit DAC circuit is presented in Figure 4. A low phase noise reference sinusoidal signal is fed to the clock distributor which generates two low-jitter clock signals; one for triggering the D flip-flop and the other for clocking the FPGA. The frequency and the phase of each clock can be configured by programming the clock distributor. For this reason a microcontroller is embedded.

After the re-clocking, the signal is fed differentially into a buffer. Finally a balun is used for transforming the differential signal to single-ended for the output.

III. CIRCUIT IMPLEMENTATION

For the jitter removal circuit two different boards have been constructed: the 1-Bit DAC and the reference oscillator.

A. The 1-Bit DAC Circuit

The 1-Bit DAC was designed to be compatible with the KC705 Evaluation Board (Kintex-7 FPGA Family) which is used in the laboratory. The clock signal is provided differentially to the KC705's *User SMA Clock Input* using LVDS_25 [4]. The single-bit digital signal is obtained single-ended from a KC705's *GPIO SMA Connector* and is fed into the 1-Bit DAC's D flip-flop using LVCMOS25 signaling [4].

Among the various interface standards LVPECL was selected for the signaling between the 1-Bit DAC's internal blocks. The main advantages of LVPECL are high speed of operation and high driving capability. The last one is important for achieving low phase noise [5].

Given the above, the following integrated circuits (ICs) were selected: The LVDS and LVPECL clock signals are generated by Texas Instruments' LMK01000 high performance clock distributor. The frequency and the phase of each clock is programmed via an Atmel's ATmega328p embedded microcontroller. The reclocking of the single-bit signal is accomplished through On Semiconductors' NBSG53A SiGe differential D flip-flop which accepts the FPGA's LVCMOS signal. The LVPECL output of the D flip-flop passes through



Fig. 5. The 1-Bit DAC board.



Fig. 6. Block diagram of the reference oscillator.

Analog Devices' ADCLK925 ultrafast SiGe ECL differential buffer. At the final stage the differential signal is converted into single-ended by MACOM's MABA-011029 transmission line balun to be matched to 50 Ohm systems. The ICs are supplied by Analog Devices' ADM7154 and ADM7155 ultralow noise RF linear regulators.

B. Reference Oscillator

To provide a low phase noise reference clock to the 1-Bit DAC, low noise phase locked loop frequency source was implemented. The generated reference is a 5dBm sinusoidal signal at 1GHz. We utilised a very narrow tuning band VCO and Analog Devices' HMC440 phase detector capable of noise floor performance of -153dBc/Hz at 10kHz for 100MHz PFD frequency. The PFD frequency reference is supplied by a Crystek low phase noise 100MHz crystal oscillator. After careful optimization of the crossing frequency between the reference and the VCO, the loop bandwidth was set to 6.5kHz.

The second order loop filter of the PLL was implemented using the Analog Devices' ADA4897-1. Care was taken supplying all components from dedicated low noise regulators to avoid phase noise introduction through AM to PM conversion mechanisms. The block diagram of the reference oscillator is shown in Figure 6.

IV. LAB MEASUREMENTS

Two types of measurements were carried out in the lab for evaluating the performance of the implemented system: phase noise measurements and spectral measurements for the case of a single-bit output sigma-delta modulator.



Fig. 7. The reference oscillator board.

A. Phase Noise Measurements

Phase noise was measured with a carrier at 250MHz and an offset from 100Hz to 10MHz. In order to perform the measurements the FPGA was programmed to produce a square wave at 250MHz. The results are shown in Figure 8. The blue line shows the phase noise of the single-bit signal at the FPGA output. The red line represents the phase noise of the single-bit signal after the reclocking through the 1-Bit DAC. The yellow line corresponds to the phase noise of the reference oscillator (shifted at 250 MHz since the actual carrier is at 1GHz [6]).

The performance of the reference oscillator at 250 MHz shows a noise floor of -180dBc/Hz and phase noise better than -145dBc/Hz at 100kHz offset. Notice that the phase noise of the 1-Bit DAC and that of the reference oscillator are almost identical up to 70kHz offset. This implies that the 1-Bit DAC's additive phase noise up to this offset is negligible. Beyond the 70kHz offset the D flip-flop's white phase noise sets the noise floor of the 1-Bit DAC circuit approximately at -150dBc/Hz.



Fig. 8. FPGA's (blue), 1-Bit DAC's (red) and reference oscillator's (yellow) measured phase noise with a carrier at 250 MHz. The above measurements were carried out on the E5052B SSA Signal Source Analyzer.

B. Reclocking the Sigma-Delta Modulator's Output

In order to qualify the performance of the jitter removal circuit when reclocking a sigma-delta modulated signal a 2nd order low-pass sigma-delta modulator was implemented in the FPGA. Bear in mind that the circuit was designed to work along with single-bit all-digital frequency synthesizers, the output of which are usually sigma-delta modulated signals.

The output of the FPGA is a sigma-delta modulated sinusoid at 213kHz. The FPGA clock frequency was 350MHz. Figure 9 shows the spectrum of the signal at the FPGA output and the 1-Bit DAC output with 160MHz span. We can see that after the reclocking with the 1-Bit DAC the "close-in" noise is reduced by more than 30dB.

V. CONCLUSIONS

A laboratory jitter removal circuit designed to work along with FPGA implemented single-bit all-digital frequency synthesizers was presented. As the lab measurements illustrate serious jitter attenuation is achieved by reclocking the digital signal with the 1-Bit DAC, resulting in better phase noise



Fig. 9. Comparison between the FPGA (Up) and the 1-Bit DAC (Down) output spectrum in the case of a sigma-delta modulated signal. The above measurements were carried out on the N9010A EXA Signal Analyzer.

performance. This allows to demonstrate the high dynamic range and spurs-free dynamic range capabilities of the alldigital frequency synthesizers with single-bit output.

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