Noise Shaping Advantages of Band-Pass Multi-Step Look-Ahead Sigma-Delta Modulators Over Conventional Ones in Signal Synthesis

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***Abstract*—Sigma-Delta modulators (SDMs) are capable of shaping the quantization noise out of a specific frequency band defined by their noise transfer function (NTF). A single-bit output SDM pose further advantages in applications that would typically require a multi-bit DAC, since then only a single-bit DAC is required, which is much easier to design and is inherently linear in comparison to a multi-bit one. Look-ahead SDMs have been proposed to enhance the signal-to-noise-and-distortion-ratio (SNDR) and the output bandwidth of conventional single-bit SDMs. Multi-Step Look-Ahead sigma-delta modulators (MSLA SDMs) further reduce the hardware complexity required for the implementation of typical look-ahead SDMs while maintaining their performance advantages. In this work the architecture and the benefits of the MSLA SDMs are showcased. Finally the advantages of the MSLA SDMs over single-bit conventional ones are demonstrated and several hardware implementation choices for design optimization are discussed.**

***Keywords*—Sigma-delta modulator, noise shaping, single-bit quantization, look-ahead, band-pass digital filters**

I. Introduction

A current trend in integrated circuit design is to replace as many analog or mixed-signal blocks as possible with digital equivalents. Digital circuits occupy smaller chip area, have immunity to process, voltage and temperature variations, are scalable, reconfigurable and have faster design cycles than analog or mixed-signal blocks. Frequency synthesizers are circuits that can have all-digital implementations. A known circuit used for digital frequency synthesis is the direct digital synthesizer (DDS). However, it requires a digital to analog converter (DAC) for the conversion of its digital multi-bit output to analog. An alternative method is to use the pulse direct digital synthesizer (PDDS), which has single-bit output and is ideal for all-digital system design. Nevertheless, the PDDS suffers from frequency spurs and a high noise floor [1]. A solution to this problem is to apply single-bit sigma delta modulators (SDMs) which are capable of shaping the quantization noise out of a specific frequency band [2].

The major concern about single-bit SDMs is that their noise shaping capabilities are limited due to stability restrictions. Another approach is to use look-ahead SDMs instead [3], which offer increased bandwidth, spurious-free dynamic range (SFDR) and increased signal-to-noise-and-distortion ratio (SNDR) compared to conventional single-bit SDMs. The trade-off is increased hardware complexity, which does not allow for real time applications to be implemented. Therefore, Multi-Step Look-Ahead sigma-delta modulators (MSLA SDMs) were proposed in [4] to overcome the drawbacks while retaining the advantages of look-ahead SDMs.

In the second section of the paper the MSLA SDM system architecture basics are described. In section III the parametric simulation results show the advanced capabilities of the MSLA SDMs compared to the conventional single-bit SDMs, as well as the application of the MSLA in an all-digital system. Finally, in the last section, the conclusion is discussed.

II. MSLA SDM Operation

Multi-Step Look-Ahead SDMs succeeds in improving the stability range and noise shaping characteristics of conventional single-bit SDMs by taking into account both current and future quantization errors. This is accomplished by minimizing a properly formulated cost function [3]. The concept of future ("look-ahead") errors, and therefore that of future input samples, does not imply any prediction; instead, the input signal is delayed by a number of samples equal to the number of look-ahead steps used.

Fig. 1 presents the MSLA SDM architecture of [4] where x is the modulator's input and y is the modulator's 1-bit output. The system is composed of $r+1$ two-input IIR filters (L_j^0, L_j^1) producing the $r+1$ outputs u_j, $k-r \leq j \leq k$, where k is the number of look-ahead steps and $r+1$ is the number of partial quantization error costs [4].

The quantization noise transferred to the 1-bit output is generated by the $(r+1)$-input single-bit-output quantizer and is described approximately by the linear model of noise transfer function (NTF) [3]. The NTF and the number of look-ahead steps determine the IIR filter coefficients of the MSLA SDM [4]. The order of each filter (L_j^0, L_j^1) is associated with the number of look-ahead steps, namely it is $j+k$. The filter outputs are fed to the $(r+1)$-input quantizer which is described by a function $f : \Re^{r+1} \rightarrow \{\pm 1\}$, whith argument $\mathbf{u}_n = [u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n}]$, and n is the discrete time

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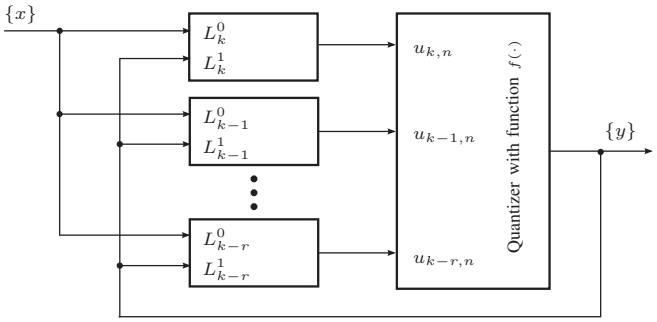

Fig. 1. The MSLA SDM system diagram.

index. The details for calculating the tvalue of the cost function and the description of the quantizer function, are outside the scope of this work and are discussed in [4].

III. MSLA SDM Implementation Aspects

This section is focused on the parameterization of the MSLA SDM in order to achieve efficient hardware implementation with optimum performance. In addition, an all-digital frequency synthesizer application with the MSLA SDM as a part of the system is shown as well.

A. Parametric MSLA SDM Investigation

For the implementation of the quantizer, specific parameters are modified with emphasis on the number of look-ahead steps k, the oversampling ratio (OSR) and the order of the filters, due to their importance on the IIR filter outputs u_j which also form the quantizer inputs [5].

The bit size of the quantizer input signals u_j, should be the smallest one possible without degrading the overall performance in terms of SNDR and NTF out-of-band-gain. Typically a fair number of integer bits, 4-5 including the sign bit and an additional 4-5 fractional bits are needed for accurate number representation. Unfortunately, a total of 8-10 bits combined for each input u_j, furtherly increases the hardware complexity for implementation beyond synthesizable limits. However, for the optimized MSLA SDM implementation that we propose, various simulations verify that 2-3 integer bits with 2-3 fractional bits are enough for accurate number representation [6].

For further performance optimization, two specific sets of simulations are investigated. The first set is in respect of the highest achievable SNDR related to the number of fractional bits required for accurate number representation between two band-pass filters, of orders 6 and 8 [7], [8]. The second set of simulations consists of comparisons between the two aforementioned band-pass filters in terms of maximum obtainable out-of-band gain while maintaining stability.

The system input is a sinusoidal signal with amplitude $A = 0.2$. The NTF central frequency is $\omega_0 = 2\pi \cdot 0.38$ and OSR $= 128$. The number of look-ahead steps k vary in $k \in \{0, 3, 4, 5, 6\}$. For the special case of $k = 0$, the MSLA reduces to a conventional single-bit SDM. The effect of the

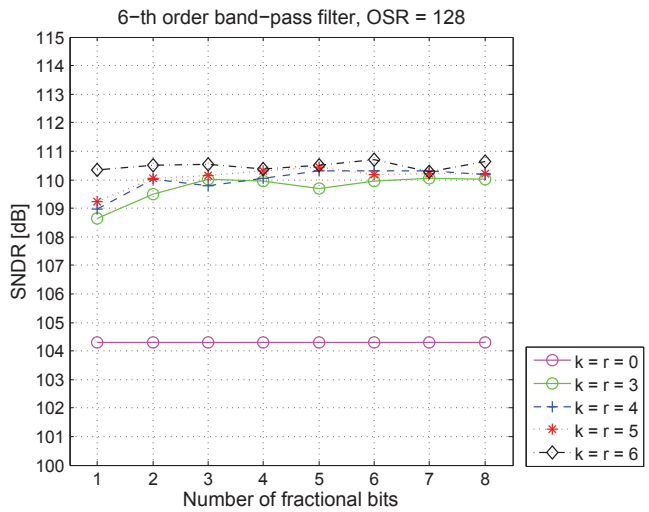

Fig. 2. SNDR vs. number of quantizer input fractional bits of the MSLA SDM for 6-th order band-pass filter

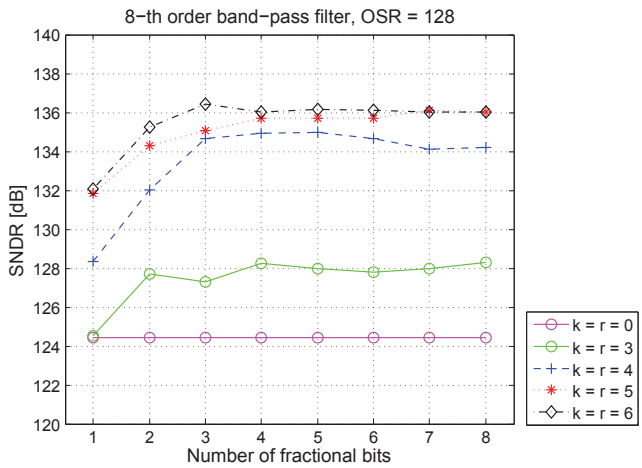

Fig. 3. SNDR vs. number of quantizer input fractional bits of the MSLA SDM for 8-th order band-pass filter

number of fractional bits are tested for values from 1 to 8. In Figs. 2 and 3 simulation results for the 6-th and 8-th order band-pass MSLA SDMs are depicted respectively. The number of fractional bits do not have any impact on the case of the conventional SDM where $k = 0$ since this corresponds to a conventional single-bit SDM. From the simulation results, it is evident that MSLA SDMs with $k > 3$ and more than 3 fractional bits exhibit at least 5dB and 3dB higher SNDR than conventional single-bit ones for the 6-th and 8-th order NTF cases respectively. The SNDR when using an 8-th order NTF instead of a 6-th order one is is also increased by approximately 15 dB. Finally, notice that using more than 3 fractional bits had no observable effect in terms of SNDR.

The effect of the number of look-ahead steps k and the number of fractional bits on the NTF out-of-band gain, is shown in

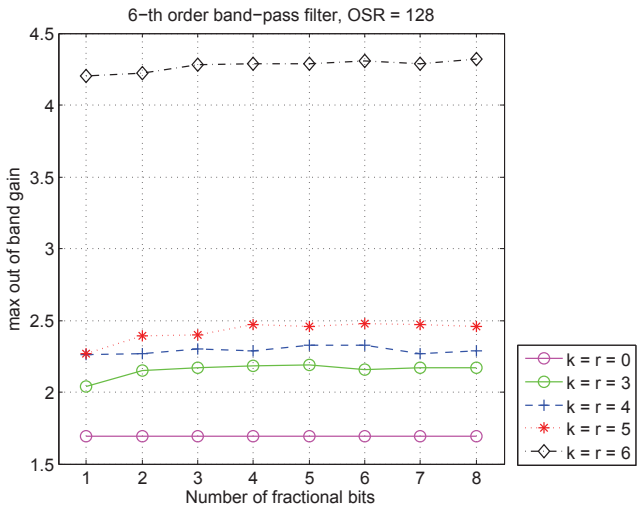

Fig. 4. Maximum stable out-of-band gain vs. number of quantizer input fractional bits of the MSLA SDM for 6-th order band-pass filter

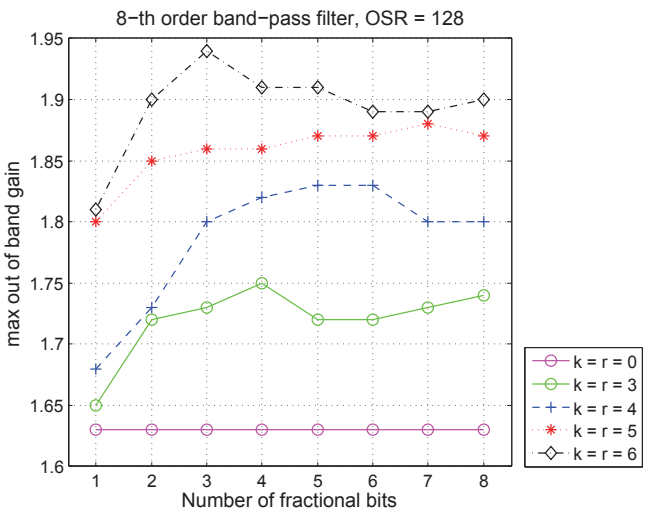

Fig. 5. Maximum stable out-of-band gain vs. number of quantizer input fractional bits of the MSLA SDM for 8-th order band-pass filter

Figs. 4 and 5. Previous system parameters remain unchanged, meaning that the input signal amplitude is $A = 0.2$, the NTF central frequency $\omega_0 = 2\pi \cdot 0.38$ and $OSR = 128$. As an initial observation, the conventional SDM $(k = 0)$ achieves much lower NTF out-of-band gain when compared to MSLA SDMs $(k >= 3)$. As the number of look-ahead steps increases, the NTF out-of-band gain also increases. The highest out-of-band gain possible for the 6-th order NTF does not compensate the higher order of an 8-th order NTF in terms of SNDR. This is a general observation. Finally, as the number of fractional bits increases, there is no significant impact on the maximum possible NTF out-of-band gain.

The simulation results for an 8-th order band-pass MSLA SDM based frequency synthesizer with 5 fractional bits in

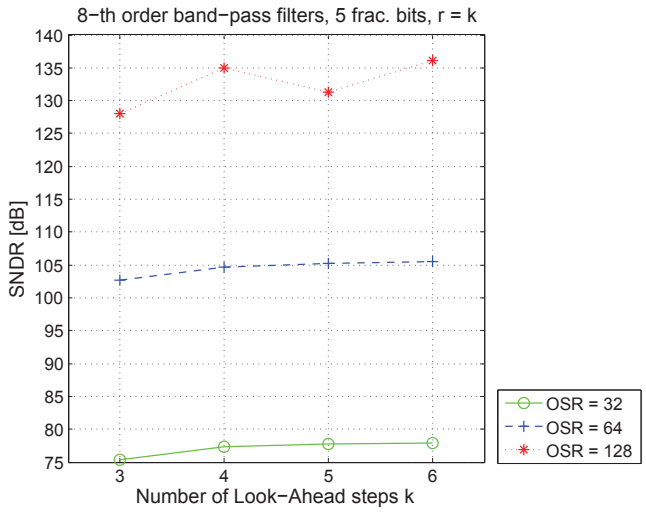

Fig. 6. SNDR vs. look-ahead steps k of the 8-th order band-pass MSLA SDM with various values of OSR

terms of the SNDR for various values of OSR are depicted in Fig. 6 with the number of look-ahead steps as a parameter. The sinusoidal input has amplitude $A = 0.2$ and the central NTF frequency is $\omega_0 = 2\pi \cdot 0.38$. Higher OSR leads to increased SNDR outputs as expected. Also notice that compared to previous results, the number of fractional bits can be reduced to 3 without reducing the overall performance. This is important since it results in an efficient hardware implementation.

B. Hardware Implementation Choices

As far as the behavior of the quantizer is concerned, function $f(\mathbf{u})$ that implements the quantizer logic, is an odd function and a look-up table (LUT) is a viable and efficient method for its hardware implementation. For example, in the case of $k = r = 3$, using 6 bits for each of the 4 quantizer inputs, results in $(4 \cdot 6) = 24$ input bits. Each input combination is stored in the LUT as 1 bit. As mentioned before, due to the odd symmetry of the LUT, a total of $2^{24-1} = 8.389$ MBits need to be stored which can be further reduced by one or two orders of magnitude from the logic optimization during synthesis. In the aforementioned MSLA SDM with $k = r = 3$ and a 6 bit input (1 sign bit, 2 integer bits and 3 fractional bits), we synthesized it for in a Xilinx Kintex-7 FPGA KC705 Evaluation Kit target device. The implementation result utilizes only 2.58% of the FPGA resources. The complete analysis of the results is summarized in Table I.

C. MSLA SDM in an All-Digital Frequency Synthesizer System

As a practical application, the MSLA SDM can be used as a part of an all-digital frequency synthesizer system [9], [10]. Its purpose is to filter the given input and shape the quantization noise outside the desired frequency band [10]. A DDS generates a high-resolution digital sinusoidal signal that is afterwards fed to the MSLA SDM for 1-bit quantization.

TABLE I
MSLA SDM QUANTIZER DETAILED SYNTHESIS RESULTS

Primitive	Description	Used	Utilization
LUT6	6-input LUT	4244	2.58%
LUT5	5-input LUT	390	
LUT4	4-input LUT	310	
LUT3	3-input LUT	802	
LUT2	2-input LUT	462	
MUXF7	16:1 multiplexer	10	$< 0.01\%$

A frequency synthesized control word w is used to select the output frequency as $f_{\text{synth}} = (w/2^N)f_{\text{clk}}$, where N is the bit-width of the phase accumulator. The complete system architecture is shown in Fig. 7. The output bandwidth given the clock of the system, f_{clk}, is directly related to the OSR by:

$$\text{BW}_{\text{out}} = f_{\text{clk}}/(2 \cdot \text{OSR}). \tag{1}$$

From (1) it is clear that as the value of the OSR decreases, the BW is increased but at the cost of increased in-band noise and reduced SNDR. In Figs. 8 and 9 the output spectra are depicted and support the aforementioned statement $\text{OSR} = 32$ and $\text{OSR} = 128$ respectively. The range of frequencies that can be generated is determined solely by the NTF central frequency for band-pass, the OSR and the system frequency:

$$f_{\text{synth}} \in \left[f_0 - \frac{1}{4 \cdot \text{OSR}} f_{\text{clk}}, f_0 + \frac{1}{4 \cdot \text{OSR}} f_{\text{clk}} \right] \tag{2}$$

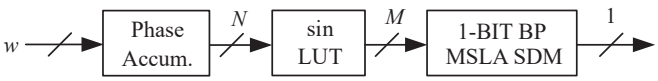

Fig. 7. All-digital frequency synthesizer using a 1-bit band-pass MSLA SDM.

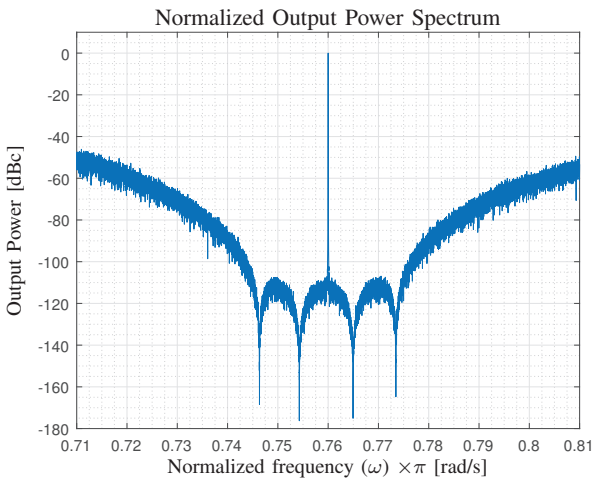

Fig. 8. Output bandwidth of MSLA SDM with OSR = 32

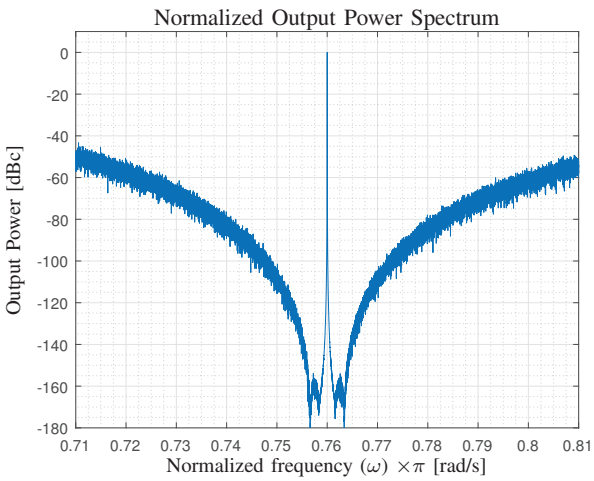

Fig. 9. Output bandwidth of MSLA SDM with OSR = 128

IV. CONCLUSION

In this work MSLA SDMs and the fundamentals of its operation were presented. The advantages of MSLA SDMs over the conventional single-bit SDMs in terms of SNDR were shown to be significant. It was also demonstrated that the number of look-ahead steps k and the order of the NTF play a crucial role when selecting the target SNDR as well as the NTF out-of-band gain. Finally, in terms of hardware efficiency, the quantizer implementation as a LUT was presented and its hardware requirements were quantified.

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