Efficient All-Digital Frequency Synthesizer Based on Multi-Step Look-Ahead Sigma-Delta Modulation

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***Abstract*—An all-digital frequency synthesizer system architecture with single-bit digital output generating frequency signals while shaping the quantization noise outside of the useful frequency range is presented. The system uses two identical low-pass single-bit Multi-Step Look-Ahead Sigma-Delta modulators (MSLA SDMs) in a quadrature (I-Q) configuration driven by two multi-bit digital orthogonal sinusoidal signals generated by a direct digital synthesizer (DDS). MSLA SDMs operate in the baseband and their outputs are interleaved and frequency up-converted to generate the desirable high-frequency output signal. The system architecture and the hardware complexity of it are parametrized on the number of look ahead steps, the Over Sampling Ratio (OSR) and the filter's order of the MSLA SDMs as well as on the balance between OSR, desirable frequency range span and Signal to Noise and Distortion Ratio (SNDR).**

***Keywords*—all-digital synthesizer, frequency synthesizer, noise shaping, single-bit quantization, sigma-delta modulation**

I. Introduction

The need for all-digital systems has been increasing due to the advantages of digital integrated circuits as technologies continue to scale down. Digital frequency synthesis is an application that can benefit from all-digital designs. Pure analog or mixed-signal frequency synthesizers lack the digital accuracy, fine frequency resolution and the fast frequency hopping of digital frequency synthesizers. Furthermore, digital circuits offer additional advantages such as immunity to process, voltage and temperature variations (PVT), scalability, reconfigurability, faster design cycles, smaller chip area etc.

In order to avoid the use of analog or mixed-analog components in an all-digital system, a direct digital synthesizer (DDS) is crucial for the input sequence [1]. However, a digital to analog (DAC) converter is required for the conversion of the multi-bit output to analog. A purely digital alternative to DDS is the single-bit-output pulse direct digital synthesizer (PDDS). The drawback of the PDDS is that it introduces frequency spurs and a high noise floor [2]. In contrary, a DDS combined with a digital single-bit band-pass delta-sigma modulator (SDM) [3], can shape the quantization noise out of the desired frequency band and overcome the issue of the multi-bit DAC [4]. The most important limiting factor for the highest possible generated frequency is the operating frequency of the SDM. It should be at least twice that of the generated frequency and also, depending on the required bandwidth, it should be higher than the oversampling ratio (OSR) times the bandwidth.

Higher synthesizable frequencies can be achieved by applying two low-pass SDMs in quadrature configuration and using 3 multiplexers for interleaving and upsampling [5]. The two low-pass SDMs are clocked at half the frequency of the third multiplexer. An optional fourth multiplexer can be used in order to further increase the the generated frequencies.

In this work we propose to use Multi-Step Look-Ahead SDMs, further improving upon the noise shaping characteristics and the stability of conventional single-bit SDMs [6]. This is achieved by considering both current and future quantization errors to calculate the output whereas conventional SDMs take into account only current quantization errors. As a result, more aggressive noise transfer functions (NTFs), i.e. NTFs with higher out-of-band gain, can be used, leading to increased signal-to-noise-and-distortion-ratio (SNDR). Moreover, the output bandwidth range can be adjusted according to the OSR [3].

The following section provides a brief explanation of the MSLA SDM operation as well as the frequency synthesis system architecture that we propose. Section III gives a complete analysis with simulations and test cases and finally section IV concludes the discussion.

II. Frequency Synthesizer Based on MSLA SDMs in Quadrature Upconversion Scheme

In the first part of this section a detailed description of the proposed frequency synthesizer architecture is given. In the second part, a detailed analysis of the MSLA SDM operation is put forward.

A. Frequency Synthesizer Architecture

The proposed frequency synthesizer architecture is shown in Fig. 1. The two DDS's generate two orthogonal sinusoidals with frequency:

$$f_{BB} = \left(w/2^N\right) f_{clk}.$$

The frequency control word (FCW) w is responsible for selecting the frequency to be synthesized. The bit-width of the phase accumulator is noted as N and defines the generated frequency resolution. For the I and Q configuration a $\pi/2$ phase difference is mandatory in order to avoid images in

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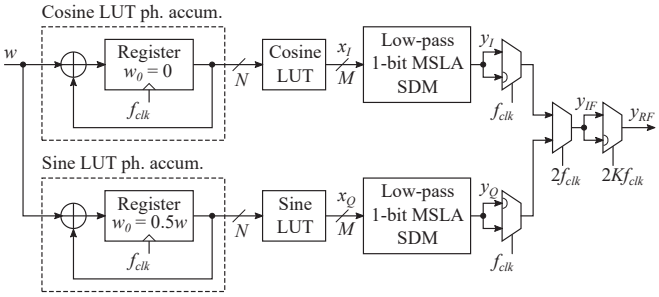

Fig. 1. All-digital frequency synthesizer using two 1-bit low-pass MSLA SDMs in quadrature configuration.

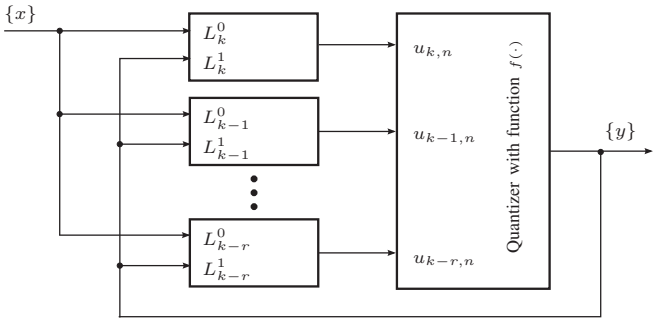

Fig. 2. The MSLA SDM system diagram.

the output spectrum. Therefore, the initial value of the sine look-up table (LUT) phase accumulator is $w_0 = 0.5w$ while the value of the corresponding cosine LUT phase accumulator is $w_0 = 0$. Afterwards the two DDS sinusoidal outputs, x_I and x_Q, are fed into two identical low-pass MSLA SDMs to convert the multi-bit output to a single-bit one. Each of the outputs is then up-converted using a multiplexer. A third multiplexer is used for the addition of the two resulting signals. This intermediate frequency signal y_{IF} has frequency:

$$f_{IF} = (f_{clk}/2) + f_{BB}. \tag{1}$$

As mentioned before, another multiplexer is capable of generating higher frequencies. This multiplexer has a sampling rate of $2Kf_{clk}$. The final synthesizable frequencies are given by:

$$f_{RF,i} = mf_{clk} \mp (f_{IF}/2)\,,\ 0 \le m \le K,\ m \in \mathbb{N}^+, \tag{2}$$

with the constraint of $0 \le f_{RF,i} < Kf_{clk}$. The value of m defines the number of available frequency bands to be synthesized and therefore must be chosen appropriately.

The MSLA SDM OSR is chosen in relation to the desired output bandwidth. The intermediate signal frequency range for a given OSR is:

$$\mathrm{BW}_{IF} = \left[\frac{f_{clk}}{2} - \frac{f_{clk}}{2\cdot\mathrm{OSR}}, \frac{f_{clk}}{2} + \frac{f_{clk}}{2\cdot\mathrm{OSR}}\right] \tag{3}$$

Moreover, the frequency range of the final output signal y_{RF} is:

$$\mathrm{BW}_{RF} = \left[mf_{clk} \mp \frac{f_{clk}}{4} - \frac{f_{clk}}{2\cdot\mathrm{OSR}}, mf_{clk} \mp \frac{f_{clk}}{4} + \frac{f_{clk}}{2\cdot\mathrm{OSR}}\right] \tag{4}$$

B. MSLA SDM Operation

In Fig. 2 the complete MSLA SDM system is depicted. It consists of $r+1$ two-input IIR filters (L_j^0, L_j^1), where $k-r \le j \le k$, and an $(r+1)$-input quantizer. As the number of look-ahead steps k increases, the performance of the MSLA SDM increases accordingly. The term look-ahead does not imply that any future input samples are predicted. Instead, the input is delayed by k samples. Parameter r determines the number of partial quantization errors to be taken into account and takes values from 0 to k. As shown in [6] the highest increase in performance is observed for $r = k$, when $k > 3$ and $k \in \{3, 4, 5, 6, 7, 8\}$. An in-depth description and analysis of MSLA SDMs is given in [6].

The NTF order, the OSR and the NTF out-of-band gain determine the in-band noise and the SNDR. As the OSR increases, the SNDR also increases but with the cost of reduced useful output bandwidth, which is a design trade-off. Another design concern is the stability of the NTF [7], [8] which is directly associated to the out-of-band gain $||NTF||_\infty$; while the number of look-ahead steps k and the OSR increase, the maximum allowable gain also increases, resulting in higher SNDR. To maintain the theoretical SNDR a clock signal with low enough phase noise can be used.

C. The Synthesizer Transfer Functions

The NTF of the frequency synthesizer at signal point y_{IF} can be easily derived by using the transformation $z \to -z^2$ to convert the low-pass NTF to band-pass [3], namely

$$NTF_{BP}(z) = NTF_{LP}(z)|_{z=-z^2}. \tag{5}$$

The NTF at the position of the output signal y_{RF} is derived from NTF_{BP}. The effect of the fourth multiplexer can be modeled as the multiplication of signal y_{IF} with a cosine wave having frequency $\omega = \pi$ or $f = Kf_{clk}$. To apply the previous observation we first need to convert the discrete-time $y_{IF}[n]$ to the equivalent continuous-time one $y_{ZOH,IF(t)}$ using the zero-order hold transformation:

$$y_{ZOH,IF}(t) = \sum_{n=0}^{\infty} y_{IF}[n] \cdot \mathrm{rect}\left(\frac{t - \frac{1}{2}nT_{clk}}{\frac{1}{2}T_{clk}} - \frac{1}{2}\right) \tag{6}$$

where $T_{clk} = 1/f_{clk}$. Therefore, the continuous time y_{RF} signal is

$$y_{RF}(t) = y_{ZOH,IF}(t) \cdot \cos(2\pi K f_{clk} t). \tag{7}$$

To describe the frequency-domain behavior of the proposed synthesizer we take the Fourier transfroms of the involved signals:

$$Y_{ZOH,IF}(f) = H_{ZOH}(f) \cdot Y_{IF}(f) \tag{8}$$

where:

$$H_{ZOH}(f) = e^{-j\pi f \frac{T_{clk}}{2}}\ \frac{\sin(\pi f \frac{T_{clk}}{2})}{\pi f \frac{T_{clk}}{2}}. \tag{9}$$

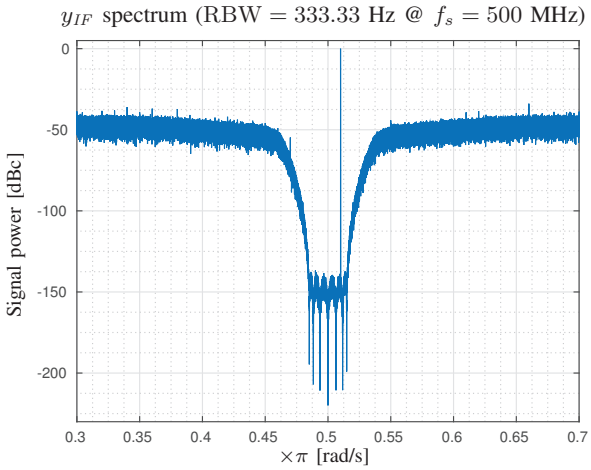

Fig. 3. Spectrum of the frequency synthesizer output y_{IF}.

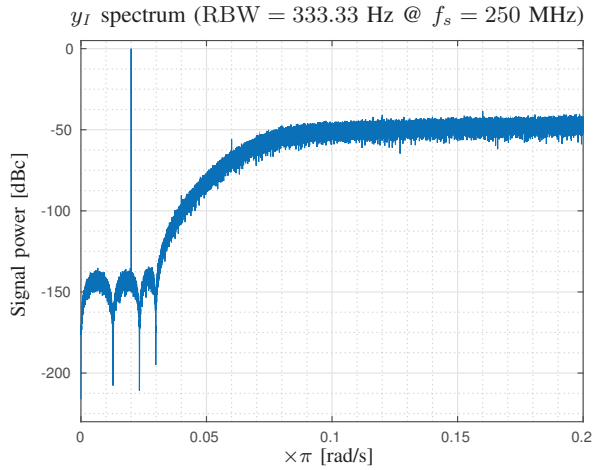

Fig. 4. Spectrum of the MSLA SDM output y_I.

The fourier transform of (7) is the convolution of the Fourier transforms of $y_{RF}(t)$ and $\cos(2\pi K f_{clk} t)$, i.e.:

$$Y_{RF}(f) = \left[e^{-j\pi f \frac{T_{clk}}{2}} \frac{\sin(\pi f \frac{T_{clk}}{2})}{\pi f \frac{T_{clk}}{2}} \cdot Y_{IF}(f) \right] * \frac{\delta(f - K f_{clk}) + \delta(f + K f_{clk})}{2}. \quad (10)$$

So, the initial NTF_{BP} is first transformed by the ZOH transfer function, including the upsampling operation, and afterwards by its convolution with the spectrum of the cosine signal with frequency $f = K f_{clk}$, consisting of two delta functions located at frequencies $f \pm K f_{clk}$.

III. Design Choices and Simulation Results

In order to investigate the behavior of the proposed system architecture, several design parameter choices were tested. For the system shown in Fig. 1, the I and Q inputs are $x_I = 0.4\cos(2\pi \cdot 0.01n)$ and $x_Q = 0.4\sin(2\pi \cdot 0.01(n+0.5))$ respectively. The order of the low-pass MSLA SDM NTF is 7, OSR = 32 and $r = k = 6$. The clock frequency used is $f_{clk} =$ 250MHz and therefore the sampling frequency was twice that value, namely $f_s = 500$MHz. The resolution bandwidth is RBW = 333.33Hz and results to a spurious-free dynamic range (SFDR) of DR $= -137\,\text{dB} - 10\log_{10}(\text{RBW}) = -162\text{dBc/Hz}$. In Fig. 3 the output spectrum of y_{IF} is shown with SNDR of SNDR = 104.5dB. It is clear that for a specific OSR, so high SNDR cannot be achieved using conventional single-bit SDMs. It is also noteworthy that the spectra of y_I and y_Q are identical. The spectrum of y_I is depicted in Fig. 4.

As mentioned in the previous section, the use of a fourth multiplexer further increases the frequency ranges that can be generated. In our case, a value of $K = 2$ is used, which leads to a sampling frequency of $f_s = 4f_{clk} = 1$GHz for the final multiplexer. The power spectrum is shown in Fig. 5. A zoom-in of that spectrum around the frequency corresponding to $m = 2$ and the minus sign is depicted in Fig. 6. Since

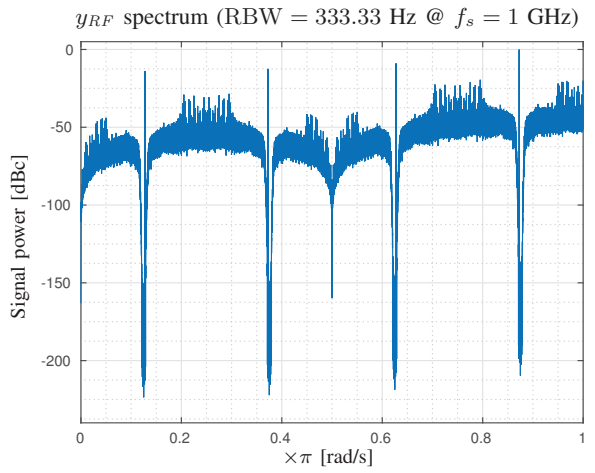

Fig. 5. Spectrum of the the frequency synthesizer output y_{RF} for $K = 2$.

$f_{BB} = 0.01 f_{clk} = 2.5$MHz frequency $f_{IF} = 125 + 2.5\text{MHz} = 127.5$MHz. The generated frequencies are:

$$\begin{aligned} f_{RF,1} &= 0 \cdot 250 + 63.75 \text{ MHz} = 63.75 \text{ MHz} \\ f_{RF,2} &= 1 \cdot 250 - 63.75 \text{ MHz} = 186.25 \text{ MHz} \\ f_{RF,3} &= 1 \cdot 250 + 63.75 \text{ MHz} = 313.75 \text{ MHz} \\ f_{RF,4} &= 2 \cdot 250 - 63.75 \text{ MHz} = 436.25 \text{ MHz}. \end{aligned}$$

Another design of the proposed system is to consider not only the multiplexer frequency range that can be generated but also the MSLA SDM parameters that have immense impact on the hardware implementation. In Fig. 7 it is shown that the number of look-ahead steps k and the OSR directly affect the observed SNDR; while both parameters are increased, SNDR also increases, but at the cost of lower bandwidth as suggested by (3). It was also mentioned that the maximum NTF out-of-band gain resulting in stable operation decreases as the OSR increases. This is justified in Fig. 8, for $OSR \in$

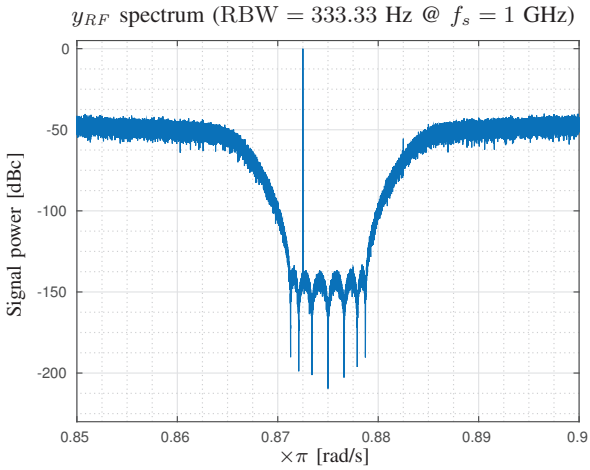

Fig. 6. Zoomed-in spectrum of the the frequency synthesizer output y_{RF}.

$\{16, 32, 64, 128, 256\}$ and $k \in \{0, 3, 4, 5, 6, 7, 8\}$. For the special case of $k = 0$, the MSLA SDM is equivalent to a single-bit conventional one. Both Figs. 7 and 8 indicate that the MSLA SDMs exhibit superior performance than conventional single-bit ones.

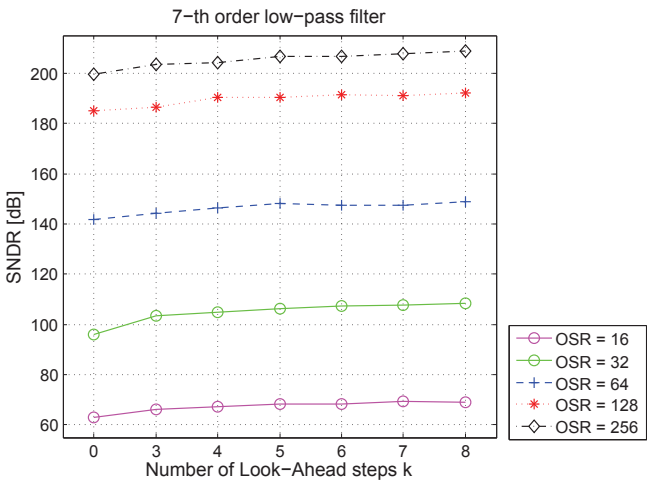

Fig. 7. MSLA SDM 7-th order low-pass filter SNDR vs look-ahead steps k as the OSR increases.

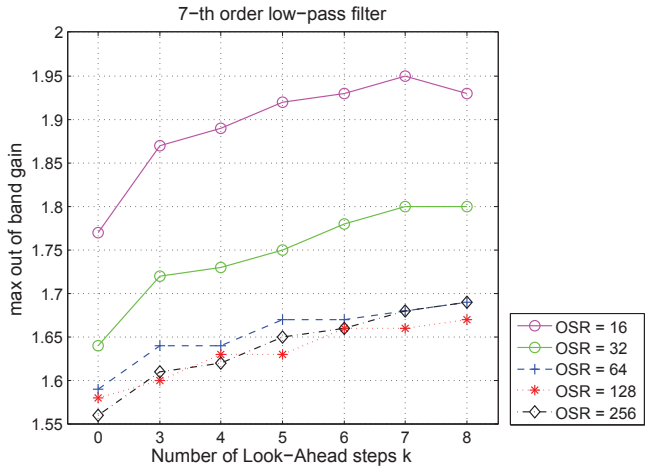

Fig. 8. MSLA SDM 7-th order low-pass filter maximum out-of-band-gain vs look-ahead steps k as the OSR increases.

IV. Conclusion

The overall performance of single-bit MSLA SDMs over conventional single-bit ones is found to be significant. The presented all-digital frequency synthesizer system architecture is well capable of generating various frequency ranges using two low-pass MSLA SDMs in quadrature configuration. The only limiting factor is the operating frequency of the final multiplexer and therefore synthesis of high frequencies, for example in the GHz range, is possible. The system is all-digital apart from a band-pass analog filter for the attenuation of the out-of-band quantization noise which might be required by some applications.

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