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A CMOS Closed Loop AMR Sensor Architecture

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***Abstract*—A fully analog, closed loop, signal conditioning circuit is presented for the readout of Anisotropic Magneto-Resistance magnetic sensors. The architecture is based on a fully differential design, consisting of an instrumentation amplifier with chopping to achieve low output noise, followed by a trans-conductor. The output current of the transconductor is directly fed back to the sensor, through a dedicated on-chip inductor for magnetic field offsetting purposes, closing this way a negative feedback loop. The proposed design has been implemented and simulated in TSMC 180nm $5\,\mathrm{V}$ CMOS process.**

***Keywords*—AMR, CMOS, Signal Conditioning**

I. Introduction

Accurate and reliable measurements of magnetic fields has been a critical part in many technical areas. Compasses, magnetic storage disks, non-contact switches and current sensors are just a few examples of the numerous applications in which magnetic sensors are being extensively used.

Several solutions are available, that offer very high sensitivity [1]. However, most of them are large in size, and, therefore, they turn out to be unsuitable for small form factor applications, such as hand held devices and nano-satellites. Fluxgates, consisting of magnetically coupled coils around a high permeability core, tend to be bulky and take up space, especially when discrete electronics come into play. Superconducting Quantum Interference Devices (SQUIDs), although being very small themselves, need to be cooled down to extremely low temperatures, usually by the means of liquid helium. This makes them, as a complete instrument, even heavier than fluxgates. Apart from this inconvenience, their bandwidth is limited to very low frequencies, bellow $1\,\mathrm{Hz}$. While search coils, resembling fluxgates in size, are based upon Faraday's law of induction and therefore, in contrast to SQUIDs, are unable to measure dc and low frequency fields.

Anisotropic Magneto-Resistance (AMR) sensors on the other hand, being composed of ferromagnetic thin film resistive strips, are bulk manufactured on silicon wafers. This not only allows them to be available in a variety of commercial IC packages, but also opens the possibility for them to be co-assembled with other necessary readout circuitry and systems. This key benefit, in addition to the ever growing field of Application Specific Integrated Circuits (ASICs), has given AMR sensors the opportunity to emerge as a very attractive and promising alternative, which offers a good balance between performance and cost [2].

In this work we present the design of a fully analog, CMOS, closed loop signal conditioning circuit (SCC), which targets the HMC1001/2 family of AMR sensors by Honeywell. Not only does this SCC open the possibility of integration with the sensors themselves, but it also aims to improve upon their performance in terms of linearity and temperature insensitivity. First, a brief description of these sensors' structure, characteristics and non idealities is carried out in **Section 2**. In **Section 3**, the complete system architecture of the closed loop is presented and each of its key blocks is analyzed separately, while **Section 4** reports the achieved improvements along with our conclusions.

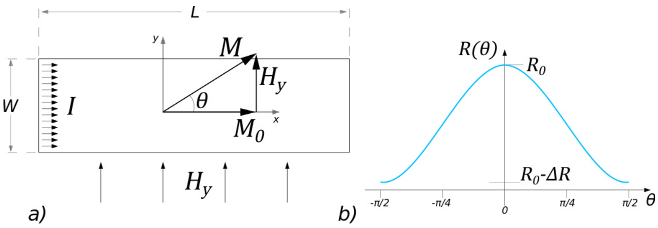

Fig. 1: **(a)** NiFe permalloy sensing strip of length L and width W showing a distinct inner magnetization M_0 along the x-axis and **(b)** it's R(θ) versus θ DC transfer characteristic.

II. Structure, Characteristics and Non Idealities of the AMR Sensors

Magnetoresistive sensors are made of a nickel-iron alloy (NiFe permalloy) thin film, which is deposited onto a silicon wafer and patterned as a resistive strip [3]. During manufacturing, they are subjected to a strong magnetic field which sets their preferred axis of magnetization or magnetization vector M_0, parallel to their length (x-axis, see **Fig.1(a)**). If no external magnetic field is present, the magnetic domains of the strip remain aligned with their inner magnetization vector M_0 and, hence, are parallel to the current I flowing through the strip. Therefore $\theta = 0°$, where θ is the angle the magnetic domains form with respect to the flow of current I. Under these conditions the strip has maximum resistance R_0. However, when an external magnetic field H_y is applied perpendicularly to the length of the strip or parallel to the y-axis (the y-axis is the axis of sensitivity), it causes the magnetic domains to rotate : $M_d = M_0 + H_y$ and the angle θ to increase depending on the strength of the applied magnetic field. This causes the strip's electrical resistance to decrease anywhere from $2\,\%$ to $3\,\%$ (see **Fig.1(b)**). This effect, is known as the anisotropic magneto-resistance effect. It was discovered by William Thompson in

1897, it has a very fast response ($1\,\mathrm{MHz}$ to $5\,\mathrm{MHz}$) and it can be roughly approximated by the following equation :

$$R(\theta) = R_0 - \Delta R sin^2(\theta) \tag{1}$$

Since the AMR effect follows a square-sine relation, the strip is not capable of sensing magnetic field polarity [3]. To correct this, a method called "barber pole biasing" (bpb) is employed (see **Fig.2(a)**). This is accomplished through a layout technique that places high-conductivity (aluminum or copper) shorting bars at a 45° angle across the film's width. The current preferring to take the shortest path through the film, flows from one bar to the next at an angle ϕ of -45°. As a result the strip's AMR operating point is shifted down to R_0 - ΔR/2 [3], a region of its characteristic which is also more linear. (solid curve in **Fig.2(b)**).

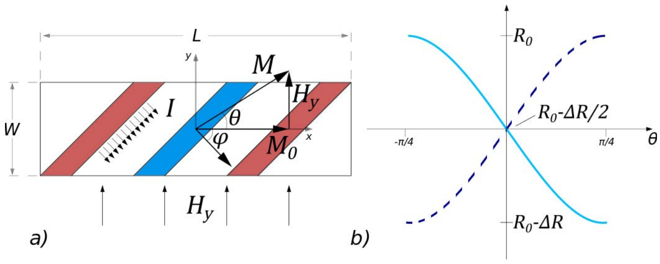

Fig. 2: **(a)** Permalloy strip with bpb. **(b)** The shifted characteristics of the permalloy strip for 45° angle (solid line curve) and -45° angle (dashed line curve) bpb.

Similarly the permalloy strip can be manufactured with opposite direction, -45° angle barber poles, resulting in a 45° angle ϕ of current flow with respect to M_0 and a mirrored characteristic (dashed curve of **Fig.2(b)**). In order to maximize the otherwise low sensitivity and limit the large temperature dependency ($0.3\,\%/°\mathrm{C}$) of a single AMR device, four of these permalloy strips are combined to form a Wheatstone Bridge. Two strips with 45° angle and two strips with -45° angle bpb are placed diagonally to take full advantage of the bridge topology. Now both magnitude and polarity can be sensed.

Despite these improvements, the AMR sensors still present a high non-linearity ($1\,\%$FS to $2\,\%$FS), a considerable temperature coefficient ($-0.10\,\%/°\mathrm{C}$) (see **Fig.7**), a high offset voltage ($-60\,\mathrm{mV}$ to $30\,\mathrm{mV}$ when excited at $5\,\mathrm{V}$) and a tendency of the magnetic domains to lose their magnetization alignment M_0. This is of concern since the AMR effect behaves well, with low noise and good repeatability only when the domains of the films are all aligned correctly, parallel to M_0. To ensure this a dedicated on-chip inductor called the Set / Reset (S / R) strap has been placed very close to the permalloy strips and parallel to M_0. When a switching current pulse is passed through this inductor, it generates a strong pulsed magnetic field in the direction of M_0, which effectively realigns the film's domains. Similar to S / R strap, a second on-chip inductor, the Offset strap, is also provided which serves for static magnetic field nulling purposes. In our case however, it is used as a feedback element, in order for the sensor to operate in a negative feedback loop.

III. The Closed Loop Architecture

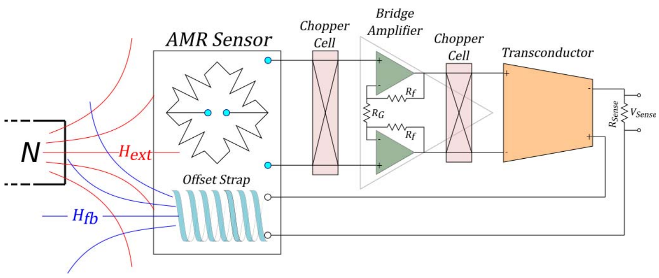

Fig. 3: Block diagram of the closed loop architecture

The complete circuit architecture including the sensor, is illustrated in **Fig.3**. It consists of a chopper stabilized bridge amplifier, followed by a simple transconductor connected back to the sensor through the offset strap and in series with a sense resistor R_{Sense}. Its principle of operation is as follows.

When an external magnetic field H_{ext} is applied to the sensor, the bridge instantaneously becomes unbalanced. Immediately the negative feedback loop is activated. It senses this voltage, amplifies it by the bridge amplifier accordingly and then converts it into a current by the transconductor which drives the offset strap to generate an opposing magnetic field, H_{fb}, to the external one being measured. The two fields cancel each other out (H_{ext} - H_{fb} $\approx$ 0) and the bridge's output voltage is driven very close to zero. The resulting current that is required to cancel the applied field is measured using the resistor, R_{Sense}, which generates a voltage drop across it, V_{Sense}. This is a direct measure of the applied magnetic field's strength.

A. *Bridge Amplifier*

The amplifier configuration employed here is that of a typical instrumentation amplifier's first stage. Two identical single-ended operational amplifiers (opamps) are connected by three resistors, of which the two, R_f, are the same and the third, R_G, sets the gain according to :

$$A_v = 1 + 2R_f/R_G \tag{2}$$

The result is a fully differential non-inverting bridge amplifier (BA). Although this configuration consumes slightly more power compared to traditional fully differential opamps it's advantages are that it presents very high input impedance, so as to not load the AMR sensor, allowing at the same time small value gain-setting resistors to be used in order to keep noise levels low. Here, resistances of R_f = $50\,\mathrm{k\Omega}$ and R_G = $1\,\mathrm{k\Omega}$ produce a set gain of 100 ($40\,\mathrm{dB}$), at a bandwidth of $500\,\mathrm{kHz}$ and an input referred broadband noise of $10\,\mathrm{nV}\,\sqrt{\mathrm{Hz}}^{-1}$.

As for the internal structure of each opamp, a 2-stage amplifier topology is chosen which is illustrated in **Fig.4**. The design shown consists of a differential-input, single-ended output Folded Cascode amplifier with a PMOS differential input pair $M_{1,2}$ and NMOS common gate transistors $M_{5,6}$, followed by a PMOS common source output stage M_{12}. All the bias currents in the circuit are generated by wide swing

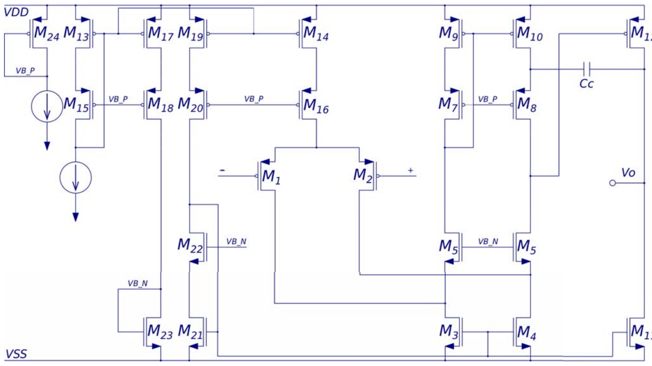

Fig. 4: Schematic diagram of the operational amplifiers.

cascode current mirrors. These provide high output impedance, thereby maximizing dc gain and CMRR, without reducing output swing [4].

Finally, by connecting a $2\,\mathrm{pF}$ capacitor C_C from the opamp's output to the drain of M_{10}, indirect feedback compensation is performed. This compensation technique not only saves physical space compared to traditional $RC - Miller$ compensation, but also provides excellent stability margins, and better supply noise rejection [5]. A list of the opamp's simulated parameters is given bellow :

Parameter	Achieved Value
Power Supply Voltage	+5V (single)
Small-Signal DC Gain	$100\,\mathrm{dB}$
Unity-Gain Frequency	$60\,\mathrm{MHz}$
Phase Margin	$75.94°$
Gain Margin	$12.45\,\mathrm{dB}$
Settling Time($0.1\,\%$ Error)	$27\,\mathrm{ns}$ rise, $22\,\mathrm{ns}$ fall
Current Consumption	$2.312\,\mathrm{mA}$
Input Referred Noise (Broadband)	$7\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$

The large-signal step response and settling time measurement were acquired applying a $1\,\mathrm{V}$ amplitude step waveform, the opamp being in unity-feedback configuration with a $2.5\,\mathrm{V}$ input common-mode voltage and a $1\,\mathrm{pF}||20\,\mathrm{k\Omega}$ load. Rise time was measured to be $27\,\mathrm{ns}$, while fall time was less, at $22\,\mathrm{ns}$ - a quite fast response which is absolutely recommended, if chopping is to be applied.

B. Chopping Modulation

Chopping is a continuous-time modulation technique that makes use of polarity-reversing switches, known as choppers, placed at the input and output of an amplifier to modulate its low frequency errors such as $1/f$ noise, offset, and offset drift to the modulating frequency f_{chop}, which is usually set to be much higher than the frequency band of interest. These frequency shifted errors can then be filtered out by using a low pass filter, enabling this way the realization of low noise and low offset CMOS amplifiers.

An additional benefit of this technique in our circuit is that it effectively isolates the sensor's offset voltage, which also has it's own drift ($\pm 0.03\,\%/°\mathrm{C}$), making calibration of the complete system much easier.

The chopper modulators used in the proposed design, which can be seen in **Fig.5**, are implemented with Complementary MOS switches, also known as transmission gates, each placed in between two half-sized dummy ones, which help to minimize the effects of channel charge-injection and clock feed through [6]. The choice of CMOS, instead of simple NMOS or PMOS switches also improves the linearity of the switch over a wider voltage range [7].

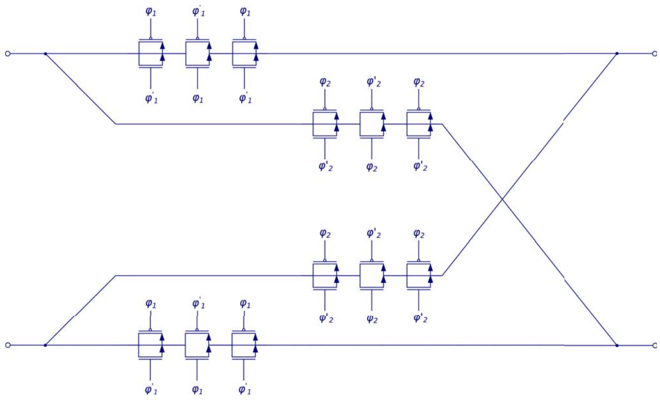

Fig. 5: Schematic diagram of the chopper cells.

C. Transconductor

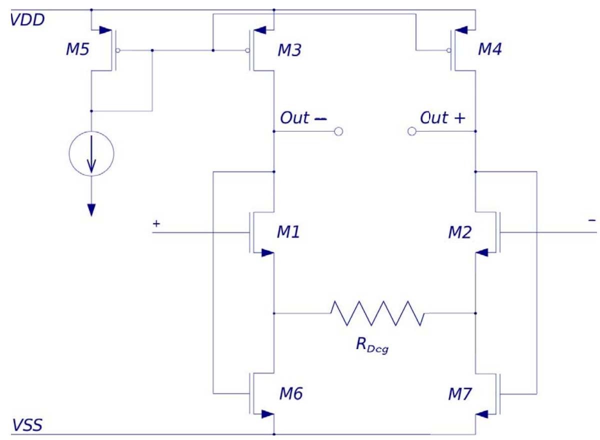

Fig. 6: Schematic diagram of the transconductor.

The circuit responsible for converting the BA's output voltage into a current to be fed back to the AMR sensor is the transconductor illustrated in **Fig.6**. Required to deliver up to $100\,\mathrm{mA}$ to the sensor's offset strap ($51\,\mathrm{mA\,G^{-1}}$), this is also the most power hungry circuit of the architecture. Resistor R_{Deg} improves linearity, while $M_{6,7}$ set the output common-mode voltage by operating in the triode region.

IV. Simulation Results and Conclusions

The proposed closed loop architecture has been designed in TSMC $180\,\mathrm{nm}$ high voltage CMOS process, with a single

5 V power supply. The choice of this process was due to the possibility of ratiometric excitation, since the AMR sensors' recommended voltage supply is also 5 V. Cadence® Spectre® simulations give a total power consumption of 1.3 W for the complete system, including the additional circuitry not presented here such as biasing circuitry and the non overlapping clock generator needed for the choppers.

A comparison of the new closed loop DC transfer characteristics obtained at an R_{Sense} of $1\,\Omega$, with the sensors' typical open loop characteristics can be seen in **Fig.7**. The improvements in linearity as well as in temperature insensitivity are evident.

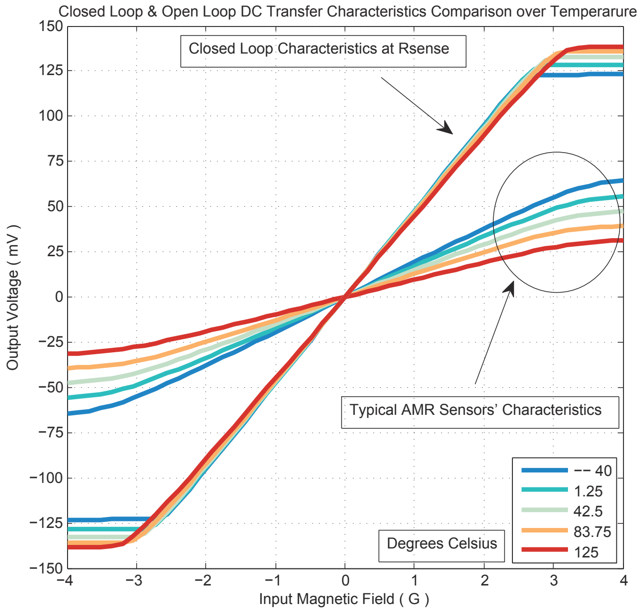

Fig. 7: Comparison of Open and Closed Loop DC transfer characteristics over the recomended temperature op. range.

The sensors' recommended temperature operating range is $-40°\mathrm{C}$ to $125°\mathrm{C}$. For temperatures above $125°\mathrm{C}$ the sensors' permalloy films approach their Currie temperature T_C, where they loose their ability to sense magnetic fields; as a result the sensor's performance degrades dramatically. No signal conditioning methodology can compensate for this, except for local temperature control.

To test the chopping operation, we set f_{chop} to 100 kHz, a frequency well inside the BA's bandwidth, and drive the model of our sensor with a sinusoidal input of 1 G and 1 kHz. The output spectrum, which is shown in **Fig.8**, points out the expected, demodulated fundamental tone found at 1 kHz, and at a strength of -26.48 dB, accompanied by chopping artifacts located at integer multiples of $2f_{chop}$. The second strongest tone between 0 and 10 kHz, which is found at 3 kHz and at -98.43 dB, denotes a spurs-free dynamic range of 71.95 dB.

Finally, **Fig.9** illustrates the closed loop's frequency response over temperature, without considering chopping. Ranging from ≈300 kHz to ≈900 kHz for 125°C and - 40°C, respectively, it makes the closed loop architecture also perfectly capable of sensing higher frequency fields. For even

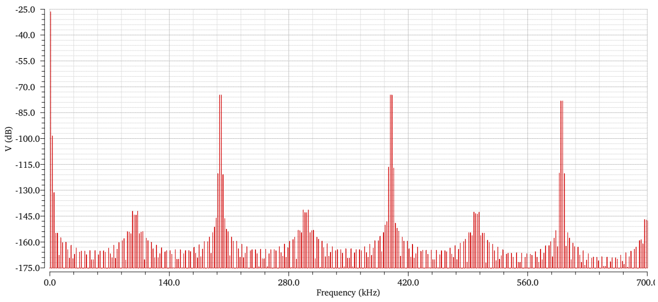

Fig. 8: Output spectrum at R_{Sense} of a 1 G, 1 kHz input signal.

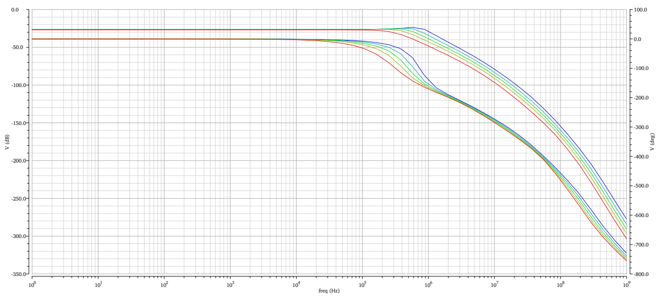

Fig. 9: Frequency response without chopping

higher frequency magnetic sensing, search coils would be preferred, as they have the best behavior compared to all other magnetometers. However, the challenge in magnetometry is to achieve high resolution measurements at low frequencies, where $1/f$ noise is the dominant factor.

A CMOS closed loop AMR sensor architecture is presented, comprising simple analog signal processing blocks, including chopping to suppress the aforementioned low frequency errors, thus making it a capable ASIC for low frequency applications, such as geomagnetic research. Simulation results demonstrate enhanced performance in terms of linearity, temperature insensitivity and noise, all of which encourage its real-life implementation.

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