Rail-to-Rail Operational Amplifier with Stabilized Frequency Response and Constant-gm Input Stage

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***Abstract*—In this paper a 3 V input and output Rail-to-Rail operational amplifer is designed in a 0.6 µm CMOS technology. It uses a complementary differential input stage, a simple class-A output stage and two current compensation networks. The first provides constant transconductance at the input by varying the square root of the input pairs' tail currents. The second ensures an almost constant frequency response throughout the entire common mode range of operation. Simulations show a maximum variation of only 9 % and 30 % for PM and GM respectively. Large-signal step response achieves a 0.1 % settling time lower than 32 ns, while its quiescent power consumption is 3.7mW.**

***Index Terms*—Operational Amplifier, Rail-to-Rail, Constant gm, Stabilized Frequency Response**

I. Introduction

Low power analog integrated circuit operation is always desirable in modern systems. Operational Amplifiers (opamps) being the key building block of such systems must be designed accordingly. It is crucial that the dynamic range of their operation is kept as wide as possible, while operating at a low supply voltage [2], [3], [4], [5].

The most common way to maximize the input common mode range is by using two complementary differential input pairs [7] as shown in Fig. 1a. However, this topology on its own presents a serious drawback. When both differential pairs are active *(Region II)*, its transconductance (gm) is twice that of when only one pair is on and the other is off *(Region I or III)*. This large variation of the input stage's transconductance (Fig. 1b) makes optimal frequency compensation impossible, which in turn can lead to severe unity gain bandwidth variations and even make the opamp unstable.

Several techniques to overcome this issue have been already proposed in the literature, and comparative studies have been carried out explaining the pros and cons of each of them [1]. Although they all provide constant gm at the input, not all of them ensure a constant frequency response of the opamp.

In this paper we shall demonstrate a design example of an input and output Rail to Rail opamp covering each of its stages separately throughout Section II. Then we will explain why an extra current compensation network is needed in order to obtain a relatively constant frequency response throughout the entire input common mode range of operation. The results of this work are presented in Section III, leading to the summary and conclusion of our endeavour in Section IV.

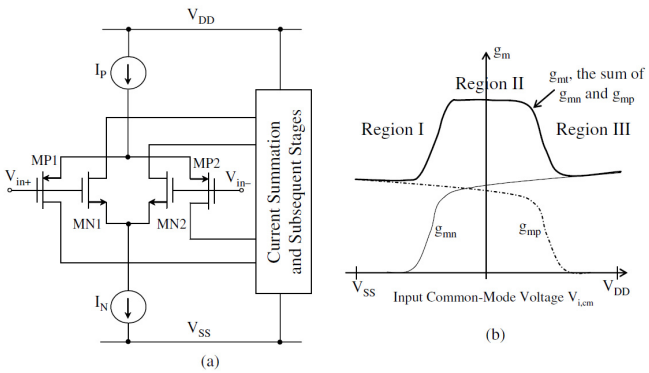

Fig. 1: Typical Input Stage, and its transconductance [1].

II. The Operational Amplifier

A. Constant-gm Rail-to-Rail Input Stage

The basic structure of the input stage is illustrated in Fig. 2. Transistors N1 and N2 form a NMOS differential pair, and transistors P1 and P2 form a PMOS differential pair.

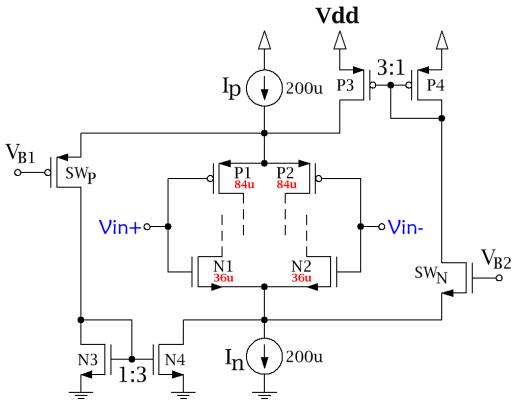

Fig. 2: Constant-gm Rail-to-Rail Input Stage.

Both pairs are biased by the same tail current: $I_n = I_p = I_{nom} = 200\,\mu\text{A}$. Furthermore they have been sized to have equal β_{eff} - meaning that $K_n = K_p = K$, where $K = \mu \cdot C_{ox} \cdot \frac{W}{L}$. This way the gm of each pair is the same [8].

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To achieve constant gm, two switches (SW_N and SW_P) and two current mirrors (N3, N4 and P3, P4) have been used to alter the effective tail currents I_n or I_p when the input common mode voltage V_{CM} exceeds the limits of proper operation of the PMOS differentail pair or the NMOS differential respectively. These switches are easily implemented using a transistor with its gate tied to a fixed bias voltage. The biasing circuit has been left out for simplicity.

The principle of operation for the three possible working regions is the following:

- When V_{CM} approaches the higher supply rail VDD and exceeds the upper limit of operation of the PMOS pair, the PMOS pair turns off while the NMOS pair remains active. As the PMOS pair turns off, the switch transistor SW_P gradually turns on and "steals" the bias current I_p. This current is now mirrored by a 1:3 current mirror - N3,N4 and added to the NMOS pair's tail current. The total current biasing the NMOS pair now is $I'_n = 3I_p + I_n = 4I_{nom}$, and its transconductance is: $g_{mn} = \sqrt{2K_n \cdot 4I_{nom}} = 2\sqrt{2K_n I_{nom}}$.
- When V_{CM} approaches the lower supply rail VSS and exceeds the lower limit of operation of the NMOS pair, the NMOS pair turns off while the PMOS pair remains active. As the NMOS pair gradually turns off, the switch transistor SW_N gradually turns on and "steals" the bias current I_n. This current is mirrored in a similar fashion by a 1:3 current mirror - P3,P4 and added to the PMOS pair's tail current. The total current biasing the PMOS pair now is : $I'_p = 3I_n + I_n = 4I_{nom}$ and it's transconductance is: $g_{mp} = \sqrt{2K_p \cdot 4I_{nom}} = 2\sqrt{2K_p I_{nom}}$.
- When V_{CM} is midway of the supply voltage ($V_{CM} \approx \frac{V_{dd}+V_{ss}}{2}$), both pairs are on and function together. The switches SW_N and SW_P are off and don't contribute to the operation of the stage. The total transconductance of the input stage is: $g_{m_{TOT}} = g_{mn} + g_{mp} = \sqrt{2K_n I_n} + \sqrt{2K_p I_p} = 2\sqrt{2KI_{nom}}$.

As a result of the above an almost constant input transconductance has been achieved. From the plotted simulation in Fig. 3, one can see the improvement of this technique over the simple circuit of Fig. 1a. It's well known that this technique still presents a variation of 15 % to 20 % as explained in [2], [1]. This is verified here by the two small "hills" in the plotted curve of gm, measuring less than 25 % higher than the nominal value of 1.45 mS.

B. Current Summation Stage

The output currents of the complementary differential pairs are added using the current summation stage which is illustrated in Fig. 4. The stage is composed of the following transistors: P5 and P6 are two current sources that provide bias currents to the NMOS differential pair and the other transistors that make up this stage. P7 and P8 are the folded common gate transistors of the NMOS differential pair. Together they form an NMOS folded cascode differential amplifier. Likewise, N7 and N8 are the folded common gate transistors of the PMOS differential pair and together they form a PMOS folded cascode differential amplifier. Finally, transistors N5 and N6 have a double role:

- they sink the bias currents of both the PMOS differential pair and the bias currents flowing through the common gate transistors.
- they form a wide swing cascode current mirror in combination with N7 and N8, serving to mirror and sum up the small signal ac currents comming from the two input pairs to a single output at the drains of P8 and N8.

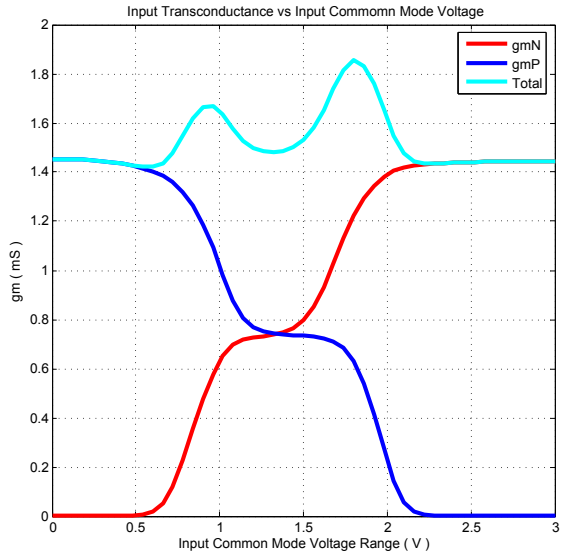

Fig. 3: Input Stage's gm variation over the entire input V_{CM} range.

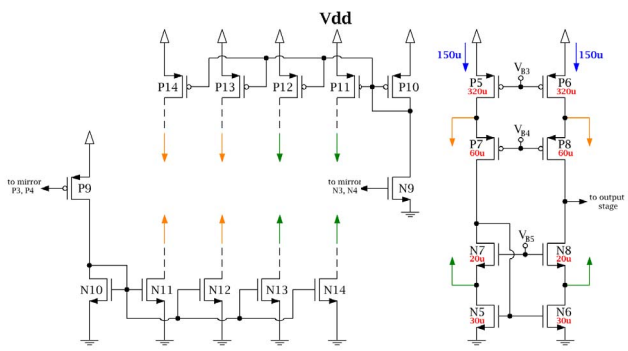

Fig. 4: Current Summation Stage.

Typically, for simple designs it is important that the source currents of P5 and P6, are designed to be larger than the total bias current of the NMOS pair I_n so that even under slew rate limiting conditions, the current summation transistors have enough remaining current to function properly. As mentioned in [3], typical ratios for $I_{P5,P6}$ are between 1.1 and 1.5 times I_n. In this work however, we did not need to increase

the current summation stage's current to such an extent. The reason is that attention was paid to lower the size of transistors and hence parasitics, providing at the same time ample current to other key spots that were prone to limit the transient behaviour.

Although in simple, non Rail to Rail, folded cascode topologies this current summation stage works well, in our case it presents a major disadvantage: its proper operation depends on V_{CM} because its bias currents and dc operating points depend on the differential pair's bias currents, which change with respect to V_{CM} as we explained in A. In order to solve this issue, we include a second current compensation network, that senses changes in V_{CM} and then compensates accordingly for the resulting changes in the input pair's bias currents. This network is depicted as the left block of Fig. 4. It is essentially an extension of the constant gm architecture and consists of the following transistor groups:

- (P9,N10,N11,N12,N13,N14) which operate when V_{CM} drops low
- (N9,P10,P11,P12,P13,P14) which operate when V_{CM} rises high

Basically, each one of the transistors N11 and N12 demands $I_{nom}/2$ from P5, P6 whenever the NMOS pair turns off, while N13 and N14 reduce the output bias currents of P1, P2 to $I_{nom}/2$. In the same manner, P11 and P12 deliver $I_{nom}/2$ to N5, N6 whenever the PMOS pair turns off, while P13 and P14 reduce the output bias currents of N1, N2 to $I_{nom}/2$.

This way, the bias currents flowing through the summation stage transistors remain almost constant and equal to their nominal values of $150\,\mu A$ for (P5,P6,N5,N6) and $150\,\mu A - 100\,\mu A = 50\,\mu A$ for the cascode transistors P7, P8 and N7, N8 for the whole range of Rail-to-Rail operation.

C. Class-A Output Stage

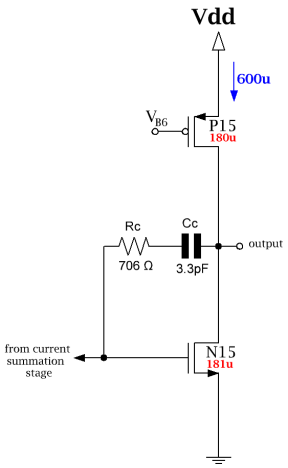

Fig. 5: Class-A, Single-Ended Common Source Stage.

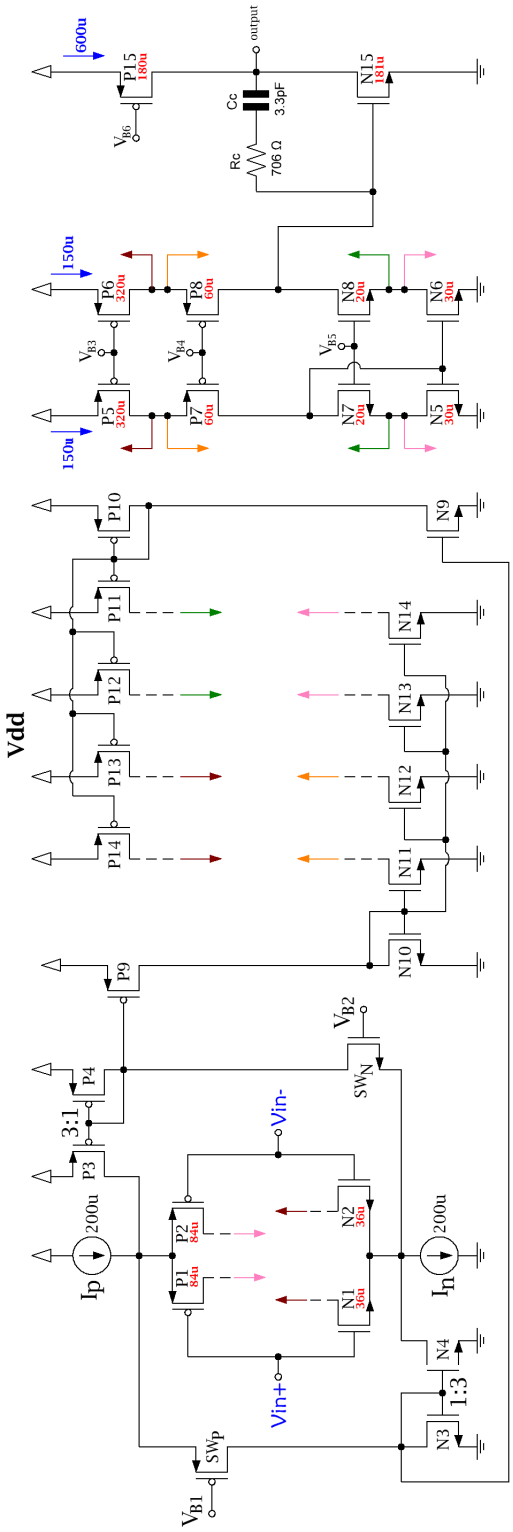

Fig. 6: The complete schematic of our Rail-to-Rail opamp.

Our output stage of choice is shown in Fig. 5. It is a simple

TABLE I: Simulation Results

Parameter	$V_{CM} = 0$V	$V_{CM} = 1.5$V	$V_{CM} = 3.0$V
Small-Signal DC Gain	89.28 dB	96.76 dB	82.61 dB
Unity-Gain Frequency	48.86 MHz	59.51 MHz	39.36 MHz
Phase Margin	91.47°	83.66°	85.14°
Gain Margin	13.72 dB	10.53 dB	13.59 dB
Settling Time (0.1% Error)	-	31.73 ns	-
Current Consumption	2.511 mA	1.471 mA	2.443 mA
Input-Referred Noise	$<9.65\,\mathrm{nV}/\sqrt{Hz}$	$<8.67\,\mathrm{nV}/\sqrt{Hz}$	$<9.42\,\mathrm{nV}/\sqrt{Hz}$
CMRR	>90 dB	>90 dB	>90 dB
PSRR	>90 dB	>90 dB	>90 dB

class-A, single-ended stage, consisting of a common-source wired transistor N15, and its current source P15.

The output stage current is biased at $600\,\mu\mathrm{A}$, to enhance transient response. After experimentation, we realised that providing more current at the output and input had by all means better results than giving more at the current summation stage.

As far as compensation is concerned, we used R-C Miller compensation directly at the common source wired transistor. The chosen values of $R_c = 706\,\Omega$ and $C_c = 3.3\,\mathrm{pF}$ not only provides excellent phase and gain margins, but also saves physical space compared to choosing higher values of capacitance.

III. Simulation Results

The complete schematic of our design is depicted in Fig. 6. Different colors tied at same nodes are used for better clarification of each stage's working principle.Table I shows the results of our simulated parameters.

The large-signal step response and settling time measurement were acquired applying an $1\,\mathrm{V}$ amplitude step waveform, the opamp being in unity-feedback configuration with a $1.5\,\mathrm{V}$ input common-mode voltage and a $1\,\mathrm{pF}\|20\,\mathrm{k}\Omega$ load. Rise time was measured to be $31.73\,\mathrm{ns}$, while fall time was less, at $27.35\,\mathrm{ns}$.

The design also offers a quite generous DC gain, very low noise and a wide unity gain bandwidth. Special mention should be given to the stability margins achieved: GM is always more than about $10\,\mathrm{dB}$, while PM is even better, always being more than $83°$ - margins that establish a very robust design.

It should be mentioned here, that careful choice of bias currents at crucial points enabled the opamp to achieve its transient response. Lower biasing provided almost the same bode plots and stability margins, but failed to achieve the required settling time. One could say that the recipe was present, but the ingredients were missing.

Last but not least, we observe a fairly constant behaviour across the whole input voltage common range. This was achieved using all the aforementioned extra current mirror networks. Of course, the price paid was extra current consumption - a fact to be expected.

IV. Conclusion

The designed Rail-to-Rail opamp performed well over all specifications. This work can be regarded as a fully functional, rigidly stable design, that could be used as a key building block in many IC designs and applications. Future implementations of the presented architecture employing newer CMOS or BiCMOS technologies may result in improved performance, particularly as far as power consumption is concerned [6], [9]. Last but not least, certain stages could be re-designed to enable a specialized usage of the opamp, since the basic performance is already very promising.

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