32-QAM All-Digital RF Signal Generator Based on a Homodyne Sigma-Delta Modulation Scheme

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***Abstract*—An all-digital sigma-delta modulator (SDM) based RF synthesizer is presented. A multiplier-less architecture for the implementation of the band-pass SDM loop filter is proposed. Furthermore, this architecture enables the adjustment of the loop filter central frequency by exploiting homodyne up- and down-conversion. The RF synthesizer is comprised of a direct digital synthesizer (DDS) and the proposed multiplier-less single-bit band-pass SDM. Due to the simplicity of the synthesizer building blocks very high generated frequencies are possible. Modualtion is easily incorporated and as a test case its performance in a 32-QAM modulation scheme is presented.**

***Index Terms*—Sigma-delta, noise shaping, single-bit quantization, multiplier-less, all-digital, homodyne, synthesizer, RF, QAM**

I. Introduction

Sigma-delta modulators (SDMs) have been proposed for all-digital frequency synthesis in a limited bandwidth dependent on the SDM oversampling ratio (OSR). Analog blocks suffer from thermal noise, dependence on the power source quality, non-linearities due to component mismatches, lack of design tool automation and increased concept-to-market time when a circuit is migrated to another IC technology. On the contrary, digital circuits do not exhibit these problems. Therefore, all-digital frequency synthesizers offer significant advantages over analog or mixed-signal designs. Single-bit representation of the output signal is crucial for the omission of mixed-signal components such as DACs.

A typical all-digital SDM-based frequency synthesizer is shown in Fig. 1. The adder and the register work as a phase accumulator generating $kw \mod 2^n$ on the k-th rising clock edge, where w is the frequency control word (FCW) [1]. Its output is fed to the cosine look-up table (LUT) whose output is $\cos(2\pi kw/2^n)$ where n is the bit-width of the accumulator's register. The LUT output is passed through a single-bit band-pass sigma-delta modulator which shapes the quantization noise outside the band of interest. Random dithering may be added to remove any frequency spurs.

II. Single-bit SDM with Quadrature Homodyne Filter

The single-bit SDM is depicted in Fig. 2. The loop filter $F(z)$ determines the OSR and the noise shaping characteristics

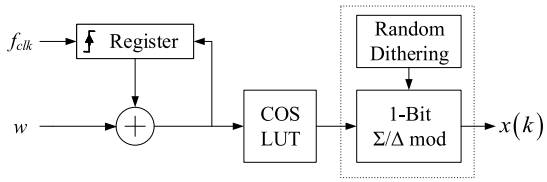

Fig. 1. Pulse DDS (PDDS) with sigma-delta noise shaping.

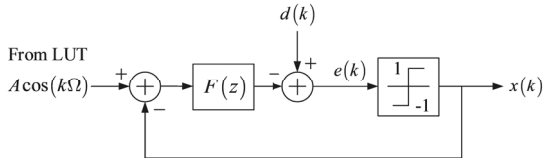

Fig. 2. The single-bit band-pass SDM.

of the SDM. A typical digital filter requires different coefficients if a change in its passband is needed. This is the case if different bands of frequencies are to be generated. Therefore, any optimizations in a programmable filter implementation would be difficult. The quadrature homodyne filter (QHF) architecture [2] can address this issue.

A. The Quadrature Homodyne Filter Architecture

The QHF architecture, shown in Fig. 3, implements the band-pass filter $F(z)$ using two fixed identical low-pass filters $H(z)$ and quadrature homodyne down- and up-conversion to achieve band-pass frequency response centered at the carrier angular frequency Ω. The QHF architecture in Fig. 3 requires

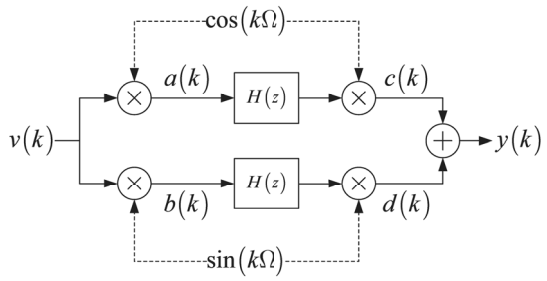

Fig. 3. The quadrature homodyne filter architecture.

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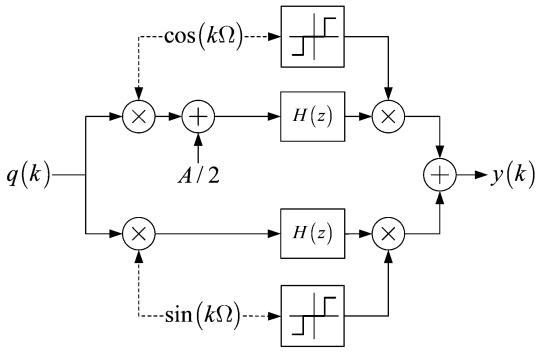

Fig. 4. QHF multiplier-free architecture; $q(k) = -x(k)$.

four multiplications, an addition and two identical low-pass filters. It is shown next that the multiplications can be eliminated.

B. The Multiplier-less Quadrature Homodyne Filter

The low-pass filters $H(z)$ of the QHF architecture can be chosen to have coefficients which are powers of 2 or sums of two or three powers of 2. This way the required multiplications are reduced to additions and shift operations.

The other four multiplications can be eliminated by exploiting first-order approximation of the QHF input and 3-level quantization of the sine and cosine signals in Fig. 3. The former eliminates the left hand side multipliers while the latter eliminates the right hand side ones. The final multiplier-less QHF architecture is shown in Fig. 4.

III. The Multiplier-less RF Synthesizer

Using the multiplier-less QHF architecture for the implementation of the SDM loop filter, the PDDS with sigma-delta noise shaping in Fig. 1 can be used for the generation of a wide range of radio frequencies by adjusting the central frequency of the QHF. Amplitude modulation can be added by varying A in Fig. 4, whereas frequency or phase modulation can be included by adding an appropriate value to w or just before the cosine LUT (Fig. 1).

A. 32-QAM Modulation Simulation Results

The aforementioned RF synthesizer architecture has been simulated in Matlab for the generation of a 32-QAM modulated RF signal. The 32-QAM modulation-demodulation simulation setup is shown in Fig. 5. The square-root raised cosine filters are used for the reduction of inter-symbol interference (ISI).

In our test-case an OSR of 1024 is used. The square-root, raised cosine filters are designed to span 10 symbols with roll-off factor $\beta = 0.25$. Using the aforementioned system parameters, the near-in spectrum in Fig. 6 was obtained for 10,000 symbols. Notice that the bandwidth of the RF synthesizer (noise suppressed frequency range), determined by the OSR, is selected according to the signal bandwidth to minimize the required OSR while retaining stability. Channel

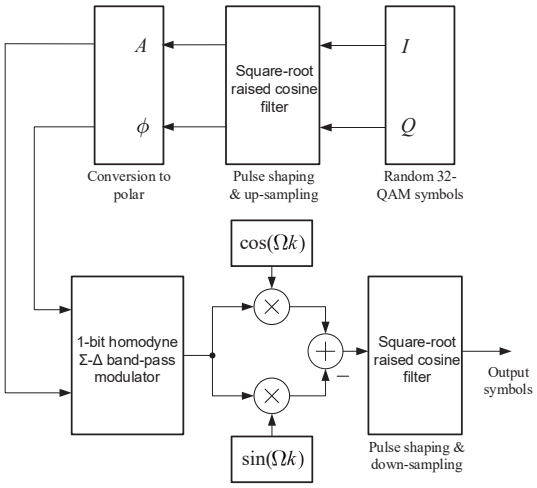

Fig. 5. 32-QAM modulation-demodulation simulation setup.

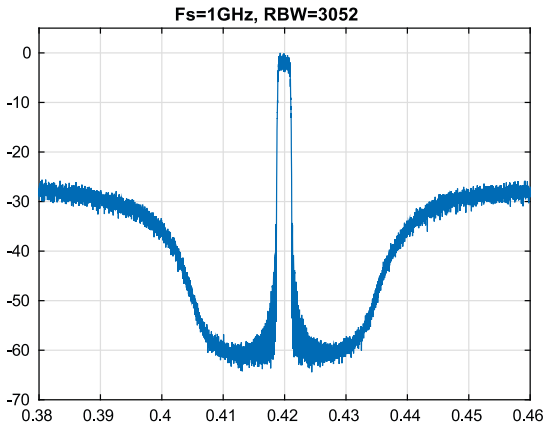

Fig. 6. Spectrum with 32-QAM modulation and OSR = 1024. Y-axis in dB, X-axis: Discrete-Time Frequency

selection is accomplished by adjusting the central frequency of the SDM.

After demodulation, the constellation diagram of the demodulated signal was attained, resulting in an RMS EVM of 0.956%. Assuming a clock frequency of 1 GHz, the proposed all-digital transmitter is capable of achieving a symbol rate of 976.56 Ksymbols/s. For 32-QAM modulation this is translated to a data rate of 4.882 Mbits/s.

References

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[2] P. P. Sotiriadis, "Single-bit all digital frequency synthesis using homodyne sigma-delta modulation," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, to appear.