Frequency Synthesis Using Low-Pass Single-Bit Multi-Step Look-Ahead Sigma-Delta Modulators in Quadrature Upconversion Scheme

Charis Basetas, Paul Peter Sotiriadis
Department of Electrical and Computer Engineering
National Technical University of Athens
Athens, Greece
E-mail: chbasetas@gmail.com, pps@ieee.org

Nikos Temenos
Department of Informatics and Telecommunications
National and Kapodistrian University of Athens
Athens, Greece
E-mail: ntemenos@gmail.com

***Abstract*—All-digital frequency synthesis using two low-pass single-bit Multi-Step Look-Ahead sigma-delta modultors (MSLA SDMs) is presented. MSLA SDMs provide better noise shaping characteristics, i.e. SNDR and bandwidth, than conventional SDMs at the cost of higher hardware complexity. The balance between complexity and performance is adjusted by the number of look-ahead steps, which is an additional design parameter. The frequency synthesizer system is comprised of two identical low-pass single-bit MSLA SDMs. Their inputs are orthogonal sinusoidals generated by a direct digital synthesizer (DDS). The frequency range of the synthesizer using a single clock signal is determined by the oversampling ratio (OSR) of the SDMs. A lower OSR results in a wider frequency range, but reduces the output SNDR. System-level simulation results of the frequency synthesizer are presented, showcasing the performance advantage of using MSLA SDMs instead of conventional ones.**

***Index Terms*—Sigma-delta, noise shaping, single-bit quantization, modulator, all-digital, quadrature, low-pass, synthesizer, look-ahead**

I. Introduction

Accurate and finely controled frequency synthesis is crucial for many modern applications. Digital frequency synthesizers have many advantages over mixed-signal and analog ones. They exhibit excellent digital accuracy, high resolution frequency control and fast frequency hopping. Furthermore, they inherit all the advantages of digital circuits, such as immunity to process, voltage and temperature variations, portability, scalability, reconfigurability, faster design cycle and smaller chip area.

Direct digital synthesizers (DDS) [1] are digital circuits capable of generating a large number of frequencies using a single reference clock. However, they require a DAC for their operation, which is a mixed-signal component. All-digital alternatives such as the PDDS (Pulse DDS) have been proposed, but they introduce frequency spurs or a high noise floor [2]. Another approach is the use of a digital single-bit band-pass sigma-delta modulator (SDM) to shape the quantization noise out of the desired frequency band [3]. This requires that the operating frequency of the SDM is at least twice that of the maximum synthesizable frequency. Thus, the SDM speed is the limiting factor.

Arbitrary maximum synthesizable frequencies, limited only by the speed of a digital miltiplexer, can be achieved using two low-pass SDMs in quadrature configuration. The two low-pass SDMs can be clocked at a lower frequency, while their outputs are upconverted and interleaved by three digital multiplexers. A fourth multiplexer running at a much higher frequency can be used to generate an even higher output frequency. This work replaces conventional SDMs in the aforementioned configuration with single-bit Multi-Step Look-Ahead (MSLA) SDMs [4]. They are digital SDMs that improve upon the noise shaping characteristics and stability of conventional SDMs by considering current and future quantization errors for the determination of their output. Conventional SDMs only take into account the instantaneous quantization error. This enables the use of more aggressive NTFs (noise transfer functions) leading to increased bandwidth, i.e. lower oversampling ratio (OSR), while retaining higher signal-to-noise-and-distortion ratio (SNDR) than conventional single-bit SDMs.

In the next section the proposed architecture is presented. In section III system-level simultion results are shown, demonstrating the performance advantage of using MSLA SDMs over conventional ones. Section IV concludes the discussion.

II. Frequency Synthesis Using Low-Pass MSLA SDMs in Quadrature Upconversion Scheme

In this section we first describe the proposed frequency synthesizer arcitecture, followed by a brief discussion about MSLA SDMs.

A. The Proposed Frequency Synthesizer Architecture

The proposed set-up is shown Fig. 1. Two DDSs are used to generate two orthogonal sinusoidals with frequency

$$f_{BB} = \left(w/2^N\right) f_{clk}.$$

To avoid an image in the final signal spectrum, a $\pi/2$ phase difference is required between the I and Q components. This is the reason why the initial value of the sine look-up table (LUT) phase accumulator is $w_0 = 0.5w$, whereas the initial value of the cosine LUT phase accumulator is $w_0 = 0$. The

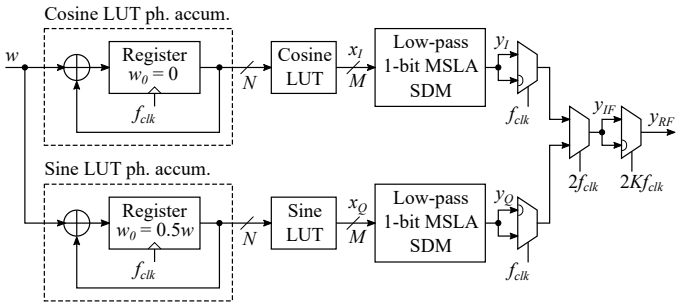

Fig. 1. All-digital frequency synthesizer using two 1-bit low-pass MSLA SDMs in quadrature configuration.

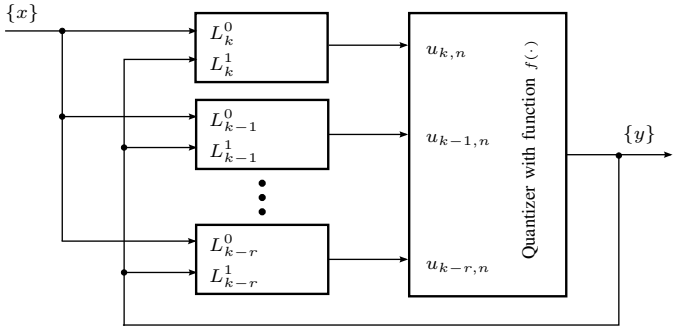

Fig. 2. The MSLA SDM system diagram.

two sinusoidal I and Q components x_I and x_Q are fed to two identical single-bit low-pass MSLA SDMs. They convert their multi-bit inputs to two single-bit bitstreams. These are then passed through a number of multiplexers that upconvert and interleave them. The sampling frequency of each multiplexer in Fig. 1 is shown under the multiplexer. The multiplexers processing the MSLA SDM output signals toggle between their inputs (normal and inverted) at a rate f_{clk}, whereas the next multiplexer toggles between the output of the I path multiplexer and the output of the Q path multiplexer at a rate $2f_{clk}$. This process results in an intermediate single-bit signal y_{IF} (Fig. 1) with frequency

$$f_{IF} = (f_{clk}/2) + f_{BB}. \tag{1}$$

This might actually be the frequency to be generated, but in the case that a higher frequency is desired another multiplexer running at frequency $2Kf_{clk}$ can be used. The resulting signal is single-bit and has frequencies given by

$$f_{RF,i} = mf_{clk} \mp (f_{IF}/2)\,,\ 0 \le m \le K,\ m \in \mathbb{N}^+ \tag{2}$$

as long as $0 \le f_{RF,i} < Kf_{clk}$.

Since the generated signal is single-bit, no DAC is required and therefore the synthesizer is all-digital. However, an analog bandpass filter is required in some applications to remove the out-of-band quantization noise generated by the MSLA SDMs.

The bandwidth of the frequency synthesizer is determined by the MSLA SDM OSR. The frequency range of the generated intermediate signal, i.e. the bandwidth of the frequency synthesizer for the output signal y_{IF}, for a given OSR is

$$\mathrm{BW}_{IF} = \left[\frac{f_{clk}}{2} - \frac{f_{clk}}{2\cdot\mathrm{OSR}}, \frac{f_{clk}}{2} + \frac{f_{clk}}{2\cdot\mathrm{OSR}}\right]. \tag{3}$$

The bandwidth of the y_{RF} signal is split into many frequency bands. Each frequency given by (2) lies inside such a frequency band. The frequency bands of the signal y_{RF} are given by

$$\mathrm{BW}_{RF} = \left[mf_{clk} \mp \frac{f_{clk}}{4} - \frac{f_{clk}}{2\cdot\mathrm{OSR}}, mf_{clk} \mp \frac{f_{clk}}{4} + \frac{f_{clk}}{2\cdot\mathrm{OSR}}\right] \tag{4}$$

for the values of m valid in (2).

B. The Role of the MSLA SDM Design Choices

The MSLA SDM system diagram is shown in Fig. 2. It is comprised of $r+1$ two-input digital IIR filters (L_j^0, L_j^1), $k-r \le j \le k$, and an $(r+1)$-input quantizer. The number of look-ahead steps k adjusts the trade-off between hardware complexity and performance. Typical values allowing for improved performance with moderate complexity increase are $r = k$, $k \in [3, 8]$. For a more detailed presentation the reader is referred to [4].

The in-band noise and the SNDR are determined by the MSLA SDM NTF order, the OSR and the NTF out-of-band gain $||NTF||_\infty$. A higher OSR results in higher SNDR at the cost of a smaller in-band frequency range. The stability limits of the sigma-delta loop manifest themselves as a type of gain-bandwidth product. More specifically, in a conventional single-bit SDM the NTF out-of-band-gain (gain) and 1/OSR (bandwidth) product cannot exceed a certain value for the loop to remain stable. In MSLA SDMs, as the number of look-ahead steps k increases, so does the $||NTF||_\infty$-1/OSR product. Thus, for a certain OSR value, more look-ahead steps k result in higher NTF out-of-band gain and in-band SNDR. However, in order to achieve the in-band noise floor dictated by the MSLA SDM NTF, a clock signal with low enough phase noise should be used. Therefore, the clock signal spectral purity is also of great importance.

C. The Noise Frequency Response of the Synthesizer

The NTF at the position of the y_{IF} signal in Fig. 1 is easily derived from that of the low-pass MSLA SDMs using the well-known transformation $z \to -z^2$ for the NTF of bandpass SDMs [5], i.e.

$$NTF_{BP}(z) = NTF_{LP}(z)|_{z=-z^2}. \tag{5}$$

The NTF at the position of the y_{RF} signal is derived from NTF_{BP} by observing that the final multiplexer essentially multiplies a possibly upsampled version of y_{IF} using zero-order hold (ZOH) with a cosine wave having frequency $\omega = \pi$ or $f = Kf_{clk}$. The upsampled by $2(K-1)$ version of

y_{IF}, converted to continuous time representation and assuming $y_{IF}[n] = 0,\ n < 0$, is

$$y_{ZOH,IF}(t) = \sum_{n=0}^{\infty} y_{IF}[n] \cdot \mathrm{rect}\left(\frac{t - \frac{1}{2}nT_{clk}}{\frac{1}{2}T_{clk}} - \frac{1}{2}\right) \quad (6)$$

where $T_{clk} = 1/f_{clk}$. So, the y_{RF} signal in continuous time representation is

$$y_{RF}(t) = y_{ZOH,IF}(t) \cdot \cos(2\pi K f_{clk} t). \quad (7)$$

Taking the Fourier transforms of (6) we can write

$$Y_{ZOH,IF}(f) = H_{ZOH}(f) \cdot Y_{IF}(f) \quad (8)$$

where

$$H_{ZOH}(f) = e^{-j\pi f \frac{T_{clk}}{2}} \frac{\sin(\pi f \frac{T_{clk}}{2})}{\pi f \frac{T_{clk}}{2}}. \quad (9)$$

The Fourier transform of (7) is the convolution of the Fourier transforms of $y_{RF}(t)$ and $\cos(2\pi K f_{clk} t)$, i.e.

$$Y_{RF}(f) = Y_{ZOH,IF}(f) * \frac{\delta(f - Kf_{clk}) + \delta(f + Kf_{clk})}{2}. \quad (10)$$

Combining (8), (9) and (10) we get the following relation

$$Y_{RF}(f) = \left[e^{-j\pi f \frac{T_{clk}}{2}} \frac{\sin(\pi f \frac{T_{clk}}{2})}{\pi f \frac{T_{clk}}{2}} \cdot Y_{IF}(f)\right] * \frac{\delta(f - Kf_{clk}) + \delta(f + Kf_{clk})}{2}. \quad (11)$$

Therefore, NTF_{BP} is transformed by first shaping it by the transfer function of the ZOH including upsampling and then convolving it with the spectrum of a cosine signal with frequency $f = Kf_{clk}$ which is composed of two delta functions at frequencies $f - Kf_{clk}$ and $f + Kf_{clk}$. To avoid confusion, in the remainder of the paper the term NTF applies to the NTF of the low-pass MSLA SDMs.

III. Simulation Results

The performance of the proposed architecture is highlighted in Fig. 3 where the power spectrum of the y_{IF} signal is shown. The I and Q inputs are $x_I = 0.4\cos(2\pi \cdot 0.01n)$ and $x_Q = 0.4\sin(2\pi \cdot 0.01(n + 0.5))$ respectively. The MSLA SDMs are configured with 7-th order low-pass filters, OSR $= 32$ and $r = k = 6$. Assuming the clock frequency is $f_{clk} = 250$ MHz, and thus the sampling frequency for signal y_{IF} is $f_s = 2f_{clk} = 500$ MHz, the resolution bandwidth is RBW $= 333.33$ Hz, resulting in a spurious-free dynamic range (SFDR) of DR $= -137\,\mathrm{dB} - 10\log_{10}(\mathrm{RBW}) = -162$ dBc/Hz. The SNDR is calculated at 104.5 dB. So high SNDR with that OSR value is not achievable with conventional single-bit SDMs. This is due to the more aggressive NTFs, i.e. NTFs with higher out-of-band gain, possible with single-bit MSLA SDMs in comparison with conventional single-bit SDMs.

The power spectra of the two low-pass MSLA SDM outputs, y_I and y_Q, are identical. The one for output x_I is shown in Fig. 4. Note that the sampling frequency for signal y_I is half of that used for signal y_{IF}, namely $f_s = f_{clk} = 250$ MHz. This is because for the interleaving process, both signals y_I and y_Q are used alternately as seen in Fig. 1.

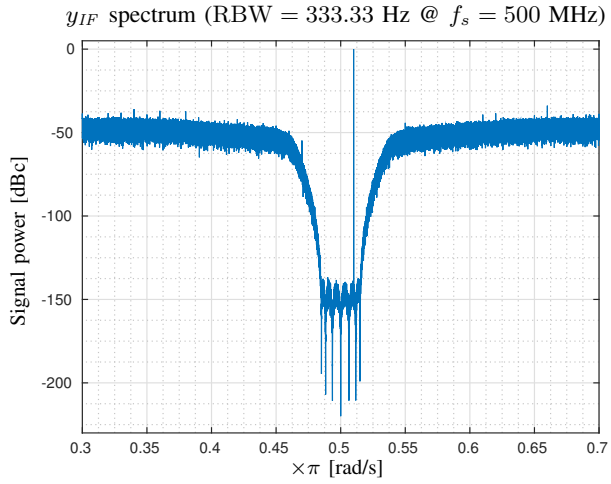

Fig. 3. Spectrum of the frequency synthesizer output y_{IF}.

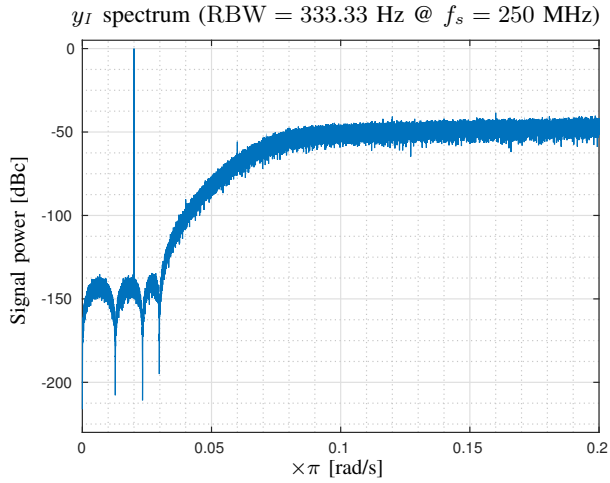

Fig. 4. Spectrum of the MSLA SDM output y_I.

In the case that a higher output frequency than y_{IF} is needed, one can use the output y_{RF} provided by the final multiplexer in Fig. 1. Using a value of $K = 2$, i.e. having a sampling frequency $f_s = 4f_{clk} = 1$ GHz, results in the power spectrum shown in Fig. 5. The generated frequencies are given by (2). A zoomed-in version of this plot for $m = 2$ and the minus sign in (2) is depicted in Fig. 6. In our test case we have $f_{BB} = 0.01f_{clk} = 2.5$ MHz. From (1), the intermediate frequency is $f_{IF} = 125 + 2.5$ MHz $= 127.5$ MHz. Thus, the generated frequencies for $K = 2$ are

$$f_{RF,1} = 0 \cdot 250 + 63.75 \text{ MHz} = 63.75 \text{ MHz}$$
$$f_{RF,2} = 1 \cdot 250 - 63.75 \text{ MHz} = 186.25 \text{ MHz}$$
$$f_{RF,3} = 1 \cdot 250 + 63.75 \text{ MHz} = 313.75 \text{ MHz}$$
$$f_{RF,4} = 2 \cdot 250 - 63.75 \text{ MHz} = 436.25 \text{ MHz}.$$

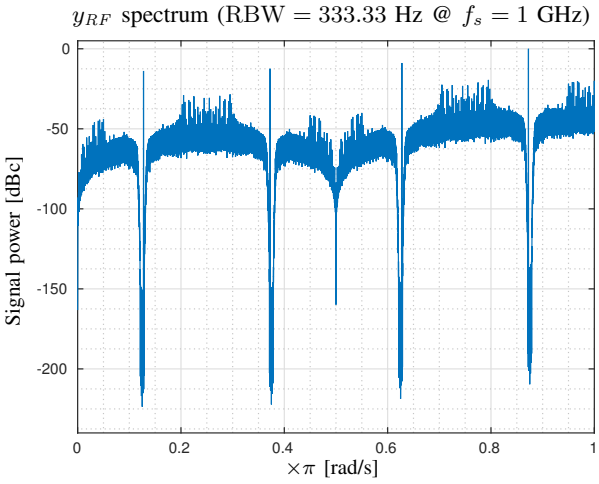

Fig. 5. Spectrum of the the frequency synthesizer output y_{RF} for $K = 2$.

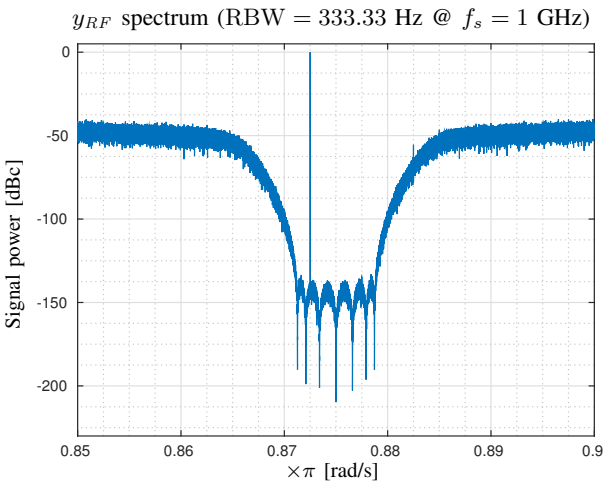

Fig. 6. Zoomed-in spectrum of the the frequency synthesizer output y_{RF}.

Since the OSR is 32, the passband of signal y_I in Fig. 4 is from DC to $f_{clk}/(2 \cdot 32) = 3.90625$ MHz. The bandwidth of the quadrature upconverted signal y_{IF} as given by (3) is 7.8125 MHz, twice that of the y_I signal, with generated frequencies ranging from 121.09375 MHz to 128.90625 MHz. For the frequency range of the zoomed-in y_{RF} signal spectrum in Fig. 6, we refer to (4) using $m = 2$ and the minus sign. This gives a frequency band ranging from 433.59375 MHz to 441.40625 MHz. The resulting bandwidth is 7.8125 MHz, the same as that of the y_{IF} signal.

In Table I the SNDR and SFDR of various MSLA SDM based frequency synthesizers are displayed for the y_{IF} output signal. The I and Q inputs are the same as those of the previous paragraph. For $k = 0$ the MSLA SDM reduces to a conventional SDM. The NTFs are designed using the highest out-of-band gain possible for the specific values of the OSR and the number of look-ahead steps k. For the determination of stability $3 \cdot 10^6$ output samples for each MSLA SDM are considered. The performance improvements over conventional SDMs are significant even for small values of k. The SFDR is calculated assuming sampling rate $f_s = 500$ MHz.

TABLE I
SNDR AND SFDR COMPARISON

OSR	r, k [a]	$\|\|NTF\|\|_\infty$ [b]	**SNDR [dB]**	**SFDR** [c] **[dBc/Hz]**
32	0	1.62	98.9	−142
32	3	1.68	102.0	−150
32	5	1.71	104.9	−161
64	0	1.57	140.6	−194
64	3	1.60	142.0	−182
64	5	1.65	147.4	−196
128	0	1.57	188.6	−233
128	3	1.61	193.9	−234
128	5	1.64	198.4	−242

[a] $r = k = 0$ corresponds to a conventional single-bit SDM.
[b] The NTF out-of-band gain.
[c] Assuming sampling rate $f_s = 500$ MHz.

IV. CONCLUSION

Frequency synthesis using two low-pass single-bit MSLA SDMs in quadrature upconversion scheme was presented. It was shown that the performance advantages of using single-bit MSLA SDMs over conventional single-bit SDMs are significant. The proposed frequency synthesizer architecture is purely digital apart from a bandpass analog filter required for the attenuation of the out-of-band quantization noise in some applications. The highest possible generated frequency is only limited by the final multiplexer operating frequency. This allows the proposed frequency synthesizer to be used for synthesizing frequencies well in the GHz range.

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