Wide-Band Frequency Synthesis Using Hardware-Efficient Band-Pass Single-Bit Multi-Step Look-Ahead Sigma-Delta Modulators

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***Abstract*—Band-pass sigma-delta modulators (SDMs) can be used for all-digital frequency synthesis with low noise in the SDM passband. To avoid mixed-signal components such as DACs, a single-bit output is required. The noise shaping characteristics of single-bit sigma-delta modulators are limited by stability requirements. Look-ahead SDMs have been proposed to increase the bandwidth and signal-to-noise-and-distortion ratio (SNDR) of conventional single-bit ones. The cost is increased hardware complexity, but Multi-Step Look-Ahead sigma-delta modulators (MSLA SDMs) can significantly reduce the required hardware complexity, while retaining the advantages of look-ahead SDMs. This work demonstrates the hardware requirements of MSLA SDMs and proposes an all-digital frequency synthesizer architecture based on band-pass MSLA SDMs. The performance of the poposed synthesizer architecture is investigated for various configurations. Finally, the advantages of using MSLA SDMs instead of conventional single-bit ones in terms of bandwidth and SNDR are quantified.**

***Index Terms*—Sigma-delta, noise shaping, single-bit quantization, modulator, all-digital, band-pass, synthesizer, look-ahead**

I. Introduction

All-digital frequency synthesis has been proposed [1] to avoid the use of analog or mixed-signal components. Some of the advantages of purely digital circuits are immunity to thermal noise, process and power supply variations, and fast design cycle due to the availability of many design automation tools. All-digital frequency synthesizers also facilitate the generation of a wide range of frequencies using a single reference clock. For true all-digital designs, a single-bit output should be used, so that no multi-bit digital-to-analog converter (DAC) is required. Furthermore, single-bit quantization allows for inherently linear output since there are only two output signal levels. Therefore, there are only gain and offset errors which do not impact the output spectrum and can be easily corrected using digital calibration techniques. However, traditional single-bit output synthesizers such as the PDDS (Pulse Direct Digital Synthesizer) suffer from frequency spurs and/or a high noise floor [2]. Digital single-bit sigma-delta modulators (SDMs) [3] can be used to shape the quantization noise out of the desired frequency band.

Single-bit SDMs have limited noise shaping capabilities due to stability restrictions. Multi-bit SDMs exhibit increased stability, but they require a DAC for the conversion of their digital multi-bit output to analog. Look-ahead SDMs [4] can offer increased bandwidth, signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) than conventional single-bit SDMs. The cost is increased hardware complexity which makes their implementation for real-time applications especially difficult. Multi-Step Look-Ahead sigma-delta modulators (MSLA SDMs) were proposed in [5] to enable hardware-efficient implementation of look-ahead SDMs.

In the next section the MSLA SDM system is briefly described. In section III its hardware complexity is investigated and shown to be low enough for real-time frequency synthesis. Section IV provides simulation results showcasing the advantages of using MSLA SDMs for frequency synthesis over conventional ones. Finally, section V concludes the discussion.

II. MSLA SDM Basics

Conventional SDMs consider only the current quantization error for the determination of their output. Look-ahead SDMs [4] improve upon the stability and noise shaping characteristics of conventional SDMs by taking into account current and future quantization errors. This is accomplished by formulating an appropriate cost function including costs associated with future quantization errors. The decision on the next output is based on the minimization of the cost function. The term "look-ahead" does not imply that the input is predicted. Instead, the output is delayed by a number of samples equal to the look-ahead steps used. A higher number of look-ahead steps results in higher SNDR, SFDR and bandwidth, due to the possibility to use more aggressive noise transfer functions (NTFs), i.e. NTFs with higher out-of-band gain and thus lower in-band noise.

The MSLA SDM is a type of look-ahead SDM proposed in [5] that has lower hardware complexity compared to other types of look-ahead SDMs. Its system diagram is shown in Fig. 1. The modulator input sequence is denoted $\{x\}$, while

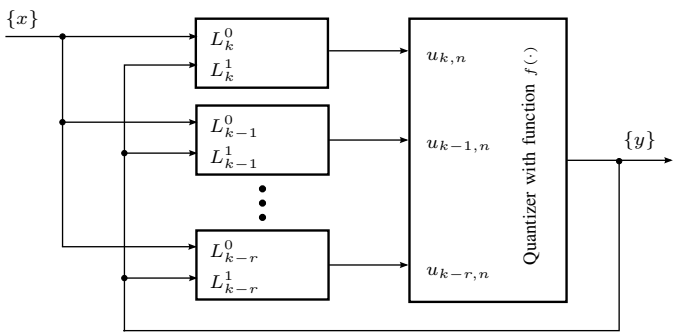

Fig. 1. The MSLA SDM system diagram.

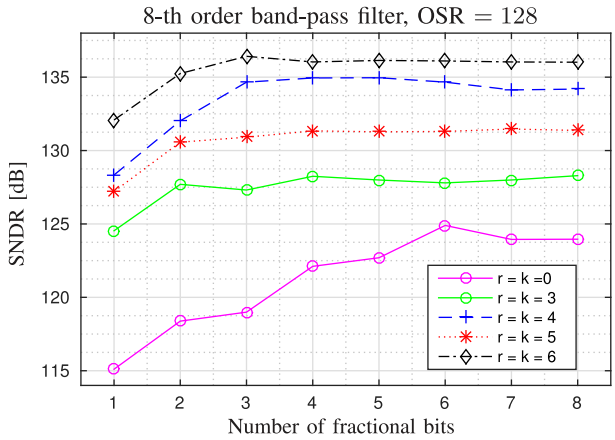

Fig. 2. SNDR vs. number of quantizer input fractional bits of the MSLA SDM frequency synthesizer with 8-th order band-pass filter and OSR = 128.

$\{y\}$ is the output sequence. The system is comprised of $r+1$ two-input digital IIR filters $\{L_j^0, L_j^1\}$ yielding $r+1$ outputs u_j, $k-r \leq j \leq k$, where k is the number of look-ahead steps and $r+1$ is the number of partial quantization error costs taken into account. The order of each IIR filter $\{L_j^0, L_j^1\}$ is $j+k$ whereas its coefficients are determined by the chosen NTF. The output of the modulator is given by a $(r+1)$-input quantizer described by a function $f(\mathbf{u}) : \Re^{r+1} \rightarrow \{\pm 1\}$, $\mathbf{u} = [u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n}]$, where n is the discrete time index. The quantizer input vector u is composed of the outputs of the IIR filters as shown in Fig. 1. The details of the quantizer function and the IIR filter coefficients are discussed thoroughly in [5].

III. MSLA SDM Hardware Implemention Investigation

As already mentioned the hardware implementation of a MSLA SDM is based on $r+1$ digital IIR filters and an $(r+1)$-input quantizer. Typical configurations are $r = k$ with $k \in [3, 8]$. For each two-input IIR filter of order m, $3m$ multiply and accumulate operations are needed for the calculation of its next output. The implementation of IIR filters has been thoroughly described in literature [6] and is not discussed here.

System-level simulations of MSLA SDMs have shown that 2-3 fractional bits and 4-5 integer bits for the representation of the quantizer input signals are enough to guarantee stable and accurate operation. This claim is justified in Fig. 2 where the SNDR of a MSLA SDM with an 8-th order band-pass filter and oversampling ratio OSR = 128 is shown for various fractional bits with look-ahead steps k as a parameter. The NTF has a central frequency $\omega_0 = 2\pi \cdot 0.38$ and the sinusoidal input signal has amplitude $A = 0.2$. Use of more than 3 fractional bits has no observable impact on the SNDR. Notice also how the SNDR improves as k is increased. This happens due to the higher out-of-band gain possible for the deisgn of the NTF while also retaining stability when using more look-ahead steps. For the simulation we have designed the NTFs using the Delta Sigma Toolbox in Matlab [7]. For each number of look-ahead steps k we have selected the highest possible NTF out-of-band gain.

For moderate values of k a look-up table (LUT) implementation of the MSLA SDM quantizer is viable. The quantizer function $f(\mathbf{u})$ is an odd function, meaning that the LUT size can be halved. As an example consider the case of $r = k = 3$ using 6 bits for each of the 4 quantizer inputs. This means that there are $(4 \cdot 6) = 24$ input bits. For each input combination the LUT stores 1 bit. Therefore, exploiting odd symmetry, a total of $2^{24-1} = 8.389$ Mbits of data need to be stored. Using logic optimization during synthesis this number is typically reduced by one to two orders of magnitude. This is well within the capabilities of modern digital circuits and FPGAs.

TABLE I
MSLA SDM Quantizer Synthesis Results

Primitive	Description	Used	Utilization
LUT6	6-input LUT	4244	2.58%
LUT5	5-input LUT	390	
LUT4	4-input LUT	310	
LUT3	3-input LUT	802	
LUT2	2-input LUT	462	
MUXF7	16:1 multiplexer	10	$< 0.01\%$

For the MSLA SDM configuration used in Fig. 2 with $r = k = 3$ and 6 bits (3 fractional bits, 2 integer bits and 1 sign bit) for each quantizer input, we have synthesized the resulting MSLA SDM quantizer for a Xilinx Kintex-7 FPGA KC705 Evaluation Kit target device. The final implementation report mentions the following primitives: 4244 6-input LUTs, 390 5-input LUTs, 310 4-input LUTs, 802 3-input LUTs, 462 2-input LUTs and 10 16:1 multiplexers. This is just 2.58% of the FPGA resources. These results are summarized in Table I.

IV. Band-pass MSLA SDM Based Frequency Synthesizer

A band-pass MSLA SDM can be used as part of an all-digital frequency synthesizer as shown in Fig. 3. A DDS (Direct Digital Synthesizer) [8] is used to generate a high-resolution digital sinusoidal signal which is then quantized to 1 bit by the MSLA SDM. The frequency control word w

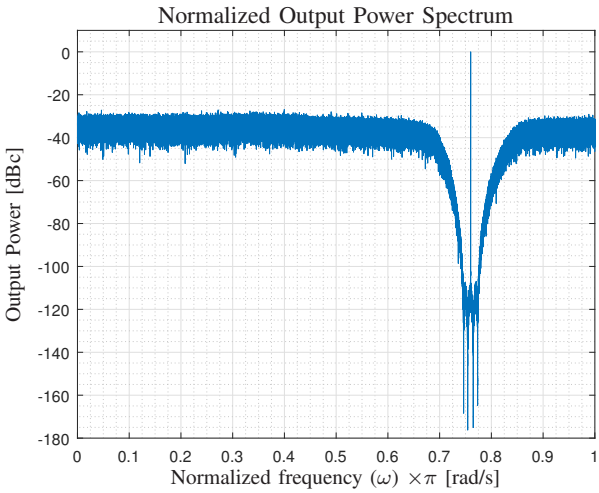

Fig. 5. Output power spectrum of the 8-th order band-pass MSLA SDM based synthesizer for OSR $= 32$ and $r = k = 4$.

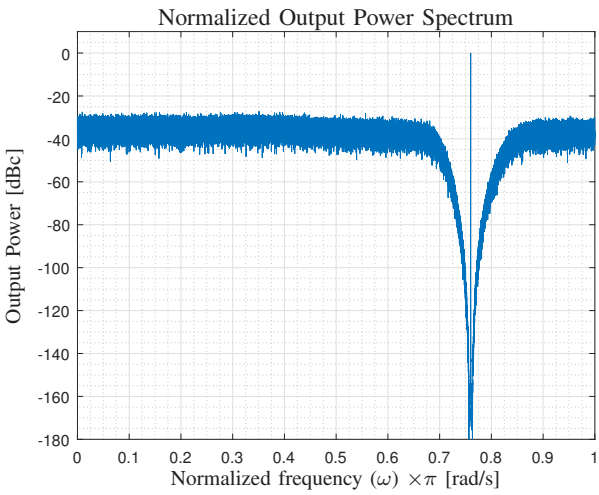

Fig. 6. Output power spectrum of the 8-th order band-pass MSLA SDM based synthesizer for OSR $= 128$ and $r = k = 4$.

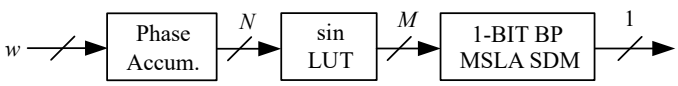

Fig. 3. All-digital frequency synthesizer using a 1-bit band-pass MSLA SDM.

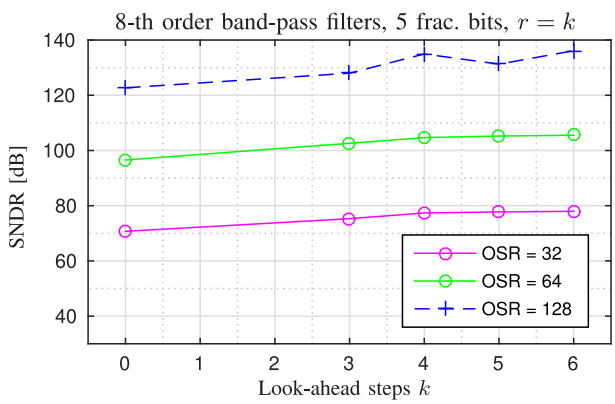

Fig. 4. SNDR vs. look-ahead steps k of the 8-th order band-pass MSLA SDM frequency synthesizer with OSR as a parameter.

selects the output frequency as $f_{\text{synth}} = (w/2^N) f_{\text{clk}}$, where N is the bit-width of the phase accumulator.

The in-band SNDR of 8-th order band-pass MSLA SDM frequency synthesizers for different values of OSR and look-ahead steps k is depicted in Fig. 4. For $k = 0$ the MSLA SDM reduces to a conventional SDM. The sinusoidal input has amplitude $A = 0.2$ while the central frequency of the NTFs is $\omega_0 = 2\pi \cdot 0.38$. The SNDR improvement over conventional SDMs ($k = 0$) is 10 dB or more for $k > 3$. The range of the synthesizable frequencies is determined by the NTF central frequency and the OSR and is given by

$$f_{\text{synth}} \in [f_0 - \frac{1}{4 \cdot \text{OSR}} f_{\text{clk}}, f_0 + \frac{1}{4 \cdot \text{OSR}} f_{\text{clk}}] \quad (1)$$

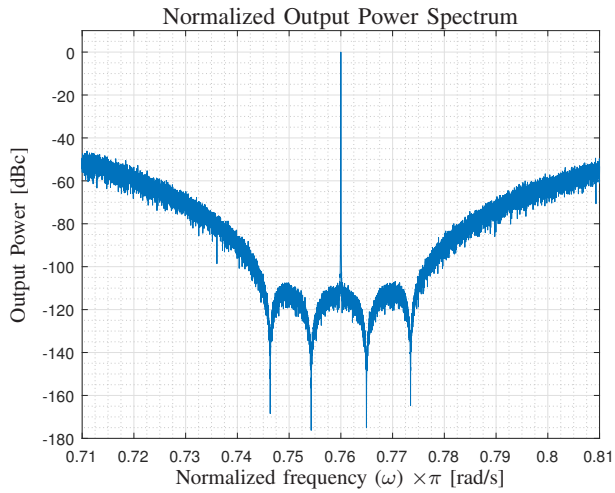

Fig. 7. Zoom-in of Fig. 5.

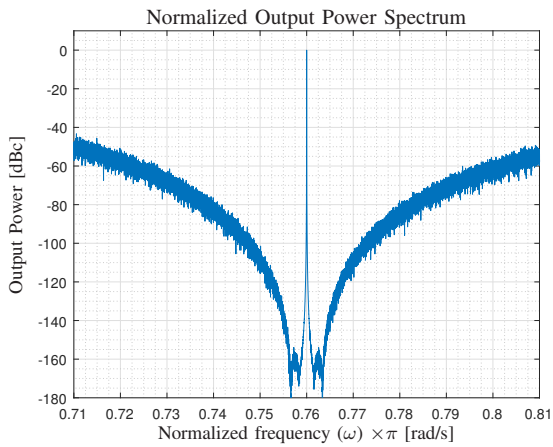

Fig. 8. Zoom-in of Fig. 6.

where f_0 is the central frequency of the NTF. Therefore, the synthesizable frequency bandwidth is

$$\mathrm{BW}_{\mathrm{synth}} = f_{\mathrm{clk}}/(2 \cdot \mathrm{OSR}). \tag{2}$$

Wideband frequency synthesis with low in-band noise is possible using a lower value for the OSR and exploiting the higher SNDR of MSLA SDMs over conventional single-bit ones.

For two of the aforementioned cases, namely for $r = k = 4$ and $\mathrm{OSR} = 32$ and $\mathrm{OSR} = 128$, the resulting output power spectra are plotted in Fig. 5 and Fig. 6 respectively. The output power is normalized with respect to the carrier. Zoomed-in versions of the previous plots are shown in Fig. 7 and 8 for the cases of $\mathrm{OSR} = 32$ and $\mathrm{OSR} = 128$ respectively. Notice that using a lower OSR results in increased synthesizable frequency bandwidth as indicated by (1) and (2), but the in-band noise gets higher. This is a typical design trade-off.

V. Conclusion

All-digital frequency synthesis using a DDS followed by a single-bit band-pass MSLA SDM was presented. The hardware requirements of the MSLA SDM $(r+1)$-input quantizer and IIR filters where analyzed and it was shown that the hardware overhead of using MSLA SDMs is not prohibitive for real-time operation. The performance advantage of MSLA SDMs over conventional single-bit ones in terms of SNDR was quantified for various cases via simulation and it was found to be significant.

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