Single-Bit All Digital Frequency Synthesis With Homodyne Sigma-Delta Modulation for Internet of Things Applications

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***Abstract*— All-digital frequency synthesis architectures with direct modulation capability, based on single-bit sigma-delta modulation loop with an innovative homodyne band-pass filter topology are presented focusing on wireless Internet of Things (IoT) applications. A hardware-efficient multiplier-free variation of the homodyne filter is also proposed. MATLAB simulation results for 16-QAM modulation demonstrate the capabilities of the proposed architectures.**

Keywords—Digital-to-frequency converter, direct digital synthesis, filter, frequency spurs, frequency synthesis, noise shaping, quantization, sigma-delta modulation, Internet of Things

I. Introduction

The world is continuously getting more interconnected. This is reflected in the Internet of Things (IoT) concept where an increasing number of autonomous devices are part of a large network. Thus, the need for low power and low cost wireless transceivers is becoming more essential than ever before.

There is a multitude of wireless protocols that have been adopted for IoT applications. Some of them target low power operation, typically achieving lower data rates, e.g. Bluetooth and Bluetooth Smart, ZigBee and NFC, while others target high-speed wireless communications, e.g. Wi-Fi and mobile communications protocols like 2G, 3G and 4G.

All-digital frequency synthesis can be used for transceiver development. The advantages of digital circuits range from immunity to noise and temperature, supply and process variations to short concept-to-market time due to the availability of powerful design and verification automation tools. Moreover, migration of digital circuits to newer, smaller scale integrated circuit (IC) technologies is faster and more straightforward than that of analog or mixed-signal ones. They are also more easily co-integrated with other digital circuitry, such as DSP engines.

Single-bit digital synthesizers such as the PDDS (pulse direct digital synthesizer) [1] inherit all the advantages of direct digital synthesizers (DDS) like very high frequency resolution, fast frequency hopping and direct modulation. Furthermore, single-bit output has the additional advantage of requiring a single-bit DAC for the conversion of the digital output to analog. Single-bit DACs are inherently linear and only subject to gain and offset errors, which can be easily corrected. On the contrary, multi-bit DACs degrade the spectral quality of the DDS' digital output due to their complex nonlinearities and they are power hungry as well. However, traditional all-digital single-bit-output synthesizers like the PDDS and the Flying-Adder (FA) synthesizers [1]-[2] suffer from spurious tones and high deterministic jitter. Dithering has been shown to eliminate these problems [3]but it introduces a high noise floor [3].

A solution to the high noise floor problem is the introduction of noise shaping using a single-bit band-pass Σ/Δ modulator after the PDDS' cosine look-up table (LUT) as shown in Fig. 1. This way, the quantization noise spectral power is shaped away from the carrier.

The Σ/Δ band-pass modulator is formed using a *quadrature homodyne filter* (QHF) topology and a multiplier-free variation of the filter is presented to reduce complexity. Section II presents the frequency synthesizer architecture followed by the multiplier-free QHF topology. Section III expands the synthesizer to an all-digital single-bit-output transmitter with phase, frequency and amplitude modulation, and, presents simulation results of 16-QAM modulation demonstrating the capabilities of the architecture. Finally, section IV concludes the discussion.

II. All-Digital Frequency Synthesis Based on Single-Bit Sigma-Delta Modulation

Single-bit direct all-digital frequency synthesis can be achieved using the architecture in Fig. 1. Phase modulation is realized by adding a modulating signal to the input (phase) of the cosine LUT. Amplitude modulation is implemented by multiplying the cosine LUT output with the modulating signal.

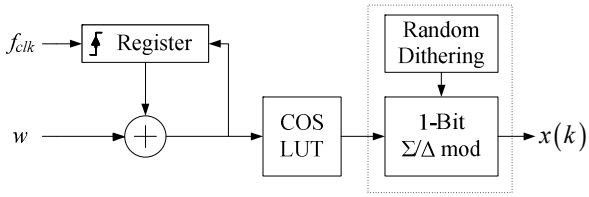

Fig. 1: DDS with Single-Bit Σ/Δ Band-Pass modulator.

The adder and the register form the phase accumulator generating $(kw) \bmod 2^n$ on the k-th rising clock edge, where w is the frequency control word (FCW) and n is the bit-width of the register. The register's value is fed to the cosine LUT giving $\cos\left(2\pi kw / 2^n\right)$. The LUT output is passed through a single-bit band-pass Σ/Δ modulator shaping the quantization noise outside the band of interest. Random dithering may be added to remove any frequency spurs [3].

A. 1-bit Σ/Δ Modulator with Quadrature Homodyne Filter

The single-bit band-pass Σ/Δ modulator is shown in Fig. 2. Using the simple model of an additive noise source for the quantizer, the *signal transfer function* (*stf*) is expressed as

$$stf(z) = \frac{F(z)}{1+F(z)}. \tag{1}$$

The *noise* and *dither transfer functions* (*ntf* and *dtf*) are

$$dtf(z) = ntf(z) = \frac{1}{1+F(z)}. \tag{2}$$

Transfer function $F(z)$ is a band-pass filter. A detailed quasilinear model predicting accurately the *stf*, *ntf*, *dtf* and the stability characteristics of the modulator is given in [4].

The tunability of the carrier frequency Ω is necessary in wireless transmitters to accommodate for multiple channels operation and fine tuning. Change of Ω should be accompanied by a shift in the pass-band of $F(z)$ to maintain a clean output spectrum of the modulator around Ω. A typical band-pass filter implementation, however, would require a change in its coefficients to change its center frequency. When the filter coefficients are variable, it is very impractical to manipulate them in order to trade some accuracy for reduction or elimination of multiplications (by expressing them as reduced sums of powers of 2). This would lead to hardware complexity reduction, increased operating frequency and reduced power consumption. Instead, this can be easily done using the quadrature homodyne filter (QHF) architecture [4] since its coefficients are fixed.

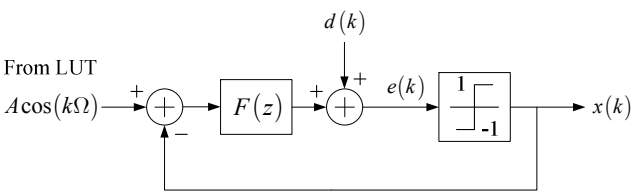

Fig. 2: Single-bit band-pass Σ/Δ modulator with dithering $d(k)$.

The QHF architecture, shown in Fig. 3, implements the band-pass filter $F(z)$ using two fixed identical low-pass filters $H(z)$ and quadrature homodyne down- and up-conversion to achieve band-pass frequency response centered at the carrier angular frequency Ω. The same LUT generates the *cosine* and *sine* signals with the appropriate phase difference of $\pi/2$.

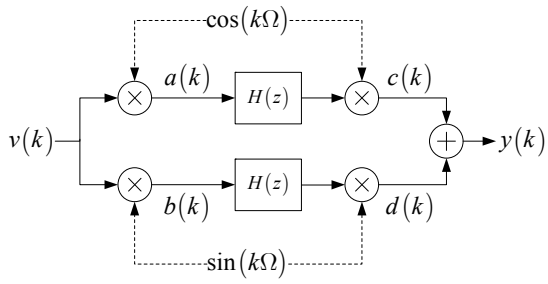

Fig. 3: The quadrature homodyne filter (QHF) architecture

It can be shown that the transfer function of the QHF in Fig. 3 is the sum of two copies of $H(z)$ frequency-shifted by $\pm\Omega$ respectively [4], i.e.

$$F(z) = \frac{1}{2}\left[H\left(ze^{-j\Omega}\right) + H\left(ze^{j\Omega}\right)\right],$$

Fig. 4 below illustrates the amplitude response of a pair of a low-pass filters $H(z)$ and the corresponding QHF $F(z)$.

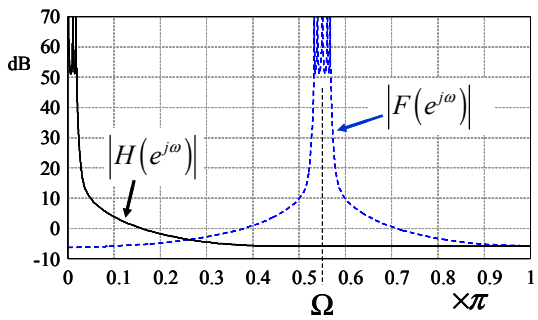

Fig. 4: Band-Pass QHF $F(z)$ response derived from Low-Pass Filter $H(z)$.

B. Removing the Four Multipliers from the QHF

The QHF architecture in Fig. 3 requires four multiplications, one addition and two identical low-pass filters. To eliminate the four multipliers we note first in Fig. 2 that the input to the filter is $v(k) = A\cos(k\Omega) - x(k)$. Assuming for now that $x \equiv 0$ we can write from Fig. 3 that $a(k) = A/2 + (A/2)\cos(2\Omega k)$ and $b(k) = (A/2)\sin(2\Omega k)$. Filter $H(z)$ is low-pass and we may safely assume that the frequency components at 2Ω and its alias at $2\pi - 2\Omega$ are sufficiently attenuated. Therefore the outputs of the filters in Fig. 3 would not change if it was $a(k) = A/2$ and $b(k) = 0$. With this in mind, the component $A\cos(k\Omega)$ in $v(k)$ has the same result as adding $A/2$ after the top-left multiplier in Fig. 3. The modification is shown in Fig. 5 where the input signal $v(k)$ is replaced by $q(k) = -x(k)$. Note now that since $x(k) = \pm 1$ the two left multiplications in the modified QHF in Fig. 5 are sign flips.

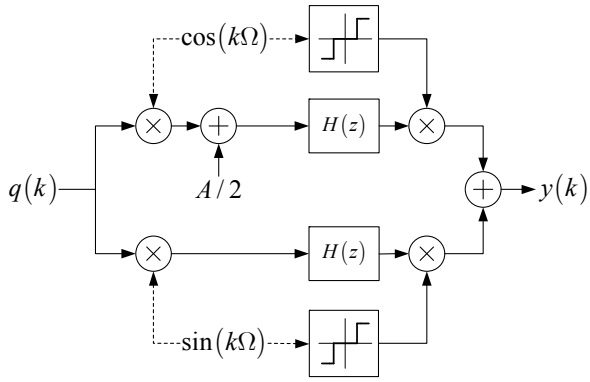

Fig. 5: Multiplier-Free Quadrature Homodyne Filter; $q(k) = -x(k)$

The other two multipliers on the right side of Fig. 3, responsible for the up-conversion, can also be eliminated. This is because simulation has shown that the output spectrum remains essentially unchanged when $\cos(k\Omega)$ and $\sin(k\Omega)$ are quantized symmetrically in three levels with thresholds $\pm\eta$, $0 < \eta < 1$, i.e. via the function Q such that $Q(x) = 0$ if $|x| < \eta$ and $Q(x) = \mathrm{sgn}(x)$ otherwise. The threshold is typically set to $\eta = 1/2$.

The aforementioned changes are reflected in Fig. 5 which is essentially multiplier-free (without taking into account those of the filters). The band-pass modulator using the multiplier-free QHF is shown in Fig. 6. Notice that now the input is half the amplitude of the initial sinusoidal input.

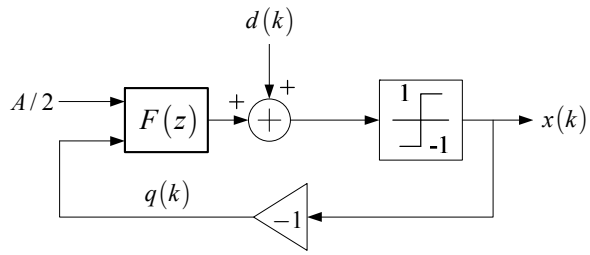

Fig. 6: Single-Bit Band-Pass Σ/Δ modulator with Multiplier-Free QHF

III. Single-Bit All-Digital Transmitter

An all-digital, single-bit output and hardware-efficient transmitter can be formed by applying carrier modulation to the combined structure of the phase accumulator and the single-bit band-pass Σ/Δ modulator with QHF, as shown in Fig. 7. Frequency modulation is achieved by varying the frequency control word w and therefore the angular frequency $\Omega = 2\pi w / 2^n$, while phase modulation is achieved by adding a phase offset $\theta(k)$ as shown in Fig. 7. Amplitude modulation is done by varying the input amplitude, i.e. $A = A(k)$.

A. 16-QAM Modulation Transmitter Simulation

The system shown in Fig. 7 has been simulated in MATLAB/Simulink using a 16-QAM modulated input signal. This modulation scheme was preferred for demonstration purposes as it is common in many IoT wireless standards.

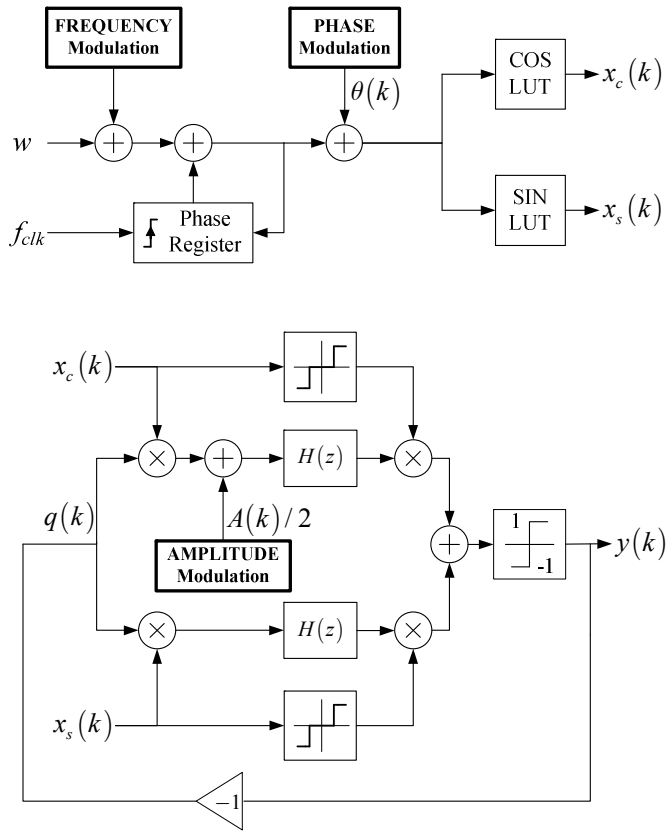

Fig. 7: All-digital transmitter based on Band-Pass Σ/Δ modulator with QHF

The input signal is generated by a sequence of random and independent uniformly distributed bits. Groups of four bits form 16-QAM symbols. The carrier frequency is $\Omega = 2\pi w / 2^n \cong 0.42\pi$ with $w = 1720$ and $n = 13$. Filter $H(z)$ is of 9-th order and a zoomed-in plot of its zeros and poles is shown in Fig. 8. The bandwidth of the resulting band-pass filter is about 0.02π and thus the transmission channel is in the frequency range $[0.41\pi, 0.43\pi]$.

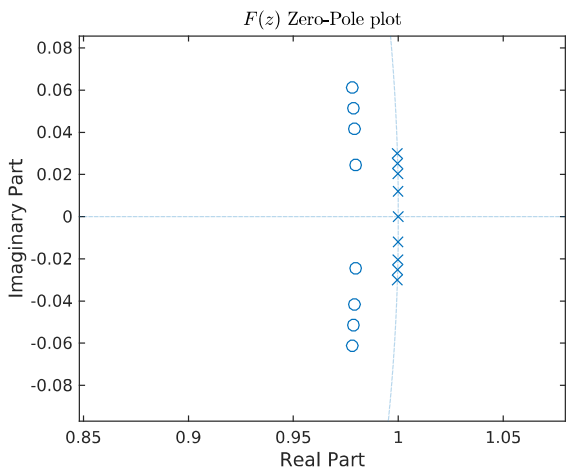

Fig. 8: Zoom-in of filter $H(z)$ zeros and poles.

B. Symbols Transmission & Receiption Simulation Setup

The setup for the 16-QAM transmitter and the receiver for generating the constellation diagram is depicted in Fig. 9. A square-root, raised cosine filter is used for pulse shaping, intersymbol interference reduction, and up-sampling of the baseband I-Q signal. The signal is then converted to polar coordinates and is fed to the multiplier-free 1-bit homodyne Σ/Δ band-pass modulator. The signal amplitude is scaled accordingly to fit the dynamic range of the Σ/Δ modulator.

For the reception, the 1-bit output of the transmitter is separated into its in-phase and quadrature components and is passed through another identical square-root, raised cosine filter for the recovery of the pulse-shaped signal and down-sampling. Amplitude gain correction is also performed.

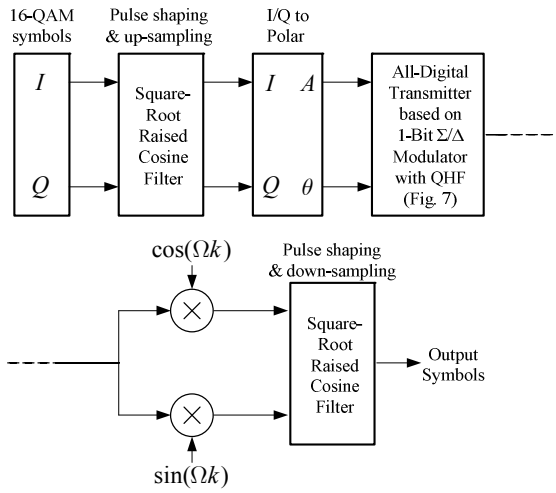

Fig. 9: 16-QAM transmitter-receiver simulation setup.

The up-sampling and pulse-shaping operations ensure that the up-converted baseband spectrum is a (small) part of the bandwidth of the band-pass Σ/Δ modulator. In our test-case an OSR (oversampling ratio) of 8192 is used. The square-root, raised cosine filters are designed to span 10 symbols with roll-off factor $\beta = 0.25$.

C. Simulation Results

Using the aforementioned system parameters, the near-in Σ/Δ modulator's spectrum in Fig. 10 was obtained with 10,000 symbols. Notice that the bandwidth of the modulator (noise suppressed frequency range) is much wider and so the modulated carrier can be isolated from the side-band quantization noise via an external analog filter. Moreover, multiple channels can fit inside the pass-band.

After demodulation, the constellation diagram of Fig. 11 was attained, resulting in an RMS EVM of 0.94%. Assuming a clock frequency of 1 GHz, the proposed all-digital transmitter is capable of achieving a symbol rate of 122 Ksymbols/s. For 16-QAM modulation this is translated to a data rate of 488 Kbits/s. This exceeds the typical requirements for IoT applications and can be increased further if a smaller OSR is used. E.g. OSR=512 increases the data rate to 7.812 Mbits/s, with the cost of reducing the number of available channels in the pass-band.

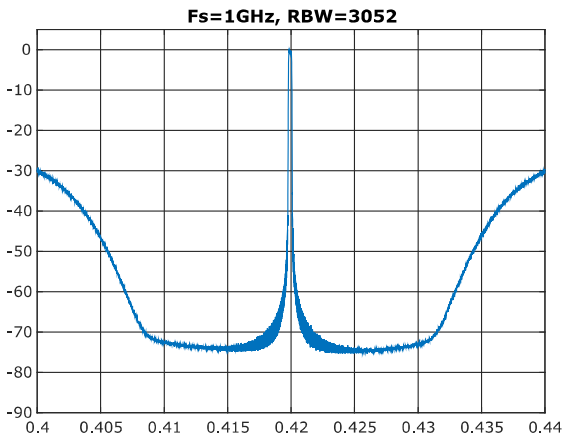

Fig. 10: Near-in spectrum of the transmitter with 16-QAM modulation.

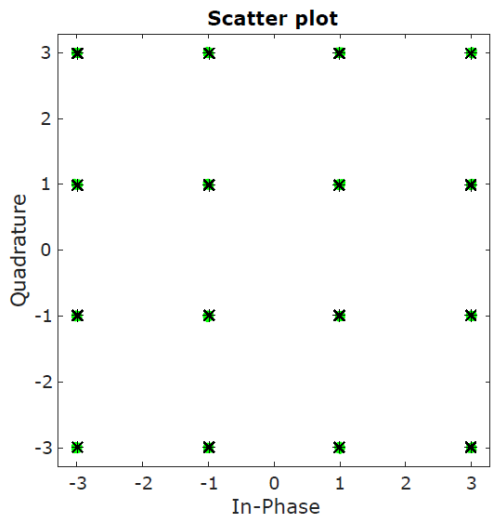

Fig. 11: Constellation diagram of 16-QAM. The asterisks mark the input symbol locations and the green dots the received symbols.

IV. Conclusion

Single-bit all-digital frequency synthesis architectures based on sigma-delta modulation with homodyne band-pass filtering have been proposed leading to all-digital transmitters whose simplicity makes them potential candidates for a diverse range of IoT applications. MATLAB simulation demonstrates the capabilities of the proposed architectures.

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