All-Digital Single-Bit-Output RF Transmitters Using Homodyne Sigma-Delta Modulation

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***Abstract*—An all-digital RF transmitter architecture capable of driving directly a switching RF power amplifier and therefore without the need of a high-speed RF DAC is presented. Modulation is achieved by directly modulating a direct digital synthesizer (DDS) generated signal. The proposed architecture is based on single-bit sigma-delta modulation using the introduced homodyne band-pass filter topology, which allows for the adjustment of its central frequency without changing its coefficients. This is achieved by using variable frequency homodyne down- and up-conversion along with a low-pass filter with fixed coefficients. Furthermore, a multiplier-less homodyne filter topology is shown to be possible, greatly reducing the hardware requirements for its implementation. MATLAB simulation results are presented based on a 64-QAM modulation scheme demonstrating the capabilities of the proposed architecture.**

***Index Terms*—Digital-to-frequency converter, direct digital synthesizer, RF transmitter, all-digital, homodyne, filter, frequency synthesis, noise shaping, sigma-delta, single-bit quantization**

I. Introduction

Low power and low cost wireless transceivers are continuously gaining importance. The Internet of Things (IoT) concept [1], where an increasing number of autonomous devices are part of a large network, plays a significant role in this direction. Since there is a large number of diverse wireless protocols adopted for IoT applications, an appropriate RF transmitter architecture should be able to deal with all these protocols.

All-digital transmitters do not rely on analog components apart from a switching power amplifier (PA) and an analog band-pass filter just before the antenna. The advantages of digital circuits range from immunity to noise and temperature, supply and process variations to short concept-to-market time due to the availability of powerful design and verification automation tools. Moreover, migration of digital circuits to newer, smaller scale integrated circuit (IC) technologies is faster and more straightforward than that of analog or mixed-signal ones. They are also more easily co-integrated with other digital circuitry, such as DSP engines.

Single-bit quantization is essential to avoid having an RF DAC and to be able to drive directly an energy efficient switching PA like a class-D PA. Furthermore, using only 1-bit allows for inherently linear operation, subject only to gain and offset errors which can be easily corrected and to not affect the generated output spectrum. Traditional single-bit synthesizers like the PDDS (pulse direct digital synthesizer) [2] and the Flying-Adder (FA) synthesizer [3], suffer from spurious tones and high deterministic jitter. Dithering has been shown to eliminate these problems [4], but it introduces a high noise floor.

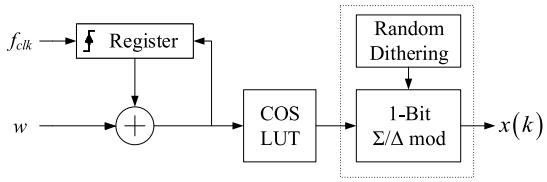

Fig. 1. PDDS with Σ/Δ noise shaping.

A solution to the high noise floor problem is the introduction of noise shaping using a single-bit band-pass Σ/Δ modulator after the PDDS cosine look-up table (LUT) as shown in Fig. 1. Now, the quantization noise is shaped away from the carrier.

In this paper the Σ/Δ band-pass modulator is built using a quadrature homodyne filter architecture. A multiplier-less version of the filter is also presented. In section II the proposed frequency synthesizer architecture is described and mathematically analyzed followed by the multiplier-less quadrature homodyne filter topology presentation. Simulation results demonstrating the effectiveness of the proposed architecture as a digital transmitter are presented in section III. Section IV concludes the discussion.

II. Sigma-Delta Modulation for All-Digital Frequency Synthesis

The architecture in Fig. 1 can be used for all-digital frequency synthesis with direct modulation capabilities. Amplitude modulation is achieved by multiplying the cosine LUT output with the modulating signal, whereas phase modulation is possible by adding a modulating signal to the cosine phase, i.e. the LUT input.

The phase accumulator, i.e. the adder and the accumulator register, generates $kw \mod 2^n$ on the k-th rising clock edge, where w is the frequency control word (FCW). The phase signal is fed to the cosine LUT which outputs $\cos(2\pi kw/2^n)$, where n is the bit-width of the phase accumulator. The LUT output is passed through a single-bit band-pass Σ/Δ modulator which shapes in-band quantization noise away from the band

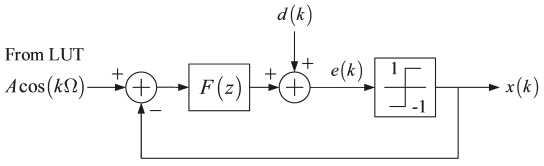

Fig. 2. The single-bit band-pass Σ/Δ modulator.

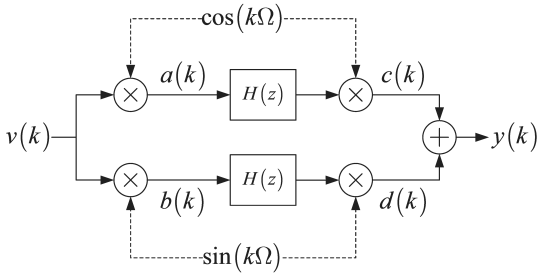

Fig. 3. The quadrature homodyne filter architecture.

of interest. Random dithering may be added to remove any frequency spurs [4].

A. 1-bit Σ/Δ Modulator with Quadrature Homodyne Filter

The 1-bit band-pass Σ/Δ modulator is depicted in Fig. 2. Replacing the quantizer by an additive noise source, the signal transfer function (stf) is expressed as $stf\left(z\right) = F\left(z\right)/\left(1+gF\left(z\right)\right)$ and the noise transfer and dither transfer functions (ntf and dtf) respectively are $dtf\left(z\right) = ntf\left(z\right) = 1/\left(1+gF\left(z\right)\right)$. $F(z)$ is a band-pass filter and g is an optional feedback gain. A more accurate quasilinear model predicting the stf, ntf, dtf and the stability characteristics of the modulator is presented in [5].

The carrier frequency Ω should be tunable to accommodate for multiple channels operation and fine tuning. However, if Ω is changed, the central frequency of the band-pass filter $F(z)$ should follow this change to maintain a clean output spectrum centered at the carrier. A typical band-pass filter implementation would require different coefficients, canceling any design optimizations tailored to a fixed set of coefficients, such as elimination of multiplications by expressing the filter coefficients as reduced sums of powers of 2. The quadrature homodyne filter architecture (QHF) can address this issue.

As shown in Fig. 3, the QHF architecture implements the band-pass frequency response of filter $F(z)$ using two fixed identical low-pass filters $H(z)$. Quadrature homodyne down-conversion is used to translate the carrier with angular frequency Ω to DC before it is processed by filter $H(z)$. The resulting signal is then translated back to Ω using quadrature homodyne up-conversion.

The cosine and sine signals can be generated by the same LUT with the appropriate phase difference of $\pi/2$. By inspecting the system in Fig. 3 and using the properties of z-transform the derivation of the QHF transfer function is straightforward. The z-transforms of the down-converted signals at $z = e^{j\omega}$ are

$$A\left(e^{j\omega}\right) = \frac{1}{2}\left[V\left(e^{j(\omega-\Omega)}\right) + V\left(e^{j(\omega+\Omega)}\right)\right]$$
$$B\left(e^{j\omega}\right) = \frac{1}{2i}\left[V\left(e^{j(\omega-\Omega)}\right) - V\left(e^{j(\omega+\Omega)}\right)\right]$$

After low-pass filtering and up-conversion we get

$$C\left(e^{j\omega}\right) = \frac{1}{2}\left[H\left(e^{j(\omega-\Omega)}\right)A\left(e^{j(\omega-\Omega)}\right) + H\left(e^{j(\omega+\Omega)}\right)A\left(e^{j(\omega+\Omega)}\right)\right]$$
$$D\left(e^{j\omega}\right) = \frac{1}{2i}\left[H\left(e^{j(\omega-\Omega)}\right)B\left(e^{j(\omega-\Omega)}\right) - H\left(e^{j(\omega+\Omega)}\right)B\left(e^{j(\omega+\Omega)}\right)\right]$$

Thus, the QHF output is $Y\left(e^{j\omega}\right) = \frac{1}{2}\left[H\left(e^{j(\omega-\Omega)}\right) + H\left(e^{j(\omega+\Omega)}\right)\right]V\left(e^{j\omega}\right)$. So, the transfer function of QHF is the sum of two copies of $H(z)$ frequency-shifted by $\pm\Omega$, i.e.

$$F\left(z\right) = \frac{1}{2}\left[H\left(ze^{-j\Omega}\right) + H\left(ze^{j\Omega}\right)\right].$$

For the implementation of the QHF architecture in Fig. 3 four multiplications, an addition and two identical low-pass filters are required. As shown next, the multiplications can be avoided.

B. Multiplier-Free Quadrature Homodyne Filter

The first step to eliminate the multipliers in the QHF is to observe in Fig. 2 that the input to filter $F(z)$ is $v\left(k\right) = A\cos\left(k\Omega\right) - x\left(k\right)$. Assuming for now that $x \equiv 0$, considering the system in Fig. 3 and using some basic trigonometric identities it holds that $a\left(k\right) = A/2 + \left(A/2\right)\cos\left(2\Omega k\right)$ and $b\left(k\right) = \left(A/2\right)\sin\left(2\Omega k\right)$. Since filter $H(z)$ is low-pass we may safely assume that the frequency components at 2Ω and their alias at $2\pi - 2\Omega$ are sufficiently attenuated. Therefore the outputs of the filters would practically remain unchanged if $a(k)$ and $b(k)$ were replaced by $\tilde{a}(k) = A/2$ and $\tilde{b}(k) = 0$. With this in mind, the $A\cos(k\Omega)$ component of the filter input $v(k)$ can be replaced by adding $A/2$ after the top-left multiplier in Fig. 3. Since the other component of $v(k)$ is $-x(k)$ we define the new filter input signal $q(k) = -x(k)$ which takes only two values, $+1$ and -1. The aforementioned modifications are shown in Fig. 4. Notice that now the two left-most multiplications in the modified QHF in Fig. 4 are reduced to simple sign flips.

The two right-hand side multipliers, responsible for the up-conversion, can also be omitted. Simulation has shown that the filter output remains essentially unchanged when $\cos(k\Omega)$ and $\sin(k\Omega)$ are quantized symmetrically in three levels with quantization step η, such that $Q(x) = 0$ if $|x| < \eta$ and $Q(x) = \mathrm{sgn}(x)$ otherwise, where $Q(\cdot)$ denotes the quantization function. A typical threshold value is $\eta = 1/2$.

The aforementioned changes are reflected in Fig. 4. Ignoring the low-pass filter $H(z)$ multipliers, the modified QHF is multiplier-free. $H(z)$ can be designed to have coefficients

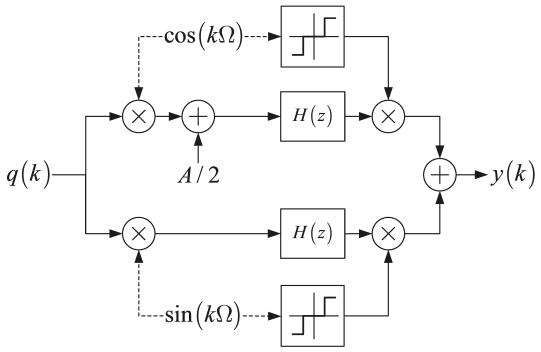

Fig. 4. Quadrature homodyne filter multiplier-free architecture.

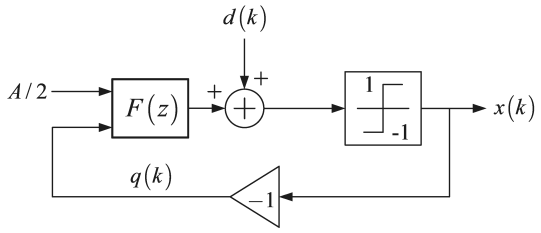

Fig. 5. The single-bit band-pass Σ/Δ modulator with quadrature homodyne filter multiplier-free architecture.

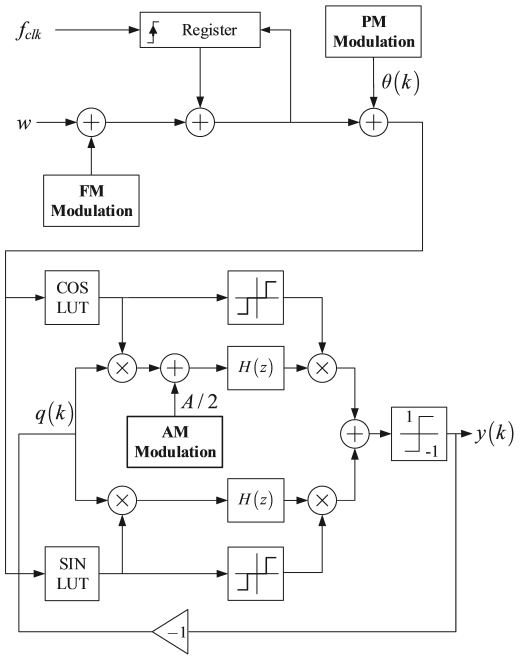

Fig. 6. The digital transmitter system with single-bit band-pass Σ/Δ quadrature homodyne filter architecture.

which are sums of two or three powers of 2 and thus it can also be multiplier-free. The single-bit band-pass Σ/Δ modulator using the multiplier-free QHF is shown in Fig. 5. Notice that now the input is half the amplitude of the initial sinusoidal input.

C. Amplitude and Frequency Modulation

Amplitude modulation is achieved by varying the input amplitude with time, i.e. $A = A(k)$, while frequency and/or phase modulation are achieved by varying the input angular frequency, i.e. $\Omega = \Omega\,(k) + \Delta\Omega\,(k)$, and/or adding an offset phase $\theta(k)$ to the input signal respectively. The complete hardware-efficient all-digital transmitter based on the 1-bit band-pass Σ/Δ modulator with the multiplier-free QHF is shown in Fig. 6. Simulation results of 64-QAM modulation are presented in the following section.

III. 64-QAM Modulation Simulation Results

The digital transmitter system shown in Fig. 6 has been simulated in MATLAB/Simulink using a 64-QAM modulated input signal. This modulation scheme was preferred for demonstration purposes as it is common in many IoT wireless standards. Other modulation standards based on amplitude and phase or frequency modulation can be implemented as well.

The input signal is generated by a random sequence of bits with uniform distribution. Groups of six bits are combined to form a 64-QAM symbol. The carrier frequency of the transmitter is $f = w/2^n$ with $w = 1720$ and $n = 13$ resulting in an angular frequency of $\Omega = 0.42\pi$. The homodyne filter $H(z)$ is low-pass of order 9. The bandwidth of the resulting band-pass filter is 0.02π and thus the transmission channel lies in the frequency range $[0.41\pi, 0.43\pi]$.

A. 64-QAM Modulation Simulation Setup

The complete 64-QAM modulation-demodulation setup for the simulation is depicted in Fig. 7. Pulse shaping for ISI (intersymbol interference) reduction and up-sampling of the baseband I-Q signal are performed by a square-root, raised cosine filter. The up-sampling and pulse-shaping operations ensure that the up-converted baseband spectrum is a (small) part of the bandwidth of the pass-band Σ/Δ modulator. In our test-case an OSR (oversampling ratio) of 8192 is used. The square-root, raised cosine filters are designed to span 10 symbols with roll-off factor $\beta = 0.25$. After filtering, the signal is converted to polar coordinates and is fed to the multiplier-free 1-bit homodyne Σ/Δ band-pass modulator. The signal amplitude is scaled appropriately to be within the dynamic range of the Σ/Δ modulator. Here, a gain of 2 is used.

For the demodulation process, the 1-bit output of the modulator is separated into its in-phase and quadrature components and is passed through another identical square-root, raised cosine filter for the recovery of the pulse-shaped signal and down-sampling. An amplitude gain correction is also performed.

B. Simulation Results

Using the aforementioned setup, the near-in spectrum of the Σ/Δ modulator output depicted in Fig. 8 was obtained for 10,000 symbols. Notice that the bandwidth of the modulator (noise suppressed frequency range) is much larger and so

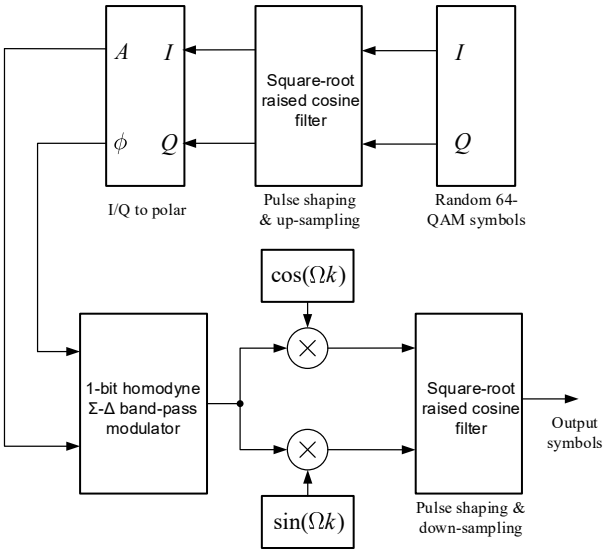

Fig. 7. 64-QAM modulation-demodulation simulation setup.

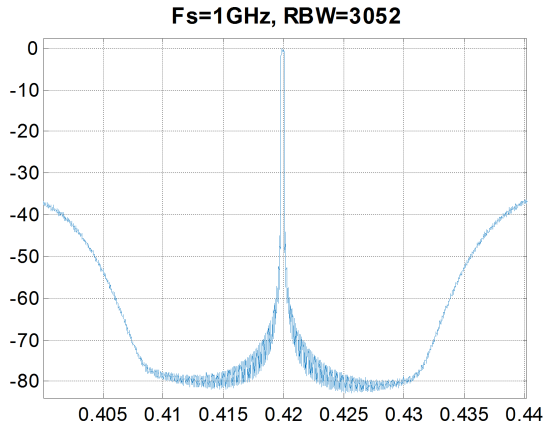

Fig. 8. All-digital RF transmitter output spectrum with 64-QAM modulation and OSR = 8192. Y-axis in dB, X-axis: Discrete-Time Frequency Ω.

the modulated carrier can be isolated from the side-band quantization noise via an external analog filter and multiple channels can fit inside the passband.

After demodulation, the constellation diagram of Fig. 9 was attained, yielding an RMS EVM of 0.955%. Assuming a clock frequency of 1 GHz, the proposed all-digital transmitter is capable of achieving a symbol rate of 122 Ksymbols/s. For 64-QAM modulation this is translated to a data rate of 732 Kbits/s. This exceeds the typical requirements for most IoT applications as it can be seen in Table I. Nevertheless, a much lower OSR can be used, e.g. 512, increasing the data rate to 11.718 Mbits/s, with the cost of reducing the number of available channels in the passband.

IV. Conclusion

A class of all-digital RF transmitters with single-bit digital output has been presented. They are based on single-bit sigma-delta modulators with band-pass filters implemented using the

TABLE I
IoT Wireless Protocol Requirements

Protocol	Frequency band(s)	Data rate
Bluetooth	2.4 GHz	1 Mbps
Zigbee	2.4 GHz	250 Kbps
Z-Wave	900 MHz	9.6-100 Kbps
NFC	13.56 MHz	100-420 Kbps
Sigfox	900 MHz	10-1000 bps
Neul	900 / 470-790 MHz	<100 Kbps
LoRaWAN	Various	0.3-50 Kbps

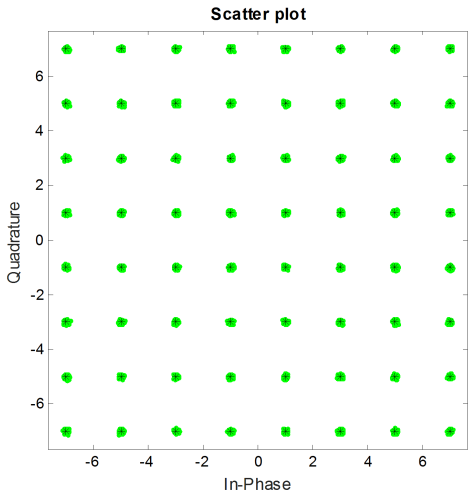

Fig. 9. Constellation of 64-QAM modulation with OSR = 8192. The asterisks mark the input symbol locations and the green dots the demodulated symbols.

introduced homodyne topology. They accept direct amplitude, phase and frequency modulation. MATLAB simulation results illustrate the output spectrum achieved in the case of an example 64-QAM modulation scheme.

References

[1] J. W. Chuah, "The Internet of Things: An overview and new perspectives in systems design," in *IEEE Int. Symp. on Integr. Circ. (ISIC)*, Dec. 10–12, 2014, pp. 216–219.

[2] V. S. Reinhardt, "Direct digital synthesizers," *Technical Report, Hughes Aircraft Co, Space and Communications Group, L.A., CA*, Dec. 1985.

[3] L. Xiu and Z. You, "A "flying-adder" frequency synthesis architecture of reducing VCO stages," *IEEE Trans. VLSI Syst.*, vol. 13, no. 2, pp. 201–210, Feb. 2005.

[4] P. P. Sotiriadis, "Spurs-free single-bit-output all-digital frequency synthesizers with forward and feedback spurs and noise cancellation," *IEEE Trans. Circuits Syst. I*, vol. 63, no. 5, pp. 567–576, May 2016.

[5] ——, "Single-bit all digital frequency synthesis using homodyne sigma-delta modulation," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 64, no. 2, pp. 463–474, Feb. 2017.