The Class of 1-bit Multi-Step Look-Ahead ΣΔ Modulators and Their Applications

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***Abstract*—The class of 1-bit Multi-Step Look-Ahead (MSLA) ΣΔ modulators is presented. They take into account current and future quantization errors improving upon the stability and noise shaping characteristics of conventional 1-bit ΣΔ modulators. The MSLA modulator system is found to be equivalent to a number of parallel conventional ΣΔ modulators sharing a multi-input 1-bit quantizer. The number of look-ahead steps along with other design parameters enable fine-tuning of performance vs. hardware complexity according to the application. The performance of MSLA modulators for various design parameter values is investigated, highlighting their advantages in a multitude of applications like digital transmitters, class-D power amplifiers and DACs.**

***Index Terms*—Sigma-delta, noise shaping, 1-bit quantization, modulator, all-digital, optimization algorithm, DAC, digital transmitter, look-ahead**

I. Introduction

Noise shaping is employed in ΣΔ modulators, trading increased sampling rate for reduced noise in a desired frequency band [1]. This is especially useful in data converters where device mismatches limit the accuracy of Nyquist-rate converters. ΣΔ data converters use oversampling and noise shaping to increase the conversion accuracy. Other applications of ΣΔ modulators include fractional-N PLLs, digital transmitters [2], all-digital frequency synthesizers [3], [4], class-D power amplifiers, SA-CD and digital microphone bitstream encoding [5], [6], to name but a few. Excluding ADCs, all other applications rely on digital ΣΔ modulators. The advantages of digital circuits are numerous. The most significant ones are the availability of design automation tools leading to faster concept-to-market time, the straightforward migration of a design to a smaller technology and their immunity to thermal noise and process, voltage and temperature variations.

The bandwidth and dynamic range of ΣΔ modulators are limited by the stability of their loop [1]. The use of a multi-bit quantizer relaxes these limitations, but introduces the problem of DAC nonlinearity due to device mismatches resulting in output spectrum degradation. Furthermore, many applications such as class-D power amplifiers, digital microphones and SA-CD require a 1-bit output. Look-ahead ΣΔ modulators have been proposed to improve stability and dynamic range while maintaining 1-bit output [5]. Their main advantage is the possibility to use NTFs (noise transfer functions) with higher out-of-band gain than conventional ΣΔ modulators. This results in higher in-band noise attenuation and thus higher SNDR (signal to noise and distortion ratio). Moreover, for a given NTF, a look-ahead ΣΔ modulator remains stable for larger input amplitude ranges.

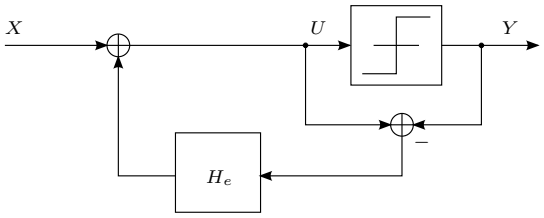

Fig. 1. The EF SDM system diagram.

The algorithmic complexity of the full look-ahead ΣΔ modulator increases exponentially with the number of look-ahead steps. Reduced complexity algorithms such as the M-algorithm [7], pruned-tree ΣΔ modulation [5] and the MSLA (multi-step look-ahead) modulator [8] have been proposed. They allow for more look-ahead steps and thus better noise shaping characteristics, while maintaining lower algorithmic complexity. A comparison of the various look-ahead algorithms in terms of their complexity and performance can be found in [8].

This paper focuses on MSLA modulators and their applications. The next section introduces them along an analysis of their design parameters. In section III design examples of MSLA modulators for various applications are presented, accompanied by simulation results. Finally, section IV concludes the discussion.

II. MSLA Modulator Basics

The error-feedback ΣΔ modulator (EF SDM) depicted in Fig. 1 forms the basis for the derivation of the MSLA modulator. The key idea is to formulate the EF SDM as an optimization algorithm and extend it to include future outputs in the optimization process. Consider now the system in Fig. 2 with output

$$Y(z) = X(z) + \frac{1}{1+G(z)}N(z), \tag{1}$$

where $X(z)$, $Y(z)$ and $N(z)$ are the z-transforms of the modulator input x_n, output y_n and quantization error $y_n - u_n$ re-

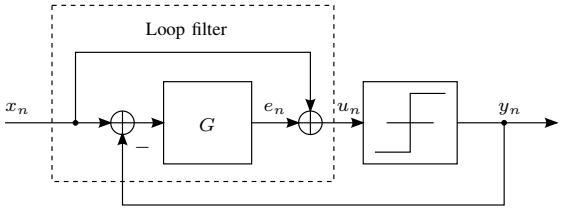

Fig. 2. The equivalent transformed EF SDM system diagram.

spectively. Filter G is selected as $G(z) = H_e(z)/\left(1 - H_e(z)\right)$ for the systems in Figs. 1 and 2 to be equivalent. It is known as the *comparison filter*. From (1) one concludes that the signal transfer function (STF) is $STF(z) = 1$ and the NTF is $NTF(z) = 1/\big(1 + G(z)\big)$. The general form of $G(z)$ is

$$G(z) = \frac{1 - NTF(z)}{NTF(z)} = \frac{\sum_{i=1}^{\ell} b_i z^{-i}}{1 + \sum_{i=1}^{m} a_i z^{-i}}. \tag{2}$$

As shown in [7], the same output y_n is obtained using the optimization algorithm

$$y_n = \underset{v\in\{\pm1\}}{\arg\min} |x_n + e_n - v|. \tag{3}$$

$|x_n + e_n - v|$ is the cost function and the modulator output y_n is the value of $v \in \{\pm1\}$ which minimizes the cost function. e_n is the n-th output of the comparison filter G with input sequence $\{x - y\}$.

A. The MSLA Modulator Optimization Algorithm

Extending the aforementioned optimization algorithm to take into account the costs associated with k future samples we derive the MSLA modulator optimization algorithm:

$$y_n = \underset{v_0\in\{\pm1\}}{\arg\min} \left(\min_{\substack{v_1,v_2,\ldots,v_k\in \\ \{\pm1\}}} \sum_{j=k-r}^{k} |x_{n+j} + e_{n+j} - v_j|^p \right). \tag{4}$$

Here k is the number of look-ahead steps and $r + 1$ is the number of partial costs

$$S_{j,n}(v_0, v_1, \ldots, v_j) \equiv |x_{n+j} + e_{n+j} - v_j|^p \tag{5}$$

taken into account. Notice that the extra parameter p is introduced compared to (3). It denotes that the cost function is the p-norm distance of the optimizing variables vector $\mathbf{v} = (v_{k-r}, v_{k-r+1}, \ldots, v_k)$ from the vector incorporating the input and the comparison filter output samples $(x_{n+k-r} + e_{n+k-r}, x_{n+k-r+1} + e_{n+k-r+1}, \ldots, x_{n+k} + e_{n+k})$. The most common choice is $p = 2$ as it minimizes the total quantization error power yielding the best SNDR. However, a value of $p = 1$ leads to a more efficient hardware implementation [8] with a small SNDR penalty.

B. MSLA Modulator Efficient Form

The computational complexity of calculating the MSLA modulator output y_n by directly evaluating (4) increases exponentially with k. In [8] it is shown that the calculations may be significantly reduced using the equivalent system description

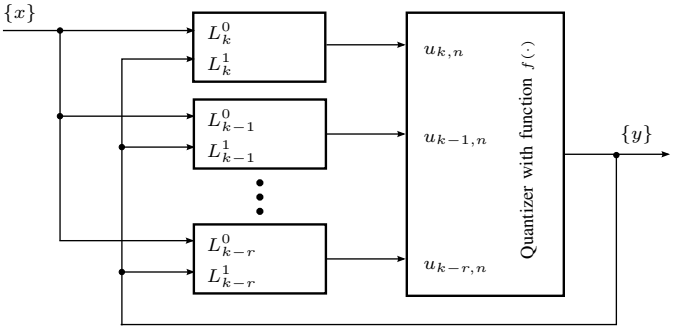

Fig. 3. The MSLA modulator efficient form system diagram.

in Fig. 3. In this description the modulator is comprised of $r+1$ two-input filters and an $(r + 1)$-input 1-bit output quantizer.

The transfer functions of the filters in Fig. 3 are given by

$$L_j^0(z) = \sum_{i=0}^{j+\ell-1} c_{j,i} z^{j-i} + G(z) \sum_{i=0}^{m-1} d_{j,i} z^{-i} \tag{6}$$

$$L_j^1(z) = -\sum_{i=j+1}^{j+\ell-1} c_{j,i} z^{j-i} - G(z) \sum_{i=0}^{m-1} d_{j,i} z^{-i} \tag{7}$$

with $k - r \le j \le k$. Coefficients $c_{j,i}$ and $d_{j,i}$ are derived from the comparison filter G coefficients b_i and a_i. The equations defining their values are thoroughly discussed in [8]. The filter outputs $u_{j,n},\ k - r \le j \le k$ are given by the difference equation

$$u_{j,n} = \sum_{i=0}^{j} c_{j,i} x_{n+j-i} + \sum_{i=j+1}^{j+\ell-1} c_{j,i} \left(x_{n+j-i} - y_{n+j-i}\right) + \sum_{i=0}^{m-1} d_{j,i} e_{n-i}. \tag{8}$$

The filter output vector $\mathbf{u} = (u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n})$ is then fed to the $(r + 1)$-input 1-bit quantizer.

The quantizer mapping function $f(\cdot)$ depends on the comparison filter G, the number of look-ahead steps k and the number of partial costs $r + 1$. It is a time-invariant function, i.e. it does not depend on n. In [8] it is shown that

$$f(\mathbf{u}) = \underset{v_0\in\{\pm1\}}{\arg\min} \left(\min_{\substack{v_1,v_2,\ldots,v_k\in \\ \{\pm1\}}} \sum_{j=k-r}^{k} \left| u_{j,n} - \sum_{i=0}^{j} c_{j,i} v_{j-i} \right|^p \right). \tag{9}$$

Therefore, the MSLA modulator output is equivalently given by

$$y_n = f(u_{k-r,n}, u_{k-r+1,n}, \ldots, u_{k,n}). \tag{10}$$

Consequently y_n is determined by the least p-norm distance of the quantizer input vector $\mathbf{u}$ from a set of points with coordinates $\sum_{i=0}^{j} c_{j,i} v_{j-i}$ in u_j axes, $k - r \le j \le k$. There is one point for each possible sequence $\{v\} = (v_0, v_1, \ldots, v_k),\ v_i \in \{\pm1\}$, resulting in a total of 2^{k+1} points in $(r+1)$-dimensional space. The advantage of using (10) over (4) is that now $f(\mathbf{u})$ can be evaluated during design for all possible values of input

vector $\mathbf{v}$ and store the results, i.e. implement $f(\cdot)$ as a look-up table (LUT). Alternatively, $f(\mathbf{u})$ can be reduced to a system of inequalities involving the input vector $\mathbf{v}$ which is much easier to calculate during operation than the direct evaluation of (4). To make the difference more concrete, calculation of y_n using (10) requires the calculation of $r+1$ filter output values using (8), while directly calculating y_n through (4) requires $(k+1)\cdot 2^{k+1}$ filter output calculations.

For a more thorough analysis the reader is referred to [8]. Therein it is also shown that MSLA modulators achieve the same or better performance than other look-ahead techniques with comparable algorithmic complexity.

C. The MSLA Design Parameters

The various design parameters of the MSLA modulator play a significant role in its performance and hardware complexity. A careful selection of their values is therefore needed to maximize the benefits while keeping a relatively low hardware complexity. The available design parameters are numerous as the MSLA modulator offers more design flexibility than conventional ΣΔ modulators through the values of k, r and p. This flexibility also manifests itself in the NTF design procedure. Next, the design trade-offs associated with each parameter are discussed.

1) The Effect of Look-Ahead Steps k: The most influential parameter of a MSLA modulator is the number of look-ahead steps k. As it is increased, the stable input signal range is also increased [8]. Furthermore, a higher value of k enables the use of a NTF with higher out-of-band gain and thus higher output SNDR, while it also suppresses non-linear effects such as frequency spurs and harmonics.

2) The Effect of the Number of Partial Costs r: The number of partial costs in (4) and (9) is denoted as r. For maximum SNDR it should be $r = k$. Using $r < k$ is a way to reduce the hardware complexity, while maintaining improved stability. This comes, however, at the expense of reduced SNDR [8], which in some applications might be acceptable.

As it can be seen in Fig. 3, the value of r has a significant impact on hardware complexity. The number of loop filters and thus the number of the quantizer inputs are equal to $r+1$. This means that as r is increased, more IIR filters need to be implemented, whereas the complexity of the $(r+1)$-input quantizer also increases. If the quantizer is implemented as a ROM, a higher value of r results in higher memory size requirements, i.e. more area and increased power consumption. If a comparator-based quantizer implementation is preferred instead, higher values of r are manifested as increased delay and thus lower operating frequency.

3) The Effect of the Partial Cost Norm: In (5) and (9) the partial costs are parameterized on p. The value of p has an impact on the transfer function and the complexity of the $(r+1)$-input quantizer in Fig. 3. As it is mentioned in [8] a value of $p = 1$ results in a lower complexity comparator-based quantizer implementation compared to a value of $p = 2$.

The value of p also influences the SNDR and the stability limits. Using $p = 2$ typically results in higher SNDR (2-3 dB) than using $p = 1$, because in that case the total quantization error power is minimized. Furthermore, using $p = 2$ allows for slightly larger stable input dynamic range.

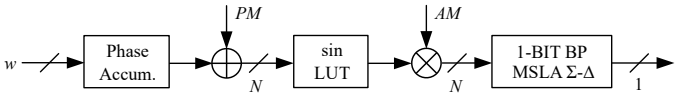

Fig. 4. All-digital frequency synthesizer using a 1-bit band-pass MSLA modulator.

III. MSLA Modulator Applications

MSLA modulators can offer improved performance over conventional ΣΔ ones when 1-bit output, high SNDR and large signal bandwidth are required. Some applications that benefit from using MSLA modulators are presented next.

A. Direct Frequency Synthesizer / All-Digital Transmitter

A MSLA modulator can be used as part of a direct frequency synthesizer to generate frequencies in a wide frequency band requiring a single clock. The direct frequency synthesizer can be easily modified to allow phase and amplitude modulation and thus it can double as an all-digital transmitter. An all-digital design requires a 1-bit output to avoid having a multi-bit DAC at its output, which would introduce nonlinear effects due to device mismatches. A straightforward approach is the PDDS (pulse direct digital synthesizer) [9], but its output spectrum is full of undesired frequency spurs. Dithering has been proposed to convert the frequency spurs to a noise floor [10], but the SNDR and dynamic range (DR) are relatively low. Higher SNDR and DR are possible over a wide frequency band if a 1-bit band-pass MSLA modulator is used as seen in Fig. 4. Notice that phase (PM) and amplitude modulation (AM) can be added to convert the MSLA DDS into an all-digital transmitter.

Using the Matlab Delta Sigma Toolbox [11] we create an 8-th order NTF with optimized zeros, central frequency $\omega_0 = 2\pi \cdot 0.38$, out-of-band gain $||\mathrm{NTF}||_\infty = 2$ and oversampling ratio $\mathrm{OSR} = 16$. The MSLA modulator of the frequency synthesizer in Fig. 4 is configured with this NTF to generate a sinusoidal with frequency $\omega = 2\pi \cdot 0.39$ and amplitude $A = 0.3$. Here, $k = 7$ look-ahead steps are used with $r = k$ and $p = 2$. From Fig. 5 it is seen that a spurious free dynamic range (SFDR) of 122 dB is achieved when accounting for the resolution bandwidth of the FFT. Assuming a 200 MHz clock which is feasible with a low end FPGA, the resolution bandwidth for 125000 output samples is $\mathrm{RBW} = 1600$ Hz. The dynamic range in dBc/Hz is calculated from the observed one using $\mathrm{DR}_{\mathrm{RBW}} = \mathrm{DR}_{\mathrm{obs}} + 10\log_{10}(\mathrm{RBW})$. In our case $122\ \mathrm{dB} = 90\ \mathrm{dB} + 10\log_{10}(1600)$. A conventional ΣΔ modulator can only achieve a DR of 114 dB. The SNDR of the frequency synthesizer using the MSLA modulator is calculated at 55.33 dB, while a conventional ΣΔ achieves 49.59 dB.

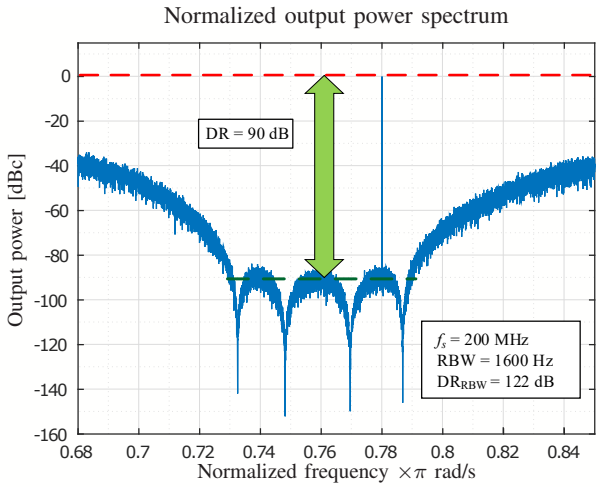

Fig. 5. Normalized power spectrum of 125000 output samples of the MSLA modulator-based frequency synthesizer.

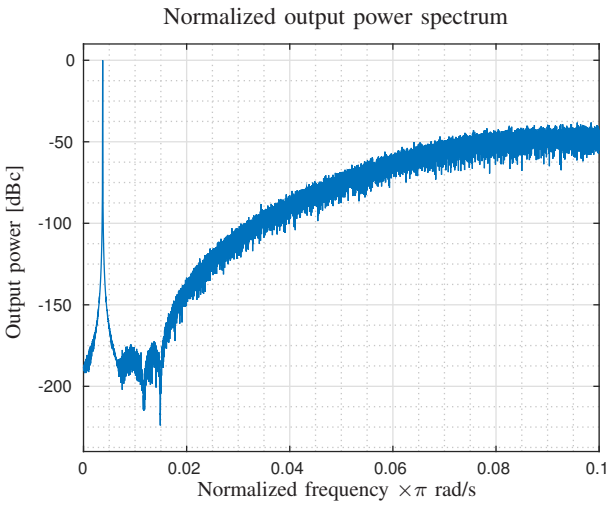

Fig. 6. Normalized power spectrum of 500000 output samples of the low-pass MSLA modulator.

B. 1-bit DAC / Class-D Power Amplifier Driver / 1-bit Bitsream Generator

A MSLA modulator with low-pass characteristics can be used as part of a 1-bit DAC if followed by a low-pass analog filter or directly as the generator of the driving signal of a class-D power amplifier for e.g. audio applications. It can also be used for the generation of the bitstream of a digital microphone or of a SA-CD. As an example we consider a 7-th order low-pass NTF with optimized zeros, out-of-band gain $||\mathrm{NTF}||_\infty = 2$ and oversampling ratio $\mathrm{OSR} = 64$. Assuming audio applications which usually require a sampling rate of 48 KHz. An oversampling ratio of 64 means that the modulator should be able to operate at a sampling rate of $64 \cdot 48$ KHz $= 3.072$ MHz which is easily achievable even for low end hardware. The MSLA modulator is configured with $k = 5$ look-ahead steps, which is a relatively low setting, $r = k$ and $p = 2$.

In Fig. 6 the normalized power spectrum of 500000 output samples of the aforementioned low-pass MSLA modulator is depicted. The input signal is sinusoidal with amplitude $A = 0.35$ and frequency $\omega = 2\pi \cdot 0.0018584$. Notice the very low noise floor in the pass-band, resulting in a $\mathrm{SNDR} = 149.5$ dB. Using the well-known formula $\mathrm{SNDR} = 6.02 \cdot \mathrm{ENOB} + 1.76$ dB [12] for the relation between SNDR and ENOB (effective number of bits) we can calculate an ENOB of 24.5 bits. A conventional ΣΔ modulator can achieve $\mathrm{SNDR} = 136.7$ dB, resulting in an ENOB of 22.4 bits, i.e. 2 bits less conversion accuracy.

IV. Conclusion

The 1-bit MSLA modulator, a variation of conventional 1-bit ΣΔ modulators, which improves their SNDR and stability characteristics while maintaining 1-bit output has been presented. 1-bit output guarantees linearity as there are only two output levels and therefore only gain and offset errors which can be easily corrected. As a digital architecture, all the benefits of digital circuits apply. The design parameters of the MSLA modulator allow for additional fine-tuning of complexity vs. performance. A multitude of possible applications has been described and the performance of the MSLA modulator in these applications has been quantified. The simulation results highlight the performance advantages of the MSLA ΣΔ modulator over 1-bit conventional ones.

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