Hardware Implementation Aspects of Multi-Step Look-Ahead Σ-Δ Modulation-Like Architectures for All-Digital Frequency Synthesis Applications

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***Abstract*—This work discusses hardware implementation considerations for a novel Multi-Step Look-Ahead modulation architecture which improves on the stability and dynamic range of conventional Σ-Δ modulators for all-digital frequency synthesis applications. The basic theoretical concepts of the architecture are analyzed and an appropriate general hardware implementation of the required mathematical operations is presented. It is shown that hardware complexity reduction is possible when noise-shaping filters with convenient coefficients are utilized. Moreover, FPGA and IC implementation examples for a specific noise-shaping filter are given, accompanied by power, area and delay estimations.**

I. Introduction

The rapid advances in deep-submicron CMOS technology combined with the multi-faceted and stringent requirements of modern wireless communications protocols, have resulted in the intensive research of highly integrated all-digital frequency synthesizers. Digital circuits in sub-100nm CMOS technologies exhibit superior characteristics, namely noise and PVT robustness, faster switching times, smaller die footprint etc. compared to the degrading analog devices characteristics such as increased leakage current and lesser degree of scalability.

All-digital frequency synthesis is an ongoing research subject and many of its challenges have not yet been completely resolved [1]. E.g., dithering techniques have been used as a remedy for spurious tones [2], while 1-bit output has been proposed for DAC-less architectures [3]–[5]. Dithering however leads to an elevated noise floor, which makes all-digital frequency synthesis unsuitable for many noise-sensitive applications. Noise shaping using Σ-Δ modulation type techniques may be used to lower the noise floor within a specific frequency band. Yet, noise shaping filters of order higher than two and high input amplitude may result in stability problems of the loop [6]. Increased dynamic range and stability may be achieved, simultaneously, if future inputs and states of the modulator are taken into account when calculating the next output sample.

This work deals with hardware implementation aspects of a new Multi-Step Look-Ahead noise-shaping architecture with single-bit output. Its reconfigurable noise-shaping properties and single-bit output make it an ideal building block for DAC-less low-noise all-digital frequency synthesizers. The theoretical background is analyzed in [7], while a brief overview is presented herein.

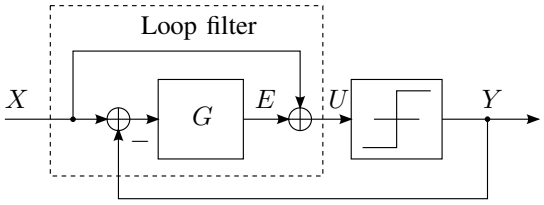

Fig. 1. The error-feedback Σ-Δ modulator topology

The remainder of the paper is organized as follows. Section II presents an overview of the Multi-Step Look-Ahead modulation scheme, setting the path for section III, where a general hardware implementation architecture is introduced. FPGA and IC implementation of a specific MSLA modulator are also discussed. Finally, section IV summarizes the results and investigates further research requirements.

II. Multi-Step Look-Ahead Modulation Overview

The conventional Σ-Δ error-feedback structure (Fig. 1) constitutes the basis of the Multi-Step Look-Ahead (MSLA) modulator. The output is determined by the comparison of the filtered difference between the high resolution input and the single-bit output against the current input. This decision rule is formulated as [8]

$$y_n = \underset{y\in\{\pm 1\}}{\arg\min} |x_n + e_n - y| \tag{1}$$

where y_n is the output, x_n is the input and $e_n = \sum_{i=0}^{n-1}(x_i - y_i)g_{n-i}$ is the filtered error sequence $\{x_i - y_i\}$. Sequence $\{g_i\}$ is the impulse response of the noise-shaping filter G and $g_0 = 0$. The frequency response of the comparison filter G allows the signals in the desired frequency range to pass, while it greatly attenuates out-of-band signals. Thus, the single-bit output tracks the input in the pass-band, pushing the quantization noise out of the signal band. The relation between G and the noise transfer function (NTF) of the modulator is $G(z) = (1 - NTF)/NTF$. A higher order filter allows for better noise attenuation, but given the stability requirements for filters oforder $N > 2$, the available design space for the NTF is greatly reduced.

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This limitation may be overcome when k future inputs of the modulator are taken into account. Then, the modified decision rule is

$$y_n = \underset{v_0\in\{\pm1\}}{\arg\min}\left(\min_{\substack{v_1,v_2,\ldots,v_k\in\\ \{\pm1\}}}\sum_{i=0}^{k}|x_{n+i}+e_{n+i}-v_i|\right) \quad (2)$$

where the arguments $v_0, v_1, \ldots, v_k$ denote all possible future values of the output $y_n, y_{n+1}, \ldots, y_{n+k}$ and k is the number of look-ahead time-instances. If the comparison filter is

$$G(z) = \frac{\sum_{i=1}^{l} b_i z^{-i}}{1+\sum_{i=1}^{m} a_i z^{-i}} \quad (3)$$

then

$$e_{n+j} = \sum_{i=1}^{l} b_i x_{n+j-i} - \sum_{i=1}^{j} b_i v_{j-i} - \\ - \sum_{i=j+1}^{l} b_i y_{n+j-i} - \sum_{i=1}^{m} a_i e_{n-i}, \quad j<l \quad (4a)$$

$$e_{n+j} = \sum_{i=1}^{l} b_i x_{n+j-i} - \sum_{i=1}^{l} b_i v_{j-i} - \sum_{i=1}^{m} a_i e_{n-i}, \; j \geq l \quad (4b)$$

where $0 < j \leq k$.

Through extensive simulations it has been concluded that superior stability and dynamic range is achieved even if only the last term or the two last terms of the sum in (2) are considered, leading to the simplified expression

$$y_n = \underset{v_0\in\{\pm1\}}{\arg\min}\left(\min_{\substack{v_1,v_2,\ldots,v_k\in\\ \{\pm1\}}}|x_{n+k}+e_{n+k}-v_k|\right) \quad (5)$$

where $v_1, v_2, \ldots, v_{k-1}$ are embedded in e_{n+k}.

In [7] it is shown that an equivalent expression for (2) is

$$y_n = \underset{v_0\in\{\pm1\}}{\arg\min}\left(\min_{\substack{v_1,v_2,\ldots,v_k\in\\ \{\pm1\}}}\sum_{j=0}^{k}|A_n^j - \sum_{i=0}^{j} c_i v_{j-i}|\right) \quad (6)$$

where A_n^j is a quantity independent of $v_0, v_1, \ldots, v_k$ and c_i are given by

$$c_i = b_i - \sum_{j=1}^{i-1} a_j c_{i-j} \quad (7)$$

with $c_0 = 1$ and $c_1 = b_1$. Using the same reasoning (5) may be rewritten as

$$y_n = \underset{v_0\in\{\pm1\}}{\arg\min}\left(\min_{\substack{v_1,v_2,\ldots,v_k\in\\ \{\pm1\}}}|A_n^k - \sum_{i=0}^{k} c_i v_{k-i}|\right) \quad (8)$$

In order to evaluate (6) or (8) a proper expression for A_n^j is needed. It turns out that

$$A_n^j = \sum_{i=0}^{j} c_i x_{n+j-i} + \sum_{i=j+1}^{j+l-1} c_i \left(x_{n+j-i} - y_{j-i}\right) + \\ + \sum_{i=0}^{m-1} d_i^j e_{n-i} \quad (9)$$

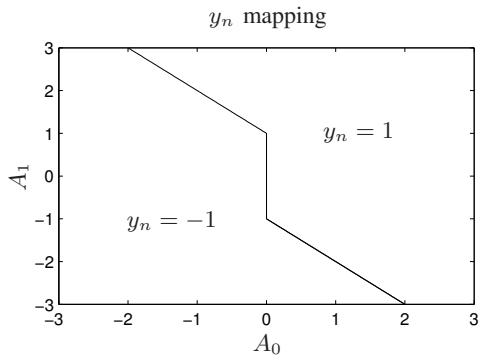

Fig. 2. Mapping regions between $A_n^0, A_n^1, \ldots, A_n^k$ and y_n for NTF $(1-z^{-1})^2$ and $k=1$

where d_i^j are coefficients depending on the filter coefficients a_i, l is the order of the numerator of the comparison filter G and m is the order of the denominator. Finally, e_n is calculated by the difference equation implied by the comparison filter

$$e_n = \sum_{i=1}^{l} b_i \left(x_{n-i} - y_{n-i}\right) - \sum_{i=1}^{m} a_i e_{n-i} \quad (10)$$

III. Hardware Implementation of the Multi-Step Look-Ahead Modulator

A. Reconfigurable Hardware Implementation Architecture

From the analysis of the previous section it should be clear that a hardware implementation of the MSLA modulator should evaluate (6) or (8). The output of the modulator y_n is a function of $A_n^0, A_n^1, \ldots, A_n^k$. It can be shown that the optimization problem (6) can be transformed into the problem of simultaneously satisfying a number of linear inequalities. Based on that, a decomposition of the hardware required for deriving the solution, whilst maintaining low complexity, is achievable. The solution may be as simple as the sign of A_n^k for special cases of (8), effectively transforming the MSLA into an equivalent conventional Σ-Δ modulator with a different, stable, NTF than the one that we started with. This is the case for the NTF $(1-z^{-1})^3$ and $k=2$. Another example of the mapping between $A_n^0, A_n^1, \ldots, A_n^k$ and y_n is depicted in Fig. 2 for NTF $(1-z^{-1})^2$ and $k=1$. Similar mappings in higher dimensions are obtained for more sum terms in (6), while different filters change the mapping region boundaries.

The calculation of A_n^j is based on (9). The coefficients c_i and d_i^j are precalculated based on the comparison filter coefficients, while $k+l-1$ previous values of the high resolution input, $l-1$ previous values of the single-bit output and $m-1$ previous values of e_n should be stored in memory elements. The proposed architecture for the computation of A_n^j is shown in Fig. 3. It consists of an IIR filter for the calculation of e_n, three multiply and accumulate (MAC) units for the computation of the three sums in (9) and three adders. The memory units and the clock signals have been omitted in the figure for clarity. This is the building block of the MSLA modulator. For the evaluation of (8), one A_n^k computation

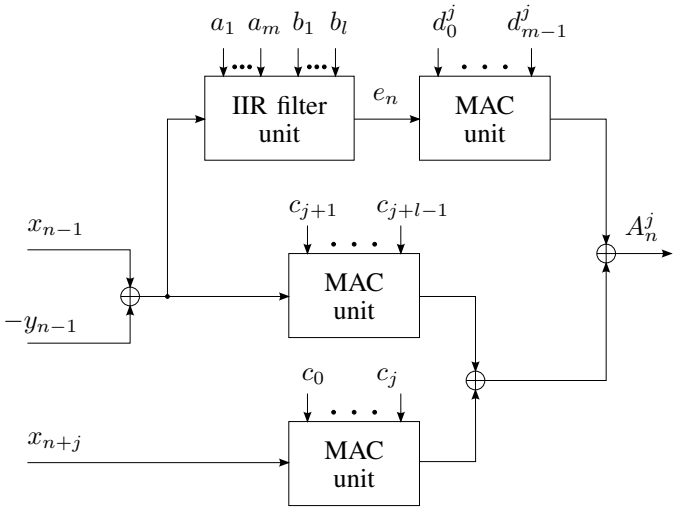

Fig. 3. A_n^j computation unit

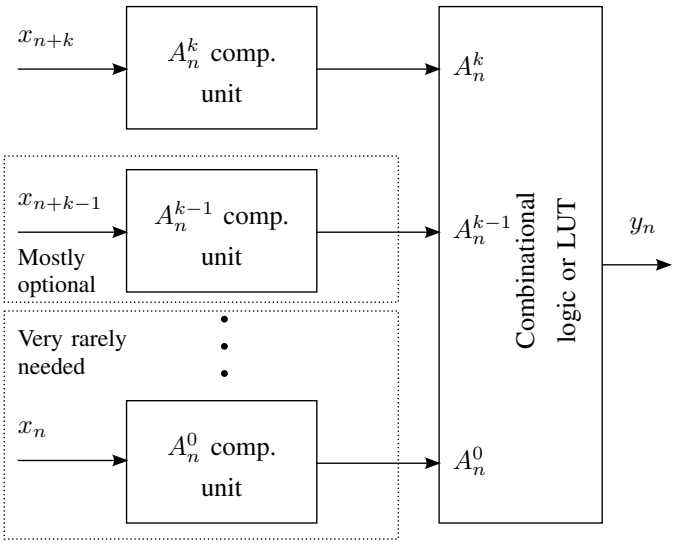

Fig. 4. Multi-Step Look-Ahead modulator hardware implementation architecture

block and additional combinational logic for the derivation of y_n from A_n^k is sufficient for a working modulator. As many as $k+1$ A_n^j computation units can be utilized in parallel in order to evaluate (6), but thorough simulations have shown that no more than one or two units in parallel for the computation of A_n^k and A_n^{k-1} are needed in the vast majority of cases. The complete MSLA modulator system is depicted in Fig. 4. The complexity of each A_n^j computation module increases with j as more multiply and accumulate operations are needed due to the increase in the number of terms of each sum in (9).

This MSLA modulator hardware implementation architecture is highly reconfigurable, since in order to accomodate for a different signal frequency band, only the coefficients have to be changed for a specific value of k. Real-time operation of the proposed digital circuit for moderate values of k is possible even if it is implemented in a low-end FPGA. Further reduction in hardware complexity and increase in maximum clock frequency is possible if the filter coefficients are simple enough, e.g. powers of two or a sum of powers of two, so that hardware multiplication units are replaced by an adder in combination with a shift operation.

B. FPGA Implementation Results

As a test-case, the MSLA modulator was implemented in a low-end Xilinx Spartan 3E Starter Board. A multiplier-less low-pass modulator design was chosen with $NTF = (1 - z^{-1})^3$. The FPGA implements (8) with $k = 2$. With this value of k, stability is maintained for a maximum sinusoidal input amplitude $A = 0.61$. The design was optimized for speed and operates with a maximum clock frequency of 142 MHz. The high-level synthesis tool reports 16 16-bit adders and 242 flip-flops for the entire design. This accounts for just 1% utilization of the total FPGA resources.

This test-case implementation demonstrates the MSLA modulator's suitability for FPGA device implementations. Its hardware requirements are minimal even for a low-end FPGA, meaning that implementations for higher values of k and for higher order comparison filters are well within the capabilities of low-end FPGA devices.

C. Standard 65nm CMOS Physical Design

The MSLA modulator with the characteristics of the previous subsection has also been implemented in a standard 65nm CMOS technology with 1.0V supply voltage. The EDA tools utilized in the design flow are the industry standard Cadence® Encounter® RTL Compiler (Synthesis) and the Cadence® Encounter® Digital Implementation (EDI) System (Place & Route). The structural netlist of the modulator consists of 540 standard cells, taking up a total area of 4,695 μm^2 with an estimated power consumption of 1.724 mW at clock frequency 400 MHz. The layout of the IC physical design is shown in Fig. 5. Aiming at the highest possible operating clock frequency using standard cells, a maximum clock frequency of 850 MHz was achieved, while the synthesized circuit occupied an area of 4,697 μm^2 with an estimated power consumption of 3.394 mW.

The hardware implementation in a common IC technology exhibits the low-power and small area characteristics of the MSLA modulator. This means that an MSLA module may easily be integrated as part of a larger design with minimal area and power overhead. Of course, as it is an all-digital design, it will benefit from any reduction in the scale of integration.

IV. Conclusions and Future Investigations

In the previous sections a hardware implementation architecture for the MSLA was proposed, along with various proposals for the reduction of the required hardware, such as the careful selection of the comparison filter in order to avoid multipliers. The MSLA modulator exhibits high order noise-shaping properties with low hardware complexity and high operating frequency, rendering it ideal for all-digital frequency synthesis applications.

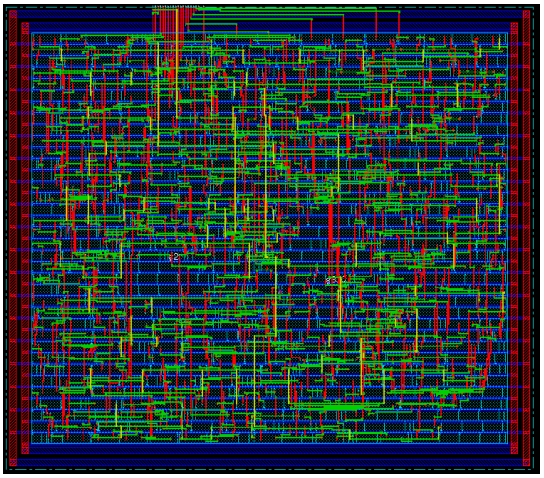

Fig. 5. MSLA standard 65nm CMOS layout

Many design aspects require further investigation and we are currently working on several techniques to make the design faster and more energy efficient. Significant improvements are expected from the bit-width optimization of each basic component of the MSLA hardware architecture, as well as from more advanced pipelining and parallelization of the required arithmetic operations. Finally, more comparison filters with a wide range of different orders and frequency characteristics need to be tested and implemented.

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