# A Mathematical Model for Time-Domain Analysis and for Parametric Optimization of a Class of Switched Capacitor RF Power Amplifiers

Panagiotis G. Zarkos[1], Christos G. Adamopoulos[1], Iason Vassiliou[2] and Paul P. Sotiriadis[1]
[1] Electrical & Computer Engineering, National Technical University of Athens, Greece
[2] Broadcom, Athens, Greece
Email: pps@ieee.org

***Abstract*—State-space modeling and analysis of a class of switched capacitor RF power amplifiers are introduced resulting in fast and accurate calculation of the output and supply-drawn power as well as of the voltage and current waveforms. Power derivation parameterized on component values and intermediate transformed impedances offers a tool for optimizing the switched capacitor RF power amplifier for maximum output power or maximum Power Added Efficiency. The accuracy of the derived results is verified with SPECTRE (Cadence) simulation.**

***Keywords—Matching network; polar modulation; power added efficiency; power amplifier; state-space; switched-capacitor circuit***

## I. INTRODUCTION

A great deal of research has been carried out recently in the field of RF power amplifiers for WLAN and cellular applications. Most modulation schemes employ non-constant envelope signals with high Peak to Average Ratio (PAR). The need to trade-off high efficiency with linearity in systems using such modulation schemes is a major challenge. A popular choice is to use a linearization technique such as Envelope Elimination and Restoration (EER), Envelope Tracking (ET), out-phasing, Pulse-width modulation (PWM) etc. [1]-[3]. All of the aforementioned techniques have shown significant results. Nevertheless, several drawbacks degrade their performance, such as the reduced overall efficiency observed in EER and the pulse swallowing effect in PWM.

Digital PA architectures using unit-cell PAs are considered in order to meet efficiency and linearity specifications [4]. The class of Switched-Capacitor (RF) PAs (SCPA) examined in this work is a case of digital PAs offering numerous advantages. To the best of our knowledge, it was introduced in [5], [6]. The core of the SCPA is formed of $N$ capacitors, a number of which (say $n$) are being switched between $V_{dd}$ and ground at the RF carrier frequency; the rest $N$-$n$ of them are connected permanently to ground. The choice of the ones being switched depends on the codeword applied at the input [5]. In the simplest case, all capacitors are of the same size, $C$ as shown in Fig. 1. Here we assume that the first $n$ capacitors are selected to switch and the last $N$-$n$ are held grounded.

Some of the advantages of SCPA are the high accuracy owing to the precise value of the ratios between capacitors that can be achieved in CMOS technology, the flexibility of scaling for higher resolution applications (e.g. from WLAN to WiMAX) and the fact that its performance is improved when the devices are scaled down. However, the low operating supply voltage due to technology down-scaling makes it difficult to achieve high output power levels. One solution is to use large impedance transformation ratio, which usually requires large die area and suffers from the significant resistive losses of the inductors in the matching network. A transformer-based power-combining method addresses this challenge [7]. Also, a cascode switching scheme can allow for higher power supply voltage and output power [5].

This work introduces a rigorous mathematical approach for the analysis of the SCPA, currently missing in the literature. Specifically, a state space analysis of the equivalent circuit of the switched capacitor PA is presented in Section II. Section III gives an estimation of the output power and supply power by determining the fundamental harmonic content of the voltage over the load resistance and the current drawn from the power supply. The accuracy of the derived results is demonstrated in Section IV where they are compared to SPECTRE (Cadence) simulation.

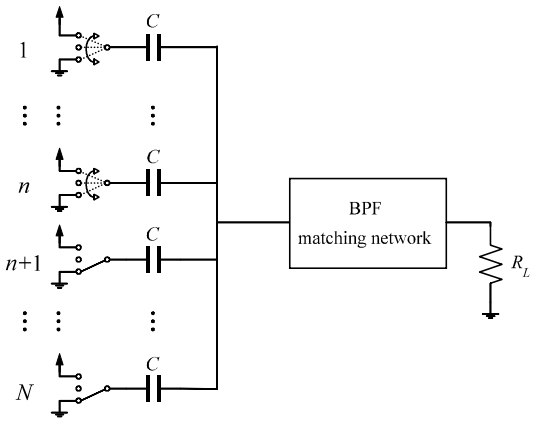


Fig. 1. $N$-path SCPA with $n$ selected caps switching between $V_{dd}$ and ground.

Described work was partially supported by Broadcom Foundation USA.

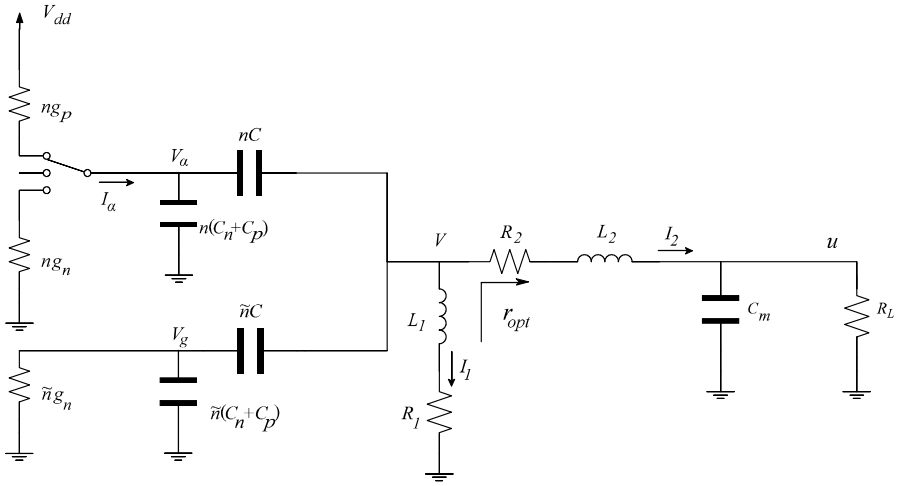


Fig. 2. Simplified model of the SCPA

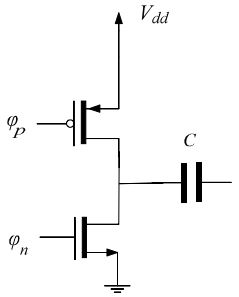


Fig. 3. CMOS switch used in the SCPA cell with non-overlapping clocks $\varphi_n$, $\varphi_p$.

## II. STATE-SPACE MODELING OF THE SC PA

In this section we use state-space analysis to model the time-domain behavior of the SCPA. The model circuit is shown in Fig. 2. It models a SCPA formed of $N$ identical capacitors, first $n$ of which are being switched between $V_{dd}$ and ground at the RF carrier frequency; and $N$-$n$ are held grounded. The switches are implemented by NMOS-PMOS pairs (Fig. 3) which are modeled approximately by equivalent conductances $g_n$ and $g_p$, respectively, since they operate in an on-off fashion. This approximation is essential for getting a tractable model amenable to analytical solutions without compromising much the accuracy of the results.

Conductances $g_n$ and $g_p$ are in parallel with parasitic capacitances, noted $C_n$, $C_p$, of the NMOS and PMOS switches respectively. Since $V_a$ is periodic the power consumption from $V_{dd}$ is the same whether $C_p$ is connected to $V_{dd}$ or ground. This explains why we chose to consider it grounded in Fig. 2.

The switching capacitors are denoted by $C$ in both figures. Inductor $L_1$ is used to tune the total capacitance $NC$ while inductor $L_2$ and capacitor $C_m$ compose the low-pass matching network employed for the impedance transformation and the suppression of harmonics. Resistors $R_1$ and $R_2$ model the finite $Q$ of inductors $L_1$, $L_2$. The load of the antenna and the optimally transformed resistance (the resistance observed right-wise between the left side of $R_2$ and ground) are $R_L$ and $r_{opt}$ respectively. The notation $g_L \equiv 1/R_L$ is also used.

It is strongly recommended to drive the gates of the CMOS switches with *non*-overlapping clocks [5]. This eliminates the crowbar currents that flow from the power supply to ground during switching transitions. This non-overlapping pulsed operation of the switches can be modeled as a tri-state switch with three possible positions: *Up*, *Down* and *Open*. During the *Up* phase the left (bottom) plate of the first $n$ capacitors $C$, selected to switch, is connected via a PMOS switch to $V_{dd}$, while during the *Down* phase it is similarly connected to ground. The two *Open* phases correspond to the time of the period (of the RF carrier) that both switches are open. The first one occurs when the PMOS switch has been turned OFF and the NMOS switch hasn't turned ON yet, while the second one occurs in the opposite transition. All of the above are shown in the timing diagram of Fig. 4 where the duty cycle $D$ is defined as the ratio of the time that the NMOS or PMOS switch is ON to the time duration of half a period, T/2. In the rest of our analysis it is assumed that the pulses of the clock(s) $\varphi_n$, $\varphi_p$ have sharp edges and the transitions are instantaneous.

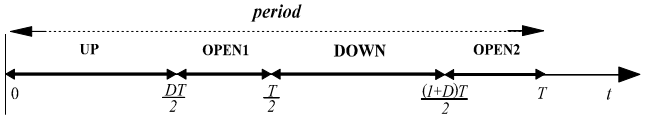


Fig. 4. Timing diagram depicting the up, down and open phases

Writing the Kirchhoff's equations for the equivalent circuit in Fig. 2 and setting $\tilde{n} = N - n$ we have:

$$V_a:\ -I_a + n\left(C_n + C_p\right)\dot{V}_a + nC\left(\dot{V}_a - \dot{V}\right) = 0 \tag{1}$$

$$V_g:\ \tilde{n}g_n V_g + \tilde{n}\left(C_p + C_n\right)\dot{V}_g + \tilde{n}C\left(\dot{V}_g - \dot{V}\right) = 0 \tag{2}$$

$$V:\ nC\left(\dot{V} - \dot{V}_a\right) + \tilde{n}C\left(\dot{V} - \dot{V}_g\right) + I_1 + I_2 = 0 \tag{3}$$

$$u:\ C_m\dot{u} + \frac{u}{R_L} = I_2 \tag{4}$$

$$I_1:\ V = R_1 I_1 + L_1\dot{I}_1 \tag{5}$$

$$I_2:\ V = u + R_2 I_2 + L_2\dot{I}_2 \tag{6}$$

Note that current $I_a$ (Fig. 2) can take one of the following three forms during the different phases of the circuit

$$\begin{aligned} I_a &= ng_p(V_{dd} - V_a) \quad &:\ &Up\ phase \\ I_a &= 0 \quad &:\ &Open\ phase \\ I_a &= -ng_n V_a \quad &:\ &Down\ phase \end{aligned} \tag{7}$$

Defining the state vector $x = [V_a, V_g, V, u, I_1, I_2]^T$ we write Eqs. (1)-(7) in the standard differential-equation matrix form of linear systems $\dot{x} = A_k x + b_k$. (Here index $k$ indicates the form of matrices $A$ and $b$ during the different phases).

TABLE I. THE DIFFERENTIAL EQUATIONS AND INITIAL CONDITIONS GOVERNING EACH OF THE FOUR OPERATING PHASES DURING A PERIOD T

| Phase | Time Period | Initial Condition | Equation |
|---|---|---|---|
| *Up*: | $\left[0, \frac{DT}{2}\right)$ | $x_0$ | $\dot{x} = A_u x + b_u$ |
| *Open* 1: | $\left[\frac{DT}{2}, \frac{T}{2}\right)$ | $x_1$ | $\dot{x} = A_o x$ |
| *Down*: | $\left[\frac{T}{2}, \frac{(1+D)T}{2}\right)$ | $x_2$ | $\dot{x} = A_d x$ |
| *Open* 2: | $\left[\frac{(1+D)T}{2}, T\right)$ | $x_3$ | $\dot{x} = A_o x$ |

Note that the matrix differential equation $\dot{x} = A_k x + b_k$ has different initial conditions and coefficient matrices $A_k$, $b_k$ during each phase of the period. This is due to the different expressions, see Eq. (7), of current $I_a$ during the four phases. The equations obtained are grouped in Table I.

The solution of the matrix differential equations in Table I are expressed using the exponential matrix $e^{A_k t}$ and the initial conditions [8]. The initial conditions are derived from the continuity requirement of the state-space variables as well as the periodic nature of the steady-state solution which demands that the state vector at the end of the period $T$ is equal to $x_0$.

## III. OUTPUT AND SUPPLY POWER

Although the matching network filters the signal to the output, $u$ may contain some harmonics as well. The desirable output power is that of the fundamental harmonic of $u$, which we derive in this Section along with the period-average power drawn from the power supply. Using the solution of the state-space equation for each phase, an expression for the amplitude $U_1$ of the fundamental harmonic of $u$ is found as a function of the state-space matrices and initial conditions of the previous section. Evaluating $U_1$ as a function of the termination resistance, an optimum value of $r_{opt}$ is found. Moreover, the power drawn from the supply can be found by determining current $I_a$ flowing through the ON resistance of the PMOS transistor during the *Up* phase. The results of this analysis are compared to those obtained from SPECTRE.

We define the scalar integrals of the fundamental harmonic of the output voltage, $u$,

$$J_{ck} = \frac{2}{T}\int_{t_{ik}}^{t_{fk}} e_4^T x_k(t)\cos(\omega_o t)\,\mathrm{d}t, \quad J_{sk} = \frac{2}{T}\int_{t_{ik}}^{t_{fk}} e_4^T x_k(t)\sin(\omega_o t)\,\mathrm{d}t \quad (8)$$

where, $e_4^T = [0 \;\; 0 \;\; 0 \;\; 1 \;\; 0 \;\; 0]$, $x_k(t)$ is the state-space solution of phase $k$ ($k$ = *Up*, *Open* 1, *Down*, *Open* 2), and $t_{ik}$, $t_{fk}$ are phase's time-boundaries. Then, the amplitude of the fundamental component of $u$ is $U_1 = \sqrt{\left(\sum_k J_{ck}\right)^2 + \left(\sum_k J_{sk}\right)^2}$. Finally, the output (RMS) power of the amplifier is given by:

$$P_{out} = U_1^2 / (2R_L) \quad (9)$$

To evaluate the efficiency of the amplifier, the power drawn from the supply, $P_s$, is determined using

$$P_s = \frac{1}{T}\int_{up} V_{dd} I_a(t)dt = \frac{ng_p}{2} DV_{dd}^2 - \frac{1}{T} ng_p e_1^T \times \times \left[ A_u^{-1}(e^{A_u \frac{TD}{2}} - I)x_0 + A_u^{-2}(e^{A_u \frac{TD}{2}} - I)\mathrm{b}_u - \frac{TD}{2} A_u^{-1} b_u \right] \quad (10)$$

## IV. SIMULATION RESULTS AND DESIGN GUIDELINES

### A. Time-domain Waveforms Comparison

The waveforms of voltages and currents of the SCPA's simplified model in Fig. 2 are derived via the solution of the state-space differential equations with their initial conditions in Table I. To verify the accuracy of the model, the waveforms are compared to the ones derived via SPECTRE simulation of the SCPA, specifically, with Periodic Steady-State simulation.

This comparison is made in Fig. 5 for $n$ = 24 and $N$ = 63. Although there is some difference at the beginning of the *Up* and *Down* phases, due to the $C_{gd}$ capacitors, which we have ignored in the model of Fig. 2, this difference does not impact significantly the output and supply power we are interested in, as demonstrated in the following subsection.

### B. Output and Supply power Comparative Results

Following the analysis in Section III we have derived the output and supply power, (9), (10) as functions of parameter $n$. We use them to calculate the Power Added Efficiency (PAE), $PAE = P_{out} / P_s$, of the SCPA. Figs. 6-8 show that the estimated output and supply power, and PAE, are good approximations of the ones derived via SPECTRE simulation of the actual SCPA.

### C. Design Guidelines and Optimization of the SCPA

Our goal is to select the values of the component parameters in order to optimize the performance of the circuit in terms of output power and PAE.

First we consider the values of transistors' parameters $r_{on}$, $C_n$ and $C_p$. Apparently, $r_{on}$ should be rather small compared to $r_{opt}$ to avoid significant power loss on the switches. On the other hand, the transistors should not be too large because this results in large parasitic capacitances $C_n$ and $C_p$ as well. Here we designed the transistors to have $r_{on}$= 7Ω, a value verified

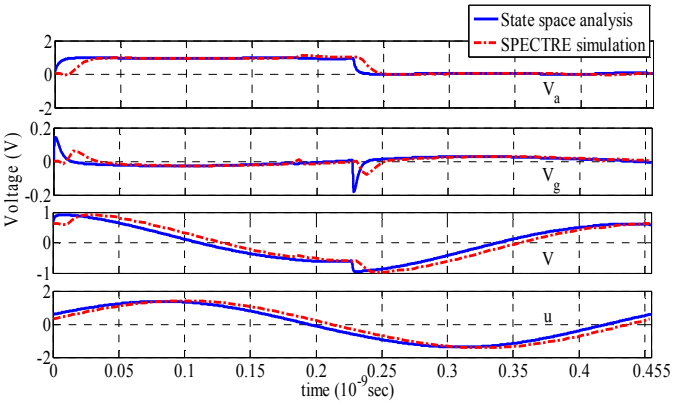


Fig. 5. Waveforms of state variables from the state-space analysis of the SCPA's simplified model in Fig. 2 and SPECTRE simulation of the SCPA, for $n$ = 24 and $N$ = 63.

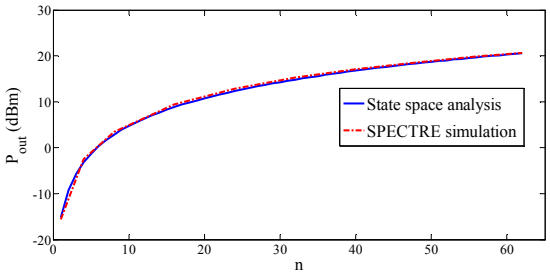


Fig.6. $P_{out}$ derived using the analytical approach of section III and SPECTRE.

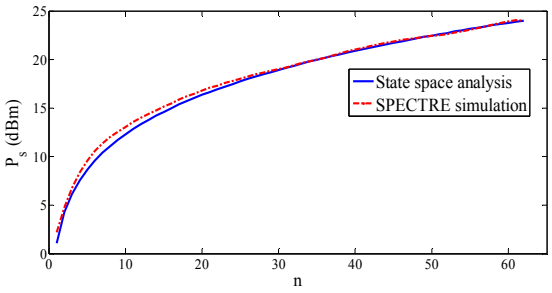


Fig. 7. $P_s$ derived using the analytical approach of section III and SPECTRE.

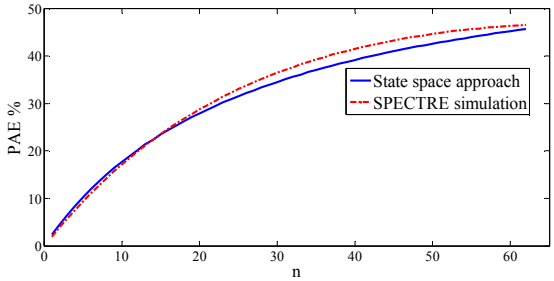


Fig. 8. PAE derived using the analytical approach of section III and SPECTRE.

using SPECTRE simulation. Moreover $C_n$ and $C_p$ turned to be negligible compared to our choice of $C = 500\,fF$, a value which was recommended in [5], [6] for this SCPA.

Next we selected inductor $L_1$ to resonate with the whole array of the switching caps $NC$, $(N = 63)$ at the carrier frequency, here assumed 2.2GHz [5], [6], so that maximum output power is achieved and higher order harmonics are filtered.

When the values of $R_L$ and $r_{opt}$ have been determined and the quality factors $Q$ of inductors $L_1$, $L_2$ are known, implying $R_{1,2} = \omega_0 L_{1,2} / Q_{1,2}$, then $C_m$ and $L_2$ of the matching network are given by $C_m = \left[1 + \sqrt{1 + 4Q_2^2 r_{opt}(R_L - r_{opt})/R_L^2}\right] / \left(2Q_2 r_{opt}\omega_0\right)$ and $L_2 = Q_2 r_{opt} R_L C_m / \left(Q_2 + \omega_0 R_L C_m\right)$ respectively. In our simulations, we assumed $Q \approx 10$ and $R_L$=50Ω while $r_{opt}$ was an optimizing parameter of the circuit.

Based on the choices above and using the theoretical development in Section III, we derived PAE, supply power and output power parameterized on $r_{opt}$ where $r_{opt}$<$R_L$. The results are plotted in Fig. 9. It is seen that *maximum output power* is achieved for $r_{opt} = 19\Omega$ independently of the value of

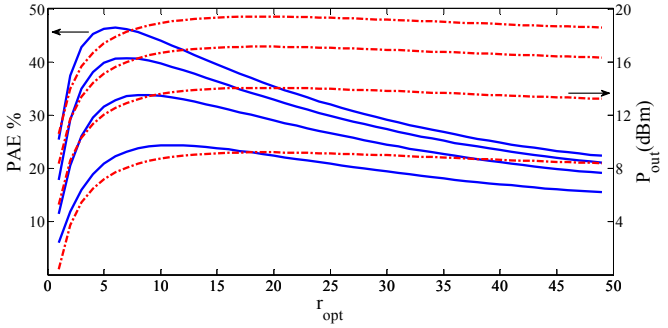


Fig. 9. Analytical PAE vs $r_{opt}$ and $P_{out}$ vs $r_{opt}$ for $n$=16, 28, 40, 52. Solid lines correspond to PAE and dashed lines to $P_{out}$.

parameter $n$. It is not the same for PAE however whose maximizing $r_{opt}$ value depends on parameter $n$ and therefore choosing the best $r_{opt}$ depends on the statistical properties of parameter $n$ and therefore the *modulation scheme* used for the signal transmitted by the SCPA.

## V. Conclusion

State-space modeling and analysis of a class of switched capacitor RF power amplifiers allowed us to derive the output and supply-drawn power of the amplifiers parametrically on the values of components and intermediate impedances, and, optimize for output power and power-added efficiency. It is shown that output power optimization is independent of the relative signal strength whereas power-added efficiency depends on the signals' statistical properties and therefore the modulation scheme.

## References


[1] P. Reynaert and M. S. J. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," IEEE J. Solid-State Circuits, vol. 40, pp. 2598-2608, Dec. 2005.

[2] H. Xu, Y. Palaskas, A. Ravi, and K. Soumyanath, "A highly linear 25 dBm outphasing power ampli• er in 32 nm CMOS for WLAN application," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, 2010, pp.306–309.

[3] J. S. Walling, H. Lakdawala, Y. Palaskas, A. Ravi, O. Degani, K.Soumyanath, and D. J. Allstot, "A class-E PA with pulse-width and pulse-position modulation in 65 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 6, pp. 1668–1678, Jun. 2009.

[4] P. Cruise, C.-M. Hung, R. B. Staszewski, O. Eliezer, S. Rezeq, K. Maggio, and D. Leipold, "A digital-to-RF-amplitude converter for GSM/GPRS/EDGE in 90-nm digital CMOS," in Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp., 2005, pp. 21–24.

[5] S. Yoo, J. Walling, E. Woo, B. Jann, and D. Allstot, "A switched capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no.1, pp. 1–11, Jan. 2011.

[6] S. Yoo, J. S. Walling, E. C. Woo, and D. J. Allstot, "A switched-capacitor power amplifier for EER/polar transmitters," in *Proc. IEEE Int. Solid State Circuits Conf.*, San Fransisco,, CA, 2011, pp. 428–430.

[7] S.-M. Yoo, J. S. Walling, E.-C. Woo, and D. J. Allstot, "A power combined switched-capacitor power amplifier in 90 nm CMOS," in *IEEE RFIC Symp.*, Jun. 2011, pp. 1–4.

[8] Dorf R., Bishop R. Modern control systems [M]. 11th ed., Upper Saddle River, NJ, USA: Prentice Hall, 2008.