Delta-Sigma Modulation Techniques to Reduce noise and Spurs in All-Digital RF Transmitters

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***Abstract*—This paper proposes a compact RF all-digital transmitter that is based on a direct digital synthesizer topology combined with Sigma-Delta modulation and other digital techniques to produce a spurs-free, high-frequency, single or few bit output with improved noise floor performance.**

***Keywords*—DDS; S/D modulator; MASH; Dithering; RF communications; Frequency synthesis**

I. Introduction

During the past few years there has been an increasing interest in replacing large, power demanding, analog intensive RF blocks with digital alternatives. This has resulted in the development of digitally intensive transmitters using a Direct Digital Synthesizer (DDS) or an All-Digital PLL as their basis to generate the desirable modulated output signal.

The proposed architecture belongs to the first class. It uses a DDS with an appropriate phase-dithering combined with a S/D modulator to allow for single-bit output (or otherwise few-bits signal representation) while maintaining a spurs-free output with low noise-floor, as well as, with a digital synchronous up-converter to reach frequencies up to (or even higher if one uses the harmonics) that of the clock. The architecture has direct capability for phase, frequency and amplitude modulation.

The DDS [1], [2] (Fig. 1) is composed of an n-bit Phase Accumulator (PhA), followed by a phase-to-amplitude conversion stage implemented by a Look Up Table (LUT), which is typically filled with one period of the *Sine* function. The m-bit digital output of the LUT is converted to an analog output signal by the Digital to Analog Converter (DAC). The DDS operates at clock frequency f_{clk} and is controlled by the frequency control word (FCW), w. Its output is a fractional division of f_{clk} and its output frequency is given by:

$$f_{out} = \frac{w}{2^n} \cdot f_{clk} \quad \text{with} \quad 0 < w < 2^{n-1}.$$

To achieve frequency division with high resolution, the PhA typically has a large size n between 16 and 64 Bits. A phase dithering stage is used after the PhA in most practical implementations [3]. This allows to keep only a fraction of those bits (the MSBs) for the address input of the LUT. As a result, the overall size of the circuit is reduced, while the output remains spurs-free.

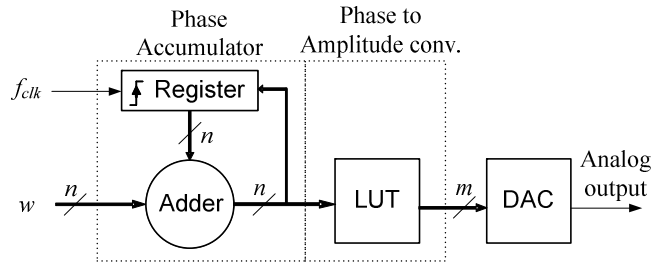

Fig. 1. Basic form of a Direct Digital Synthesizer (DDS).

One of the main drawbacks of the DDS, and the only analog part of it, is the DAC which generates the final output. In our previous work [4], we have shown that it is possible to completely eliminate the LUT and the DAC and still have a spurs-free output by only keeping the MSB of a properly phase dithered PhA as the final output. This technique results into a compact and minimalistic purely digital synthesizer, but it has an elevated noise floor due to the extensive use of dithering.

Another approach is to replace the DAC with a digitally implemented 1-bit or few bit output S/D Modulator (SDM). By doing so, the synthesizer can achieve a lower noise floor level, as the quantization noise is shaped away from the generated signal in the frequency domain. The main limitations of these techniques are that they are suitable only for lower-frequency generated signals and their demanding area - power requirements as they need large digital blocks (multipliers).

This paper proposes a compact RF DDS topology that combines Sigma-Delta modulation with dithering and other digital techniques to produce a spurs-free high-frequency single or few bit output and improved noise floor performance in comparison to similar all-digital techniques. Also, this topology, being DDS based and through the S/D block, can directly support any desirable modulation scheme [5] including FSK, PSK and QAM.

II. PROPOSED ARCHITECTURE

The proposed architecture consists of three parts, a Phase Dithered DDS based carrier generator, a digitally implemented low-pass S/D modulator and a digital synchronous up-converter.

A. Carrier generator

A DDS based carrier generator (as shown in Fig. 2) is used. Phase dithering is utilized and only the *t*-MSBs are kept to drive the *Sine* table. A small LUT with *t* as low as 6-bits and *m* equal to 10-bits is actually sufficient for our targeted noise floor level. Dithering enables a spurs-free output even in this minimalistic case.

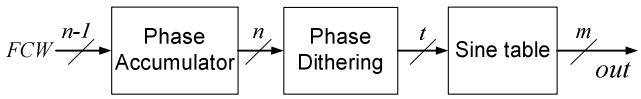

Fig. 2. Proposed Direct Digital Synthesizer (DDS) block diagram.

The output then drives the S/D modulator. The effects of dithering on single- and multi-stage S/D modulators have been investigated in [6], where it is shown that a two-stage modulator is sufficient to make the quantization noise asymptotically white.

B. S/D modulator

A S/D modulator operates as a quantizer and noise shaper, pushing the quantization noise away, in the frequency domain, from the desirable operating frequency range. Most commonly, S/D modulators are low-pass, passing low frequency signals with minimum distortion and pushing the quantization noise to the higher frequencies.

A 1st order low-pass S/D modulator can be digitally implemented using a simple accumulator. Its 1-bit output is given by the overflow signal. The 1st order modulator does not suffer the instability issues of its higher-order counterparts, but inserts many undesirable spurs in its generated signal. This issue can be solved by increasing the strength of the phase dither of the carrier generator. Typically, however, higher-order modulators (Fig. 3) are used in order to exploit their superior noise suppression and lower spur insertion. As previously stated though, they are inherently unstable, due to the non-linear characteristics of the quantizer and the behavior of their high-order loop filters.

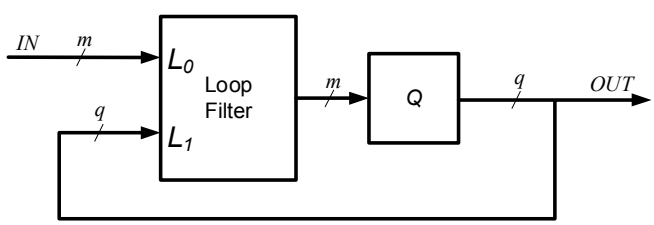

Fig. 3. A general single-quantizer digital S/D modulator [7], where L_0 and L_1 are digital filter transfer functions and *m* and *q* are the number of bits of the input and the quantizer output respectively.

A cascade of multiple 1st order modulators in consecutive stages, where the input of each stage is the quantization error of the previous one, combines the advantages of both 1st and higher-order modulators. This topology is called Multi-Stage-Noise-Shaping or MASH (Fig. 4). The MASH topology has an output of *m*-bits, where *m* is equal to the order of the synthesizer. There are other high-order topologies which can produce a 1-bit output, but they are typically significantly larger and most of them have problems with undesirable spurs in their outputs. So, for this architecture we selected the simplistic MASH topology. Many works have proposed digital S/D modulators employing dithering techniques to suppress spurious tones [8]-[10], but the resulting circuits are too complicated for our minimalistic approach.

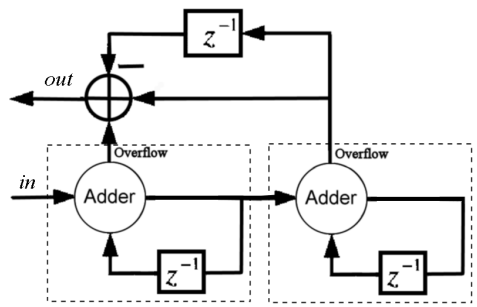

Fig. 4. A second order digital S/D MASH modulator.

The output of the MASH modulator is fed into a digital synchronous up-converter to produce the final output.

C. Digital synchronous up-converter.

The up-conversion is implemented by mixing the MASH modulator output with the $f_{clk}/2$ signal. This is done digitally by multiplying the two signals and then retiming the output using f_{clk} clocked flip-flops. By doing so, the output of the MASH modulator is flipped in the [0, f_{clk} /2] frequency range. This way, the benefits of the simple low-pass S/D modulator are transferred to the high-frequency range.

The $f_{clk}/2$ signal sampled with f_{clk} rate can take only two values constantly repeating each other, 1 and -1 (represented digitally by 0 and 1). Multiplying this signal with any f_{clk} sampled signal results into simply inverting the sign of the sampled signal every second sample. This is implemented digitally just by applying the XOR operator on every bit of the MASH modulator output with the $f_{clk}/2$ signal.

The complete proposed architecture is shown in (Fig. 5). All the blocks are operating using the same single-phase clock signal f_{clk}.

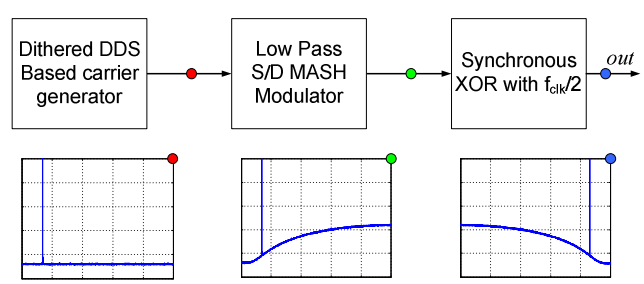

Fig. 5. The proposed synthesizer architecture. Red: Carrier generated, Green: Low-pass quantized signal, Blue: Up-converted final output.

III. RESULTS

Comparative measurements between the 1-bit dithered DDS of [4] and the proposed architecture using a 1st, 2nd and 3rd order MASH with an f_{clk} of 10Mhz are presented in **Error! Reference source not found.**. The synthesizer of [4] has a flat noise floor at 69.5dBc/Hz.

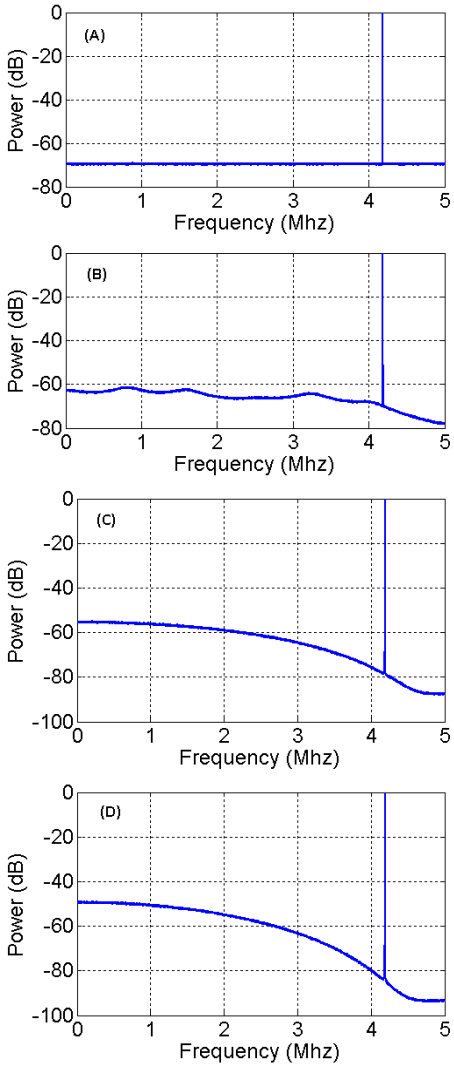

Fig. 6. Comparative measurements using f_{clk} = 10Mhz. (A) 1-bit dithered DDS described in [4], The proposed architecture: (B) using a 1st order MASH, (C) using a 2nd order MASH, (D) using a 3rd order MASH.

The 1st order one barely manages to outperform [4] when generating frequencies in the $[0.8*f_{clk}/2, f_{clk}/2]$ range.

It should be noted that the 2nd order MASH modulator has a 2-bit output and the 3rd order one has a 3-bit output. An equivalent DAC based DDS with a 2-bit output would perform at ~75.5dBc/Hz and the 3-bit one at ~81.5dBc/Hz. The 2nd order one improves this performance by at least 3dB in the $[0.8*f_{clk}/2, f_{clk}/2]$ range, while the 3rd order one improves it by another 2.5dBc.

Based on these results, the 2nd order MASH DDS offers the best balance in terms of performance, silicon area and power consumption. This topology is not larger than two times the size of the 1-bit dithered DDS described in [4]. Moreover, the 2-bit output (taking values 00, 01, 10, 11) can be converted into a 3-bit thermometer coded digital output (000, 001, 011, 111), which can be easily translated to an analog signal by combining the three signals to a common output node using identical sized resistors, thus eliminating the DAC and offering a nearly all-digital solution.

IV. CONCLUSION

This work has proposed a minimalistic Direct Digital Synthesizer (DDS) architecture, which improves the performance of [4] in the frequency range $[0.8*f_{clk}/2, f_{clk}/2]$ by employing a multi-stage S/D modulator in order to shape the quantization noise out of the signal band. It was shown that efficient and spurs-free all-digital frequency synthesis is possible with very small silicon area requirements. The advances in digital circuit technology in terms of speed, combined with the simplicity of the proposed circuit design, mean that very high synthesized frequencies can potentially be achieved. Furthermore, with minor modifications, modulated signals can be generated and the modified circuit may be used as a digital transmitter.

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