Switching Down-Converting RF Mixer with Embedded Single-Bit-Output All-Digital Frequency Synthesizer

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***Abstract*—An RF switching down-converting mixer with an embedded single-bit-output all-digital frequency synthesizer is proposed. The output spectrum of the mixer is derived analytically based on that of the synthesizer as well as with simulation. A test setup using an FPGA implementation of the synthesizer and a discrete-component switching mixer has been built. Measurements are presented confirming the theoretical derivations.**

Keywords—switching mixer; frequency synthesizer;

I. INTRODUCTION

The interest in all-digital architectures has been intensified in the RFIC industry over the past few years due to the increasing challenge in the design and the extra cost of fabrication of RF analog and mixed-signal IC versus standard digital ones in modern nano-scale IC technologies. Digital circuit design has the advantage of portability, reconfigurability, automated checking and verification.

This paper proposes a switching RF down-converting mixer whose Local Oscillator (LO) input is driven by an embedded single-bit output all-digital frequency synthesizer, offering some of the aforementioned advantages compared to traditional analog mixer architectures.

Switching mixers are popular blocks in discrete-component designs and have been implemented in RFICs [1][1]. However, they are typically driven by classical PLLs or complex mixed-signal frequency synthesizers.

The proposed mixer architecture is shown in Fig. 1 below and is based on digital transmission gates which are driven directly by the single-bit output stream of the embedded all-digital frequency synthesizer. Certain dithering techniques are also used to make the synthesizer's spectrum sinewave-like and convert spurs to continuous noise floor.

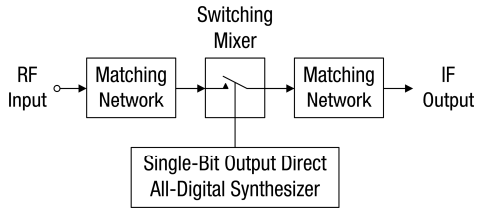

Fig. 1. Proposed switching mixer with embedded all-digital synthesizer.

First we discuss the embedded all-digital frequency synthesizer in Section II and state analytically its output spectrum. Then, the switching mixer architecture is described in Section III and its output spectrum is mathematically derived using that of the synthesizer. Finally the test setup is discussed and the measurements derived are presented and compared to the theoretical ones in Section IV.

II. EMBEDDED ALL-DIGITAL FREQUENCY SYNTHESIZER

The proposed mixer, shown in Fig. 1, comprises of a transmission gate which is digitally controlled by the all-digital frequency synthesizer. The synthesizer architecture and its output spectrum are described in the following sections.

A. Frequency Synthesizer's Architecture

The LO signal is provided by a Pulse Direct Digital Synthesizer (PDDS). It consists of a phase accumulator (*n*-bits wide), the Most Significant Bit of which is used as the output signal.

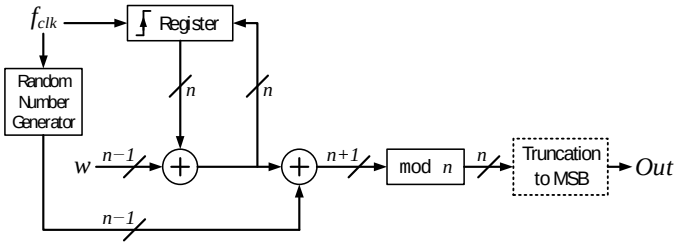

Fig. 2. Block diagram of single-bit output frequency synthesizer with phase dithering implementation.

PDDS is an extreme case of a single-bit DDS. Thus, especially when no oversampling is used, the output of the PDDS has deterministic timing irregularities and a spectrum full of strong and undesirable frequency spurs. Although the strongest frequency component is typically at the desirable average frequency, the spectral quality is unacceptable for analog and RF applications, unless a spurs-suppression technique is used.

Here we use phase dithering to randomize the synthesizer's output (otherwise) deterministic jitter and break any periodicity of it, spreading the power of the frequency spurs over the sampling bandwidth $[0, f_{clk}]$. As a drawback, a continuous noise floor is formed.

Dithering is implemented by generating a digital random sequence formed of independent and identically distributed random variables and adding it to the output of the Phase Accumulator (just before truncation) [2]. The cumulative distribution function of the random variables is of the form

$$F(u)=\left(1+\sin\left(\frac{\pi u}{2^{n-1}}-\frac{\pi}{2}\right)\right) \text{ with } u=0,1,2,\ldots,\left(2^{n-1}-1\right) \qquad (1)$$

It has been demonstrated [1] that the PDDS in Fig. 1 with such a dithering sequence results in spurs-free output.

B. Frequency Synthesizer's Output Spectrum

The average output frequency of the synthesizer, based on the clock frequency f_{clk}, is equal to $f_{LO}=\left(w/2^n\right)f_{clk}$ where the Frequency Control Word w (n-1 bits wide) ranges within $0<w<2^{n-1}$ and so f_{LO} takes values within $\left[0,\, f_{clk}/2\right]$ with step $f_{clk}/2^n$.

It can be shown that the output of the considered PDDS is equivalent to that of the uniformly dithered single-bit Nyquist-rate quantized sinewave [3]. So the Power Spectral Density (PSD) of the synthesizer's output $v(t)$, considered as a ±1 signal (and *not* as a digital 0/1 one) is given by

$$S_v(f)=\mathrm{sinc}^2\left(\frac{f}{f_{clk}}\right)\left[\frac{1}{4}\delta\left(f\pm\frac{w}{2^n}f_{clk}\right)+\frac{1}{2f_{clk}}\right] \qquad (2)$$

where $f\in\left[-f_{clk},\, f_{clk}\right]$ and the spectrum is f_{clk} - periodic except the envelop function $\mathrm{sinc}^2\left(f/f_{clk}\right)$.

III. Mixer Architecture & Output Spectrum

The mixer, shown in Fig. 1, has a simple single-ended switching structure with passive networks on the RF input and IF output ports for impedance matching. The switch, controlled by the PDDS's output acts essentially as 0/1 multiplier.

A. Mixer Output Spectrum

In this section we derive expressions of the output spectrum of the mixer. We denote the RF input signal as $g(t)$. The output of the mixer is essentially the multiplication result $y(t)=g(t)x(t)$ where $x(t)$ is the 0/1 single-bit output of the frequency synthesizer. We write $x(t)=\left(v(t)+1\right)/2$ to relate it with the ±1 signaling used for the expression of the spectrum in Eq. (2).

To determine the power spectral density of the mixer output $y(t)$ we calculate the autocorrelation function of the output[1] which is given by

$$R_y(t,t+\tau)=\frac{1}{4}E\left\{\left[v(t)+1\right]g(t)\left[v(t+\tau)+1\right]g(t+\tau)\right\} \qquad (3)$$

[1] Recall that the output of the mixer is a random signal due to the dithering.

Although $g(t)$ can be any signal, we consider it to be deterministic, e.g. a sinewave. The above equation becomes

$$\begin{aligned}R_y(t,t+\tau)&=\frac{g(t)g(t+\tau)}{4}E\left\{v(t)v(t+\tau)+v(t)+v(t+\tau)+1\right\}\\&=\frac{g(t)g(t+\tau)}{4}E\left\{v(t)v(t+\tau)+1\right\}\\&=\frac{g(t)g(t+\tau)}{4}\left[1+R_v(t,t+\tau)\right]\end{aligned}$$

where we used the fact $E\left\{v(t)\right\}=0$ for all values of t.

Since $y(t)$ is not a Wide-Sense Stationary (WSS) signal, instead of R_y we have to use the more general average-autocorrelation function defined as

$$\bar{R}_y(\tau)=\lim_{T\to\infty}\left[\frac{1}{2T}\int_{-T}^{T}R_y(t,t+\tau)\,\mathrm{d}t\right] \qquad (4)$$

To simplify the algebra we assume that $g(t)=A\sin\left(2\pi f_g t\right)$, implying after a few steps that[2]

$$\bar{R}_y(\tau)=\frac{A^2}{8}\cos\left(2\pi f_g\tau\right)\left[1+\bar{R}_v(\tau)\right] \qquad (5)$$

The power spectral density of $y(t)$ is the Fourier transform of $\bar{R}_y(\tau)$ [4], which is the convolution of the Fourier transforms of $\cos\left(2\pi f_g\tau\right)$ and $\left[1+\bar{R}_v(\tau)\right]$. The latter becomes $\left[\delta(f)+S_v(f)\right]$ where S_v is given by (2). Therefore,

$$\begin{aligned}S_y(f)&=\frac{A^2}{16}\left[\delta\left(f-f_g\right)+\delta\left(f+f_g\right)\right]\otimes\left[\delta(f)+S_v(f)\right]\\&=\frac{A^2}{16}\left[\delta\left(f-f_g\right)+\delta\left(f+f_g\right)+S_v\left(f-f_g\right)+S_v\left(f+f_g\right)\right]\end{aligned} \qquad (6)$$

Combining it with Eq. (2) we derive

$$\begin{aligned}S_y(f)=&\frac{A^2}{16}\left[\delta\left(f-f_g\right)+\delta\left(f+f_g\right)\right]\\&+\frac{A^2}{16}\mathrm{sinc}^2\left(\frac{f-f_g}{f_{clk}}\right)\left[\frac{1}{4}\delta\left(f-f_g\pm\frac{w}{2^n}f_{clk}\right)+\frac{1}{2f_{clk}}\right]\\&+\frac{A^2}{16}\mathrm{sinc}^2\left(\frac{f+f_g}{f_{clk}}\right)\left[\frac{1}{4}\delta\left(f+f_g\pm\frac{w}{2^n}f_{clk}\right)+\frac{1}{2f_{clk}}\right]\end{aligned} \qquad (7)$$

Since the mixer is used for down-conversion, the desirable component at the output is at frequency[3] $f=\left(w/2^n\right)f_{clk}-f_g$ and of amplitude $A^2\,\mathrm{sinc}^2\left(w/2^n\right)/64$ (see Eq. (7)). Again, from Eq. (7) the continuous noise power spectral density at the same frequency is given by

[2] Under some minor assumptions on the relationship between w, n and f_g.

[3] It is assumed that $f_{LO}\equiv\left(w/2^n\right)f_{clk}>f_g\equiv f_{RF}$.

$$\frac{A^2}{32 f_{clk}}\left[\operatorname{sinc}^2\left(\frac{w}{2^n}-\frac{2 f_g}{f_{clk}}\right)+\operatorname{sinc}^2\left(\frac{w}{2^n}\right)\right].$$

Therefore, the noise level with respect to the carrier equals

$$NPower = 10\log_{10}\left(\frac{\operatorname{sinc}^2\left(\frac{w}{2^n}-\frac{2 f_g}{f_{clk}}\right)}{1+\operatorname{sinc}^2\left(\frac{w}{2^n}\right)}\right)+3-10\log_{10}\left(f_{clk}\right)\ (\text{dBc})$$

If $w/2^n$ and f_g / f_{clk} are smaller than 0.3 or so then one can approximate the sinc functions with one and derive the simplified expression

$$NPower = 6-10\log_{10}\left(f_{clk}\right) \qquad (8)$$

IV. Measurements & Results

Our test setup consists of the mixer architecture in Fig. 1 with the all-digital frequency synthesizer implemented in a mini FPGA board (XuLA-50 / Xilinx Spartan-3A). Both the low-cost off-the-shelf transmission gate (with on/off switching time ~5ns) and the low-cost FPGA limit the frequency of operation of the mixer to a few tens of MHz.

Case 1: The clock frequency of the PDDS is $f_{clk} = 10\,\text{MHz}$ and its synthesized output frequency is set to $f_{LO} = 3$ MHz. The RF signal is a sinewave at $f_{RF} \cong 2.7$ MHz. The mixer's output spectrum centered at the desirable output frequency component $f_{LO} - f_{RF}$ is shown in Fig. 3.

From Eq. (8) we derive that the noise floor in this case is about $-64\,\text{dBc}$. This is exactly what the measurement in Fig. 3 below shows.

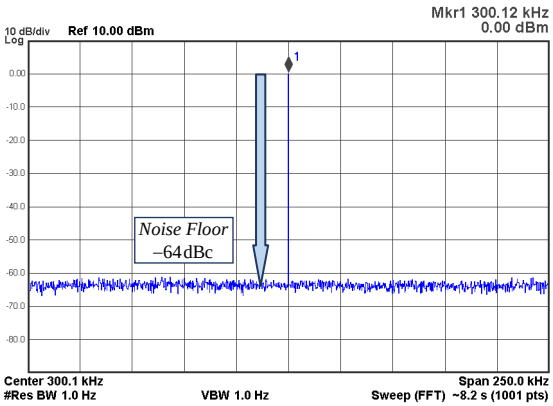

Fig. 3. Output of the switching mixer, with $f_{clk} = 10\,\text{MHz}$, $f_{RF} = 2.7$ MHz, $f_{LO} = 3$ MHz (centered at 300 kHz).

Case 2: The clock frequency of the PDDS is $f_{clk} = 200\,\text{MHz}$ and its synthesized output frequency is set to $f_{LO} = 21.2$ MHz. The RF signal is a sinewave at $f_{RF} \cong 20$ MHz. The mixer's output spectrum $0-50$ MHz is shown in Fig. 4 as well as in Fig. 5 which is centered at the desirable frequency component $f_{LO} - f_{RF}$. The gradient of the noise floor near zero frequency is probably due to the lack of calibration of the spectrum analyzer below 10MHz.

Again, using Eq. (8) we derive that the noise floor level should be about $-77\,\text{dBc}$. The estimate is confirmed by the measurement in Fig. 5 below.

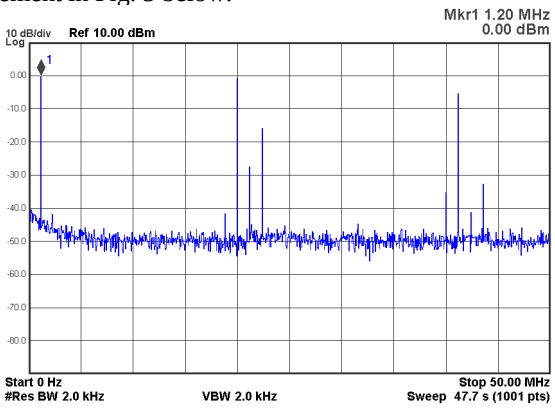

Fig. 4. Output (0-50 MHz) of the switching mixer, with $f_{clk} = 200\,\text{MHz}$, $f_{RF} = 20$ MHz, $f_{LO} = 21.2$ MHz.

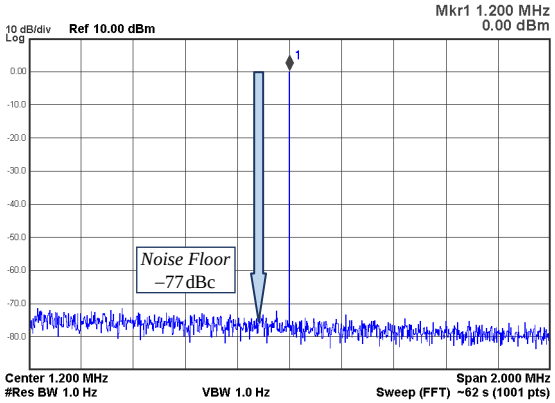

Fig. 5. Output of the switching mixer, with $f_{clk} = 200\,\text{MHz}$, $f_{RF} = 20$ MHz, $f_{LO} = 21.2$ MHz (centered at 1.2 MHz).

V. Conclusions

A switching RF down-converting mixer with an embedded all-digital frequency synthesizer has been proposed and its output spectrum has been derived mathematically. The measurements with our test setup agree with the theory. Future directions include balanced switching architectures and VLSI implementations of this approach in order to illustrate results in higher frequencies.

References

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