

All-Digital Video RF Transmitter with Embedded Direct Frequency Synthesizer

And an FPGA implementation of It

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Abstract— This paper presents a fully-digital analog-television RF transmitter realized on a small FPGA. Phase Alternating Line (PAL) encoding algorithms have been implemented along with digital filters and a Direct Digital frequency Synthesizer, for generating the carrier signal, achieving RF transmission of greyscale image captured from an onboard video camera.

Keywords—Direct digital synthesis, frequency spurs, quantization, Digital-to-Analog converter

I. INTRODUCTION

Direct digital synthesizers (DDS) or numerically controlled oscillators are important in many digital communication systems [1], [2]. Quadrature synthesizers are used for constructing digital up and down converters, demodulators, and implementing various types of modulation schemes, including PSK (phase shift keying), FSK(frequency shift keying), and MSK (minimum shift keying) [3].

A common method for digitally generating a complex or real valued sinusoid employs the use of a phase accumulator and a sine/cosine lookup table. The lookup table stores samples of a sinusoid whereas the phase accumulator is used to generate a suitable phase argument that is mapped by the lookup table to the desirable output waveform. The average frequency of the DDS is defined by the frequency control word w and the system clock, f_{clk} . The desirable frequency generated by the DDS is given by the following equation [4]:

Often a quantizer [5] is introduced between the phase accumulator and the LUT. The quantizer receives high precision phase angle and generates a lower precision representation of the angle in order to reduce the size of the LUT. This process decreases the size of the LUT from $2^n \cdot M$ to $2^t \cdot M$ but as an aftereffect introduces phase noise and unwanted spurious spectral components in the DDS output signal.

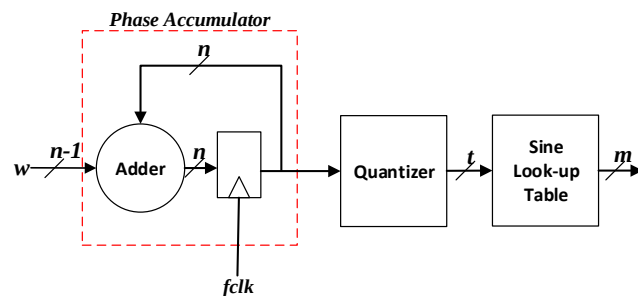


Figure. 1. Direct digital synthesizer core

Amplitude quantization is often employed in the output of the LUT, decreasing the word length of the amplitude to m bits. Amplitude quantization has an important effect on the spectral fidelity of the output signal introducing noise which decreases the signal-to-noise ratio. An approximation of the SNR in the output is given by [4]:

$$02 \cdot m$$

The maximum frequency output is given by the uniform sampling theorem — although a maximum frequency of — is often preferred.

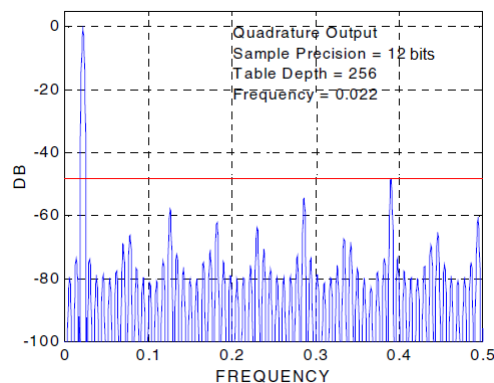


Figure. 2. Typical spectrum of the DDS core used with table depth = 256 and 12-bit precision samples [3]. Here it is $f_{out} = 0.022 \cdot f_{clk}$

The output of DDS is not perfectly periodic for most of the values of w resulting in an output signal with deterministic timing irregularities and a spectrum full of possibly strong and undesirable frequency spurs [6],[7]. Both phase and amplitude quantization techniques used in the process result in spectral artifacts. The depth of the look-up table affects the phase angle resolution and width affects the amplitude resolution of the signal. These resolution constraints are equivalent to time base jitter [8] and amplitude quantization of the signal and add spectral modulation lines and a broad-band noise floor to the signal's spectrum as shown in Fig. 2.

II. PHASE ALTERNATING LINE (PAL) ANALOG TELEVISION ENCODING SYSTEM

A fully digital PAL television signal transmitter has been designed and implemented. PAL, short for Phase Alternating Line, is one of the three color encoding systems for analogue television and has been popular in most European countries. The other two analogue systems are NTSC and SECAM [9].

PAL encoding system has some advantages compared to the other two encoding systems. In contrast to NTSC, PAL does not require tint control circuit in order to perform color correction. In contrast to NTSC, the PAL standard automatically cancels hue errors by phase reversal, so tint control is unnecessary. This causes lower saturation, which is much less noticeable to the eye than NTSC hue errors. SECAM on the other hand uses Frequency Modulation with alternative transmission of the chrominance vectors. Although this technique solves the hue errors, the signal is more sensitive to cross-color intermodulation and a delay line is required at the receiver.

A frame in PAL encoding system (576i) consists of 625 lines, with 610 visible lines divided into two interlaced frames and 15 synchronizing lines.

Vertical synchronizing sequence for field 1, starts from scanline 623 and ends in scanline 5 inclusive. It consists of 6 pre-equalizing pulses, 5 long sync pulses and 5 post-equalizing pulses.

The synchronizing sequence for field 2 starts from line 311 and ends in line 317 inclusive. It consists of 5 pre-equalizing pulses, 5 long sync pulses and 4 post-equalizing pulses. During the transmission of vertical sync pulses, teletext data can also be transmitted.

A typical PAL encoder consists of a complex system, where the chrominance components (U and V) are quadrature amplitude modulated and then added to the luminance signal (Y) in order to produce a complex baseband composite signal.

Then this signal is amplitude modulated to the desirable frequency and passed through a vestigial filter. Along with the visible components of the signal, horizontal and vertical synchronizing pulses and color subcarrier bursts are transmitted. The audio signal is Frequency Modulated and transmitted on a different carrier frequency in the same

channel. The total bandwidth of the channel, including the picture and audio signal cannot extend more than 8 MHz as shown in fig. 5.

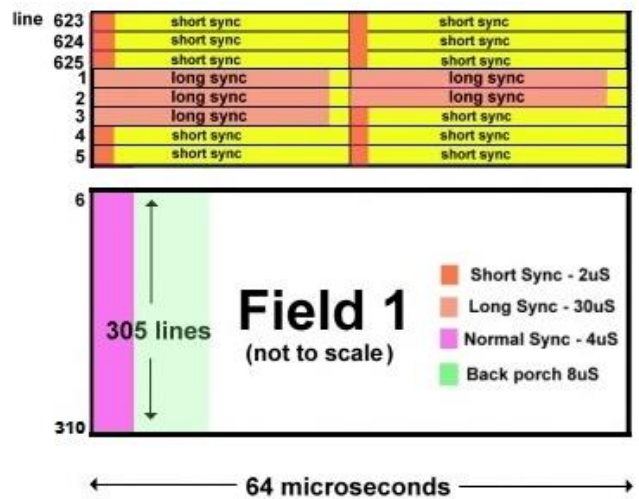


Figure 3. Field 1 in PAL consisting of picture and synchronizing scanlines

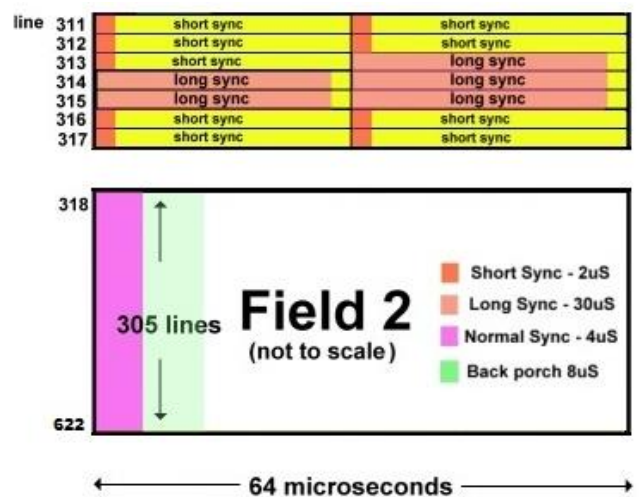


Figure 4. Field 2 in PAL consisting of picture and synchronizing scanlines

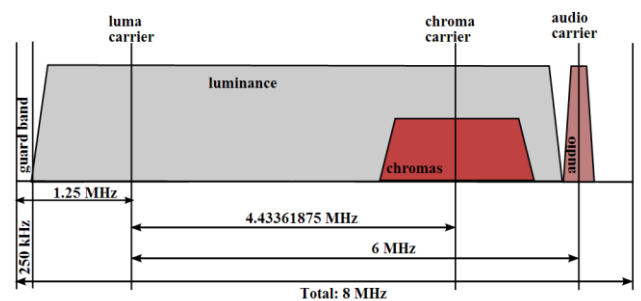


Figure 5. Spectrum of a television channel with PAL

In order to implement a PAL encoder, a specially designed Finite State Machine and visual encoding algorithms have been created Fig.6. The image transmitted can be provided from another system, using a digital interface (ie. a PC using USB) or captured directly from a

video camera. For the purpose of the live demo we selected the second approach.

Image is live captured from an onboard inexpensive VGA camera module. Due to the different timings of VGA and PAL protocols, a RAM-based frame buffer is used to store the contents of a frame. The image is then encoded to the phase alternating line system and filtered in order to meet the bandwidth limitations. We have to note that due to limitations of RAM blocks on this entry level FPGA board, only a black and white picture is transmitted, whereas in a bigger FPGA board or an ASIC, a color transmitter can be implemented with minor modifications in the architecture.

In order to modulate the encoded baseband data stream, an n-bit wide Direct Digital Synthesizer is needed. Using multi-bit-output phase-dithered DDS we generate a 9-bit wide carrier sinusoid. The amplitude modulation is digitally implemented by directly multiplying the binary carrier and the DC-shifted composite data stream. Finally using digital amplitude dithering the multi-bit modulated signal is converted to 4-bit digital stream which is converted to analog trivial DAC realized with a resistor network.

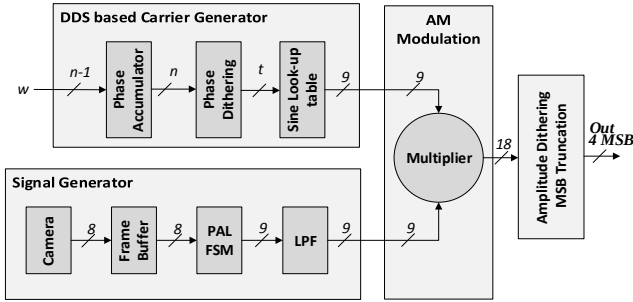


Figure 6. DDS-based all-digital PAL video RF transmitter architecture using 4 bit random dithering DAC

III. RANDOM NUMBER DITHERING AND 4-BIT QUANTIZATION

Although many techniques are proposed in order to convert the multi-bit digital signal to a single-bit analog one, many of them require the use special or accurately matched analog components and detailed and time consuming analog design.

The proposed architecture requires the minimal use of analog components and can be easily implemented on any FPGA or ASIC integrated circuit. Instead of driving the multi-bit signal to the output DAC, amplitude dithering is employed and the most significant bits are driven to a low resolution DAC. This technique eliminates most of the unwanted spurs generated in all the stages of the signal path with the cost of the increased noise floor. The noise floor at the output is given in relationship to process gain and SNR by the following equation:

$$NF = 10 \cdot \log_{10} \left(\frac{f_{clk}}{2} \right) + 6.02 \cdot \log_2 \left(\frac{\text{output levels}}{2} \right) \text{ dBc/Hz}$$

Where the first term represents the process gain and the second term represents the gain due to the use of more than one output bits.

There are two techniques proposed for quantization of a fully digital multi-bit signal into an analog single-bit one. In both techniques a source of random a uniform noise is used [10], [11]. The multi-bit uniform noise generated by a random number generator is added to the AM modulated signal fig.7 and fig.8. and then the three or four most significant bits are kept.

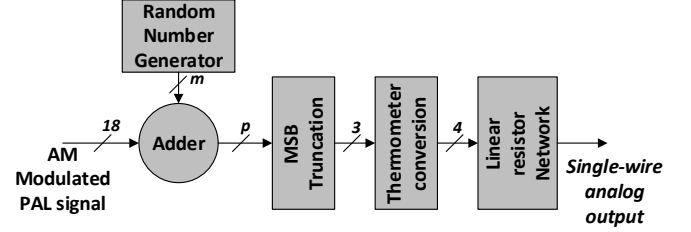


Figure 7. Binary resistor network

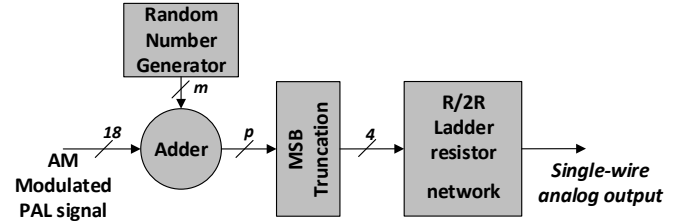


Figure 8. R/2R Ladder resistor network

In the case we use a binary resistor network, the three MSBs are thermometer coded and then driven to a binary resistor network fig. 9a.

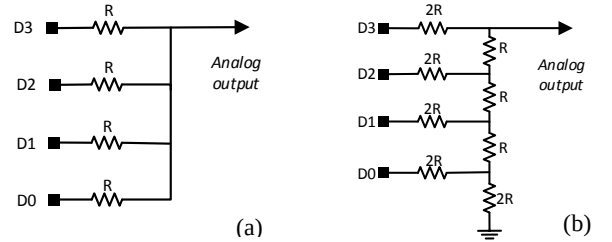


Figure 9. (a) Binary resistor network, (b) R/2R ladder resistor network

The second technique employs the use of an R/2R ladder resistor network. This technique improves the precision with the use of the same number of components fig. 9b.

IV. FPGA IMPLEMENTATION/LIVE DEMO

Based on the proposed architecture in section II, and for the purpose of a live demonstration, the demo board in fig.10 was built. It is based on Papilio One [12], an entry level FPGA board, using Xilinx's Spartan 3E XC3S250E FPGA. This entry level FPGA has an equivalent of 250K gates and

only 216Kbits of Block RAM. A phase dithered DDS of $n = 9$ bits has been selected.

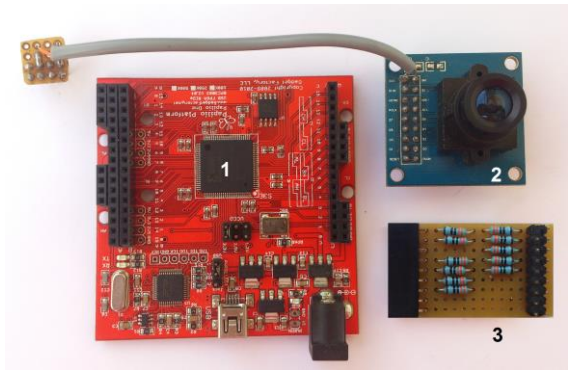


Figure. 10. Board built for the purpose of the Live Demo

1. Papilio One/ Spartan 3E FPGA Board
2. OV7670 VGA Video Camera Module
3. R/2R ladder resistor network

For the analog-to-digital conversion, a random-dithering DAC was used. The only analog components are eight resistors, avoiding the use of active analog components.

The FPGA utilization of this implementation is presented in fig.11. Despite the use of a small FPGA chip, the whole project, including the camera module, PAL encoding algorithms, AM modulation and dithering module, occupies only 14% of the total chip resources.

The implementation operated at 200MHz achieving noise floor of about 88dBc/Hz (within the desirable frequency range) fig.13.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	
Number of Slice Flip Flops	352	4,896	7%	
Number of 4 input LUTs	495	4,896	10%	
Number of occupied Slices	365	2,448	14%	
Number of bonded IOBs	20	66	30%	

Figure. 11.Device utilization of the implemented Video RF transmitter



Figure. 12. Footage from the FPGA-based PAL Video RF transmitter

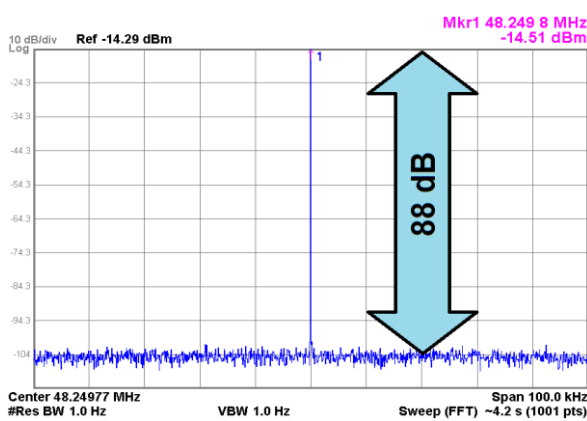


Figure. 13.FPGA Implementation (spectrum analyzer measurement of DDS output) using binary resistor network. Resolution BW = 1 Hz and waveform averaging Nav=10 runs

V. CONCLUSIONS

A versatile purely digital analog video transmitter architecture, that results in minimum chip-area, low-power and low-cost implementations, has been presented, including a nearly all-digital DAC. Measurements have demonstrated a dynamic range of over 88dBc/Hz. Random number dithering can reduce the size of the DAC, finally resulting in a single-bit output analog circuit. Through this work, it has been shown that the fabrication of traditionally analog circuits is possible, using only digital design techniques.

REFERENCES

- [1] U.L. Rohde, Microwave and Wireless Synthesizers: Theory and Design, 1st ed. Singapore: Wiley-Interscience, 1997
- [2] J. Vankka and K. Halonen, Direct Digital Synthesizers: Theory, Design and Applications, New york, Springer 2006
- [3] K. Galanopoulos*, P. Sotiriadis, "Modulation Techniques for All-Digital Transmitters Based on Pulse Direct Digital Synthesizers", IEEE International Frequency Control Symposium 2012.
- [4] Victor S. Reinhardt, "Spur Reduction Techniques in Direct Digital Synthesizers", Los Angeles: Hughes Space and Communications Company,1993
- [5] "Xilinx DDS v5.0 Compiler Product Specification", DS246 April 28, 2005
- [6] Lionel Cordesses, "Direct Digital Synthesis: A Tool For Periodic Wave Generation", Signal Processing Magazine, IEEE, July 2004
- [7] P. Sotiriadis, K. Galanopoulos*, "Direct All-Digital Frequency Synthesis Techniques, Spurs Suppression, and Deterministic Jitter Correction", IEEE Trans. on Circuits and Systems-I, Vol. 59, No. 5, May 2012, pp. 958-968.
- [8] O'Leary, P. ; Joanneum Res." A direct-digital synthesizer with improved spectral performance", July 1991
- [9] ITU Radiocommunication Bureau (BR) "BT.470-5 - Conventional television systems", February 2005.
- [10] K. Galanopoulos, P. Sotiriadis, "Optimal Dithering Sequences for Spurs Suppression in Pulse Direct Digital Synthesizers", IEEE International Frequency Control Symposium, 2012.
- [11] P. Sotiriadis, N. Miliou, "Single-Bit Digital Frequency Synthesis via Dithered Nyquist-rate Sinewave Quantization", to appear in the IEEE Trans. on Circuits and Systems-I
- [12] Papilio One FPGA Board Product Information, Available at: <http://papilio.cc/index.php?n=Papilio.Hardware>