Optimal Dithering Sequences for Spurs Suppression in Pulse Direct Digital Synthesizers

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***Abstract*—Spurs-free frequency synthesis with minimal noise floor is achieved by the classical Pulse Direct Digital Synthesizers using a new class of dithering sequences with specific statistical properties. The generation of dithering sequences having statistical properties very close to those of the ideal ones with low-complexity architectures is also discussed and used to form All-Digital frequency synthesizers of minimal footprint and power consumption.**

I. INTRODUCTION

Over the past decade Direct All-Digital Frequency Synthesis (DADFS) techniques have gained popularity over the traditional analog and mixed-signal alternatives [1]-[4]. These techniques are typically realized using a digital frequency divider (Fig. 1) which (fractionally) divides the reference clock and is programmed by the frequency control word (FCW).

The output is a 1-bit digital signal and since the frequency divider can only change its output value on rising (or falling) edges of the reference clock, the generated signal is not perfectly periodic for most of the values of the FCW. However the output signal has an average frequency, which is set by the FCW.

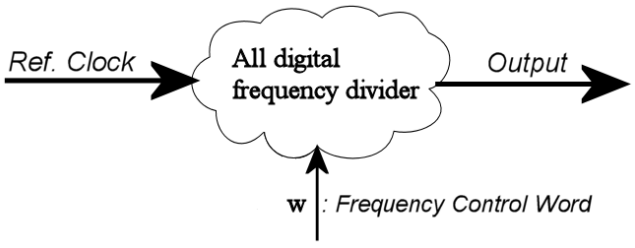

Figure 1. Typical DADFS functionality diagram.

DADFS being purely digital topologies have all the advantages of digital circuits. So using these techniques a technology-portable fully scalable and reconfigurable synthesizer can be easily included as a block in any digital library. By doing so, the development time of a synthesizer can be eventually reduced from months to minutes. In this work in particular, we focus on proposing a DADFS-based frequency synthesizer architecture of minimal chip area and power consumption with acceptable performance for a wide range of applications.

One of the most commonly used DADFS cores is the Pulse Direct Digital Synthesizer (PDDS) [2]. Other available DADFS cores are the flying adder synthesizer [3], the fractional N/N+1 dividers [4] etc. The PDDS (Fig. 2) is actually a reduced version of the standard DDS core [2] without the Sin Look Up Table and the Digital to Analog converter. It consists only of a phase accumulator (*n*-bits wide), the Most Significant Bit of which is used as the output.

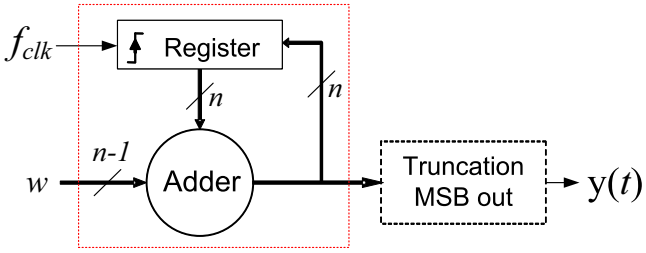

Figure 2. Pulse Direct Digital Synthesizer (PDDS) core.

Based on the reference clock f_{clk}, Eq. (1) gives the average output frequency of the PDDS which is proportional to the FCW (*n*-1 bits wide) and can range within (0 , $f_{clk}/2$), typically with very high resolution.

$$f_{ave} = \frac{w}{2^n} \cdot f_{clk} \tag{1}$$

As with all DADFS, the output of PDDS is not perfectly periodic for most of the values of the FCW resulting in an output signal with deterministic timing irregularities and a spectrum full of strong and undesirable frequency spurs as

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shown in Fig. 3. The strongest frequency component is (typically) at the desired average frequency f_{ave} but unless some spurs-suppression technique is used, the spectral quality is unacceptable for analog and RF applications.

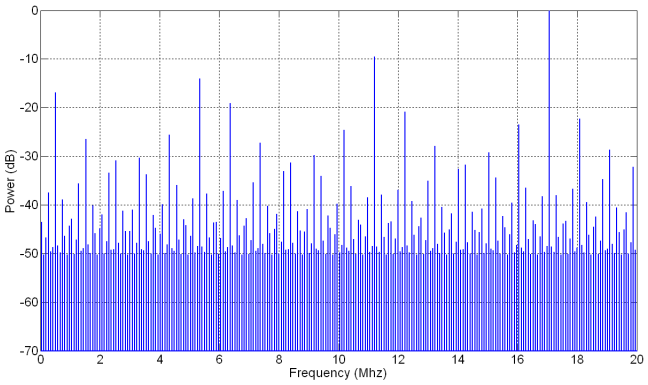

Figure 3. Output spectrum of PDDS (Matlab, f_{clk} = 40Mhz).

Various spurs-reduction techniques have been proposed [1]. These mainly fall into three categories: *Pulse retiming* using some type of adjustable delay elements [5],[6], *Filtering* techniques using a cleanup PLL or analog filters and the *Dithering* technique [4],[7]. Among them the only one that can be purely digitally implemented, while achieving high spurs-suppression is the dithering technique.

In spurs-suppression dithering, a digital random sequence is added to a certain point of the synthesizer. The goal is to randomize the synthesizer's output deterministic jitter breaking any periodicity of it and spreading the power of the frequency spurs over a wide frequency range. As a drawback a (flat or slightly colored) noise floor is formed.

Dithering techniques strongly depend on the properties of the random sequence used. The first property is its Spectral properties, like the Power Spectral Density (PSD). A noise signal is called white noise when it has a flat PSD. The second one is its Distribution properties, like the probability mass function of its symbols $f_x(x) = P(r = x)$ and its cumulative distribution function $F_x(x) = P(r < x)$. The simplest case is when we have a uniformly distributed sequence (with a flat f_x function and linear $F_x(x) = ax$ function).

In this paper we first examine the properties that the random dithering sequence should have to result in a spurs-free PDDS output. Then we examine various techniques both for optimal and semi-optimal dithering sequence generation.

II. Spurs Suppresion Using Dithering in PDDS

There are two main ways of applying dithering to a PDDS core [7]. The first one, *frequency dithering*, is realized by adding the random sequence to the FCW of the Phase Accumulator as illustrated in Fig. 4. The second one, *phase dithering*, is implemented by adding the sequence to the output of the Phase Accumulator (just before truncation) as shown with Fig. 5. It has been shown in [1] that these two schemes generate equivalent results under certain conditions. The phase dithering scheme thought has overall a lower hardware complexity and so we focus on this one in the paper.

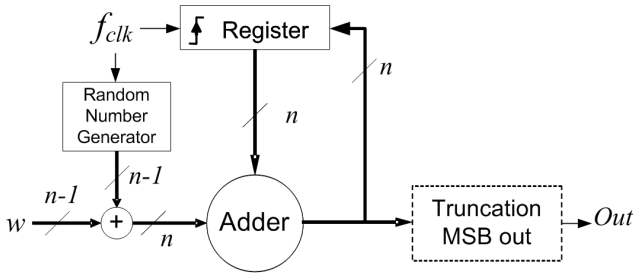

Figure 4. Frequency dithered PDDS core.

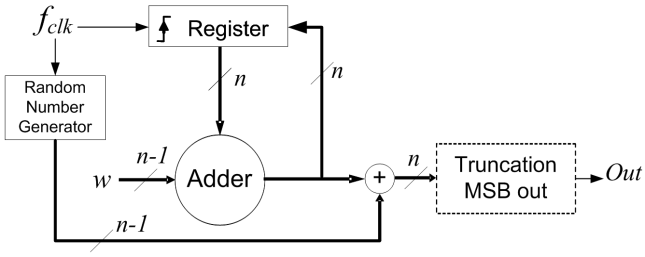

Figure 5. Phase dithered PDDS core.

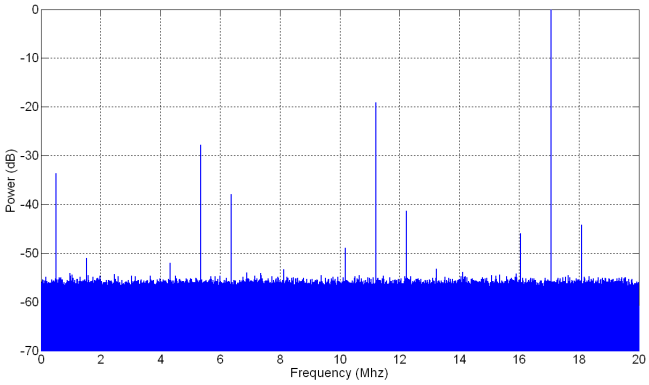

Figure 6. Spectrum of a phase dithered PDDS using a white and uniform noise sourse (Matlab, f_{clk} = 40Mhz).

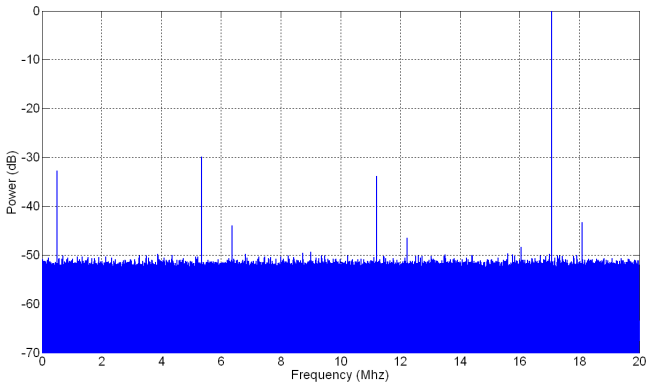

Figure 7. Spectrum of a phase dithered PDDS using a white and uniform noise sourse of increased strength (Matlab, f_{clk} = 40Mhz).

Typically, white and uniform random sequences are used for the phase dithered PDDS, but as we can see in Fig. 6, this type of random sequence fails to eliminate many of the undesirable frequency spurs, especially the strongest ones. One can increase the dithering amplitude to further suppress the spurs, however, complete elimination is not possible in most cases (Fig. 7) and the noise floor increases significantly.

Note that generally, the dithering scheme and sequence used imply the number and strength of the remaining spurs while the FCW only defines their frequencies. In the next section, a new approach to choosing the statistical properties of the random dithering sequence is presented. It provably results in elimination of all spurs and introduces the minimum possible noise floor.

III. Optimal Dithering Sequence

Extended analysis and experimentation with the selection process of random dither sequences for spurs suppression indicates that the distribution properties of the random sequence are the most important ones. From here on we focus on the distribution assuming that the spectrum of the random sequence is white.

For the case of the phase-dithered PDDS this work proposes the random dithering sequence with probability mass function f_x of the form $\sin(0:\pi)$ and equivalent cumulative distribution function F_x of the form $\sin(-\pi/2:\pi/2)$ as shown in Fig. 8. The sequence should always have the typical signal amplitude of n-1 bits, as indicated in Fig. 5.

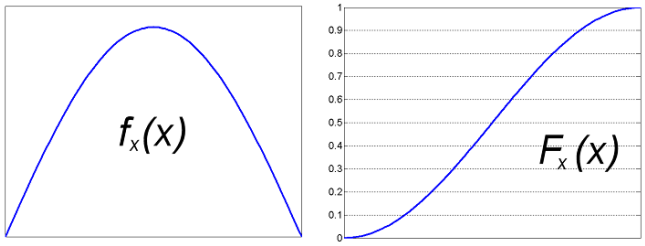

Figure 8. Proposed dithering sequence: Probability mass function f_x and Cumulative distribution function F_x.

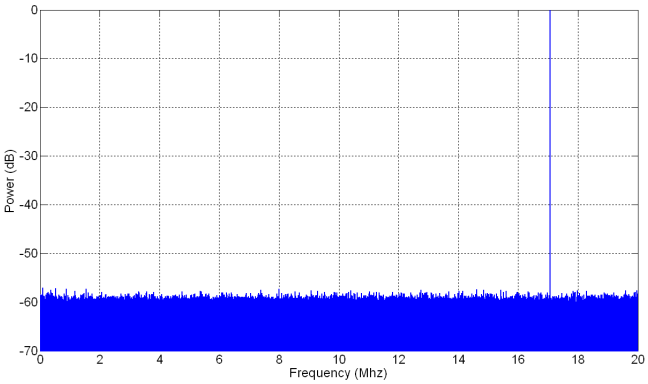

Figure 9. Spectrum of a phase dithered PDDS using the proposed (optimal) dithering sequence (Matlab, f_{clk} = 40Mhz).

Using such a dithering sequence results in *spurs free* output spectrum, like that in Fig. 9; this has been proven mathematically in a more general setting implying the optimality of the proposed sequence. Moreover, the noise floor in Fig. 9 is lower than that in Fig. 6 resulting from uniformly distributed white noise of similar amplitude.

The proposed sinusoidal-distributed random sequence can be generated by passing a white, uniformly distributed random sequence thought an *Arcsin* (inverse sin) type of function (Fig. 10). The result is a white noise sequence of the desired distribution properties. This method however may require an involved hardware implementation.

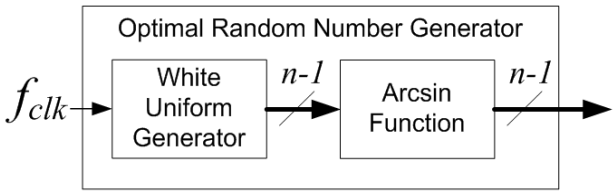

Figure 10. Method for generating the optimal sequence.

IV. Semi-Optimal Dithering Sequences

The closer the distribution of a random sequence is to that of the optimal the better its spurs reduction properties are. In an effort to minimize the hardware complexity of the dithering sequence generator we present the two distribution-approximation techniques of Fig. 11.

Approximation-I (red dotted) is of *Triangular* form and it can be generated by adding two independent white and uniform noise sources (R_{wu1} and R_{wu2}), i.e. $r_I = (R_{wu1} + R_{wu2})/2$. The generated sequence should have elements n-1 bits wide, so amplitude normalization is in order.

Approximation-II (green dashed) is of *Trapezoidal* form and is also implemented by the weighted averaging of two independent noise sources: $r_{II} = (R_{wu1} + R_{wu2}/2)\cdot(2/3)$. As seen in Fig. 11, this approach fits better to the ideal sequence, on the other hand it requires an additional multiplier for the implementation of the (2/3) scaling factor.

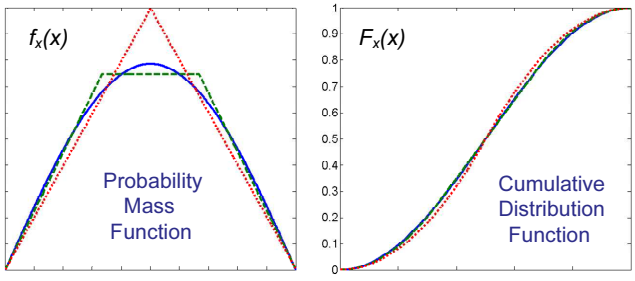

Figure 11. Probability Mass Function and Cumulative Distribution Function of: an ideal sequence (blue solid), approximation I (red dotted, of Triangular form) and approximation II (green dashed, of Trapezoidal form).

The output spectrum of a phase dithered PDDS using approximation-I is presented in Fig. 12. The improvement (compared to the white uniform dithering of Fig. 6) is significant, but there are still three strong spurs remaining. As

expected the approximation-II behaves better as it only fails to eliminate two spurs (Fig. 13). The remaining spurs are also of relatively low strength. The noise floor is in both cases on par with the optimal dithering sequence (Fig. 9).

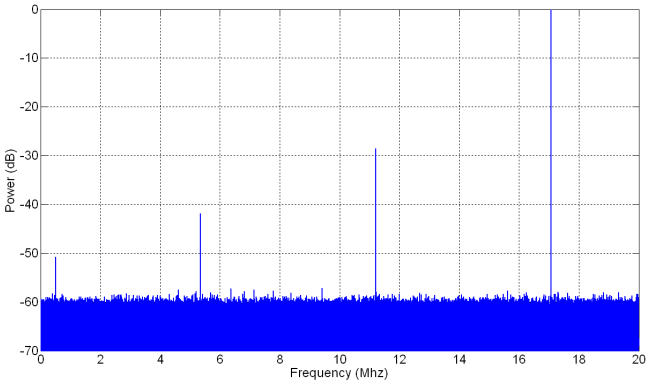

Figure 12. Spectrum of a phase dithered PDDS using Approximation-I type sequence (Matlab, f_{clk} = 40Mhz).

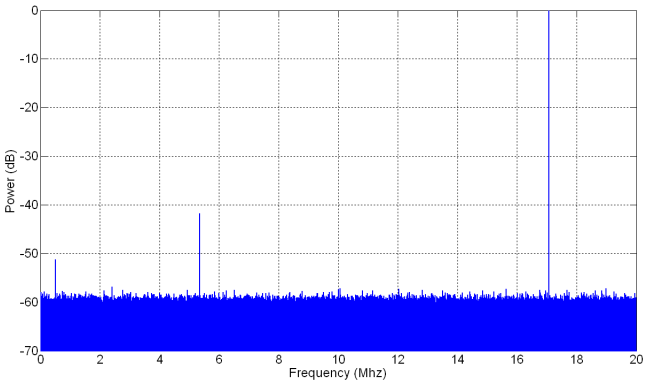

Figure 13. Spectrum of a phase dithered PDDS using Approximation-II type sequence (Matlab, f_{clk} = 40Mhz).

V. FPGA IMPLEMENTATION

The proposed architecture of Approximation-II has been implemented using a Xilinx Spartan 3e (of 500K equivalent gates) FGPA evaluation board (Fig. 15). A phase dithered PDDS of n = 25 bits has been selected. The design achieved an operating frequency of f_{clk} = 200Mhz. The proposed minimalistic architecture allowed this high frequency of operation of this entry-level FPGA board. The actual FPGA implementation device utilization of this small design is shown in Fig. 14. The spectral performance is presented in Fig. 16. The implementation achieves a noise floor performance of about 80dBc/Hz.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	126	9,312	1%
Number of 4 input LUTs	87	9,312	1%
Number of occupied Slices	89	4,656	1%
Number of MULT18X18SIOs	1	20	5%

Figure 14. FPGA Implementation (Device Utilization)

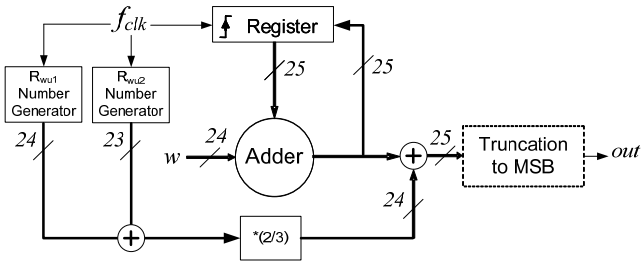

Figure 15. Block diagram of a phase dithered PDDS core of 25-bit, using Apoximation II for random sequence generation. (FPGA implemented)

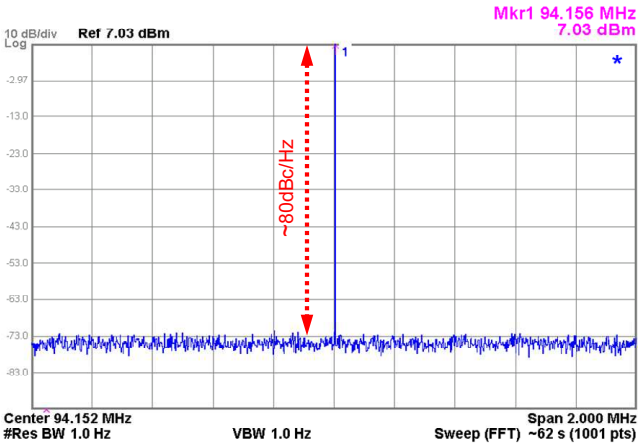

Figure 16. FPGA Implementation (spectrum analyzer measurement)

As a closing comment we should note that the noise floor level is independent of the value of the FCW and only depends on the rate of the reference f_{clk} signal. Doubling the rate will further decrease the noise floor level by 3dB/Hz. The following formula gives the exact relation between f_{clk} rate and noise floor: $Noise\ floor = \left(10\log_{10}\left(f_{clk}\right) - 3\right)$ dBc/Hz.

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