All-Digital Low-Power Radio-Transmitter Architecture

And an FPGA Implementation of It

Kostas Galanopoulos
Electrical and Computer Engineering
National Technical University of Athens, Greece
galanopu@ieee.org

Paul P. Sotiriadis
Electrical and Computer Engineering
National Technical University of Athens, Greece
pps@ieee.org

***Abstract*— An All-Digital FM radio transmitter is presented supporting both analog and digital modulation schemes. It is composed of an all-digital frequency synthesizer, an all-digital modulator, and a nearly all-digital ADC for analog audio acquisition. This All-Digital radio transmitter is a versatile architecture, which provides an alternative to popular analog-RF architectures, offering low cost, minimal chip-area and low-power solutions while achieving performance, adequate for many modern wireless applications.**

All-Digital transmiter, FM Radio transmiter, Pulse Direct Digital Synthesizer, oversampling ADC.

I. INTRODUCTION

RF transceivers are some of the few remaining analog-intensive blocks in modern wireless Systems-On-Chips. Designing their RF/analog blocks, in contrast to digital ones, requires significant effort and time due to limited automation and porting capability in the design process. In addition, RF blocks may require advanced fabrication technologies which are much more expensive than standard CMOS ones. Over the past decades, major effort has been dedicated in replacing analog and RF blocks by digital ones, e.g. frequency synthesizers [1] and base-band signal processors, resulting in dramatic cost reduction.

This paper (and demo) presents an all-digital transmitter implemented in a mini FPGA board (XuLA-50 / Xilinx Spartan 3A of 50k equivalent gates). The architecture is very versatile and can be easily modified to accommodate most of the commonly used modulation schemes as well as to operate in any desirable frequency supported by the FPGA or ASIC technology used. For the purposes of the demo and due to the limitations of the particular FPGA board (maximum operating frequency: fclk = 200Mhz), the transmitter has been setup to operate in the FM radio band (87.5 to 108.0 MHz) and be modulated by audio signal generated by an external source.

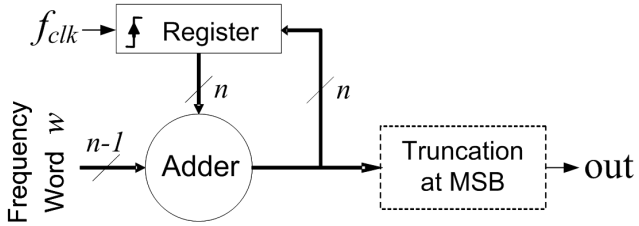

Figure 1. Pulse Direct Digital Synthesizer core.

The All-digital transmitter is based on Direct All-Digital Frequency Synthesis (DADFS) and Modulation techniques along with some other near All-Digital techniques for Analog to Digital and Digital to Analog conversions (as Σ/Δ and oversampling).

II. DIRECT ALL-DIGITAL FREQUENCY SYNTHESIS

The DADFS fractionally divides a reference clock signal f_{clk} (using a digital divider) to produce the output signal. A Frequency Control Word (FCW) w sets the division ratio and so the Average output Frequency.

One of the simplest to build and most commonly used DADFS cores is the Pulse Direct Digital Synthesizer (PDDS) Figure 1, [2]-[4]. It consists of a phase accumulator (of *n* bits-wide), the Most Significant Bit of which is used as the output. This digital 0/Vdd output (RF) signal can be used to drive a highly efficient on/off RF power amplifier or be fed to an antenna via an output digital inverter of the FPGA.

The PDDS is a synchronous FSM so its output can only change its value at the (rising) edges of the system clock [4]. Hence the output is not a perfect periodic signal and has timing irregularities (deterministic jitter) for most generated (average) output frequencies Figure 2. This (deterministic) Jitter is less than or equal to ½ Clock Cycle. The average frequency of the output is given by the expression:

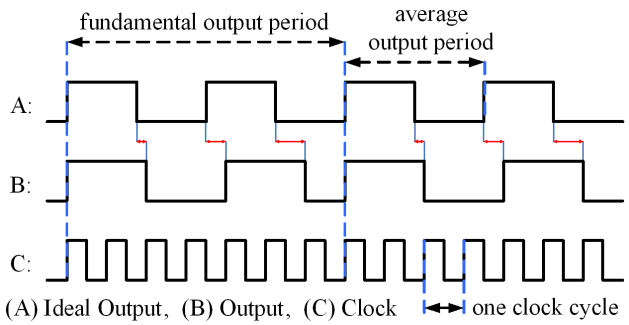

Figure 2. Output of the Pulse Direct Digital Synthesizer.

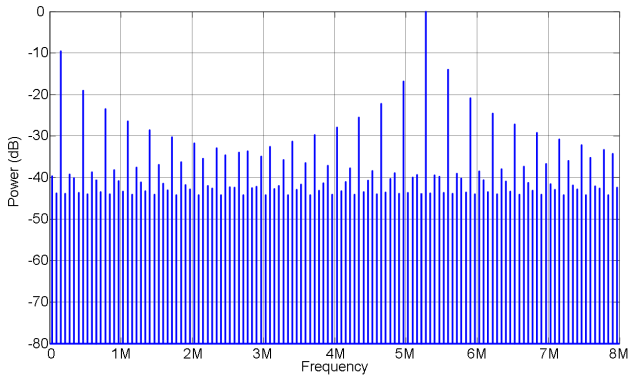

Figure 3. Output spectrum of PDDS (Matlab, f_{clk} = 16Mhz).

$$f_{ave} = \frac{w}{2^n} \cdot f_{clk} \tag{1}$$

The FCW, w, of the PDDS is n-1 bits wide so it can generate frequencies up to $f_{clk}/2$, typically with very high resolution (n can be large, e.g. n=20). The output waveform is periodic of fundamental frequency f_{fund} which is less than or equal to f_{ave} (typically it is significant less), given by:

$$f_{fund} = \frac{\gcd\left(w, 2^n\right)}{2^n} \cdot f_{clk} \tag{2}$$

The deterministic jitter of the PDDS output causes strong undesirable spurs in the frequency domain, Figure 3 (MATLAB). Due to these strong spurs the PDDS cannot be used as an All-Digital transmitter unless a spurs reduction technique is used [4]. Among them the only one that can be purely digitally implemented is the Dithering technique [5].

III. Spurs Reduction Using Dithering

In spurs reduction using dithering scheme a random phase or frequency dithering is applied to PDDS to break the periodic patterns of the output. By doing so the power of the undesirable frequency spurs is spread over a wide range of frequencies (ideally a frequency continuum). While this method can completely eliminate all undesirable spurs, major part of the

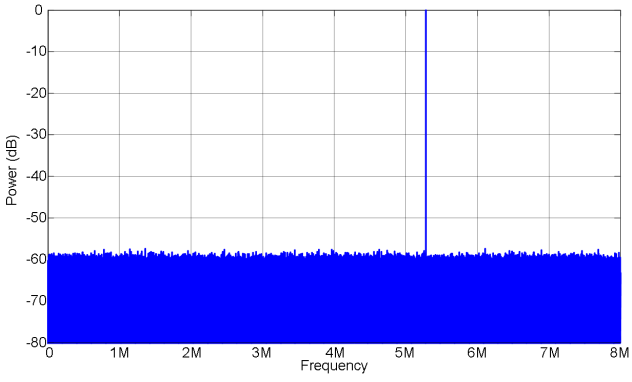

Figure 4. Output spectrum of dithered PDDS (Matlab, f_{clk} = 16Mhz). Equivalent resolution bandwidth is 1 Hz

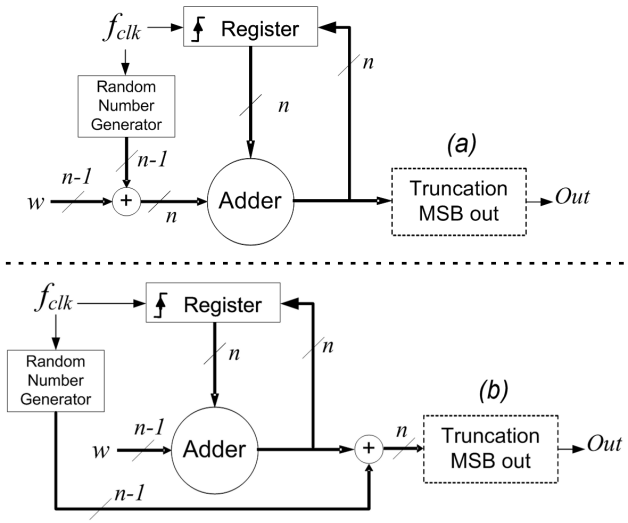

Figure 5. Dithering on PDDS: a) Frequency Dithering b) Phase Dithering

spurs' power is converted into wideband noise raising the noise floor Figure 4 (MATLAB). This is a drawback of the dithering technique. The noise floor is lowered using higher f_{clk}.

There are two ways to apply dithering to a PDDS. The first one is illustrated in Figure 5a, where a random number sequence is added directly to the FCW. This method is called frequency dithering. It is preferable that the output sequence of the random number generator has a zero mean so that the f_{ave} of the output of the PDDS remains unaltered.

The second way is called phase dithering and is illustrated in Figure 5b. Here the random number sequence is added to the output of the Phase Accumulator, just before the MSB truncation which eventually gives the single bit output.

IV. All-Digital PDDS Modulation Schemes

A PDDS core can be easily modified to implement most modulation schemes [6]. FM / FSK modulation (Figure 6) is done by adding a data stream (of relatively small width k and mean value = 0) to the FCW. PM / PSK modulation can also be implemented in a similar simple way by adding the data steam to the output of the Phase Accumulator (just before truncation).

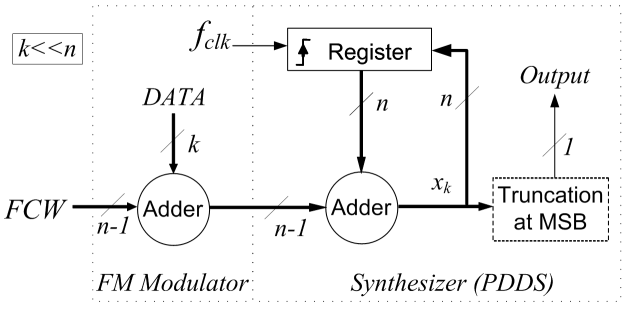

Figure 6. FM modulated PDDS topology

V. 1-BIT OVERSAMPLING ADC

This All-Digital FM Radio transmitter has been designed to be modulated from a digital data stream. The stream can either be directly provided from another system using some digital interface (like from a PC using USB), or created for an external analog audio source (like an mp3 player) using an Analog to Digital Converter. For the purposes of the live demo we selected the second approach.

An ADC is typically a circuit of many analog components (including active ones) and so it doesn't fit well with this All-Digital application. To counter this problem we chose instead to build a nearly All-Digital 1-bit oversampling ADC [7] like that illustrated in Figure 7. This is mostly a digital circuit that only uses a few passive analog components. The analog source is connected to a resistor / capacitor network that in turn interacts with the rest and digitally implemented circuit. The comparator unit can be a simple CMOS inverter. The signal is sampled using a high frequency clock and then it is low pass flittered (using an IIR Filter) to produce the final *k*-bit wide Digital Data stream. This topology is able to sample baseband signals of relative low Bandwidth with high accuracy. Hence it is an ideal method for sampling signals like audio or other analog sensor signals.

VI. IMPLEMENTATION MESURMENTS

This design has been implemented in various FPGA boards. Figure 8 presents the output spectrum of a PDDS implemented in a Xilinx Spartan 3E (of 500k equivalent gates), with and without Dithering. In terms of spurs reduction performance of the dithering technique, these measurements verify the simulation of Figure 4; the output is clear of undesirable spurs. The dynamic range of the Dithered PDDS, defined as the power ratio of the carrier over the noise floor (in dBc/Hz), is significantly higher here compared to that of Figure 4 (~70 vs ~59). This is because of the higher frequency of the f_{clk} signal (200Mhz here vs. 16MHz in Figure 4). The dynamic range is not at the level needed for cell-phones but it is sufficient for relatively sort range, low power RF applications. An ASIC implementation could enable us higher operating frequencies and in turn lower noise floor levels.

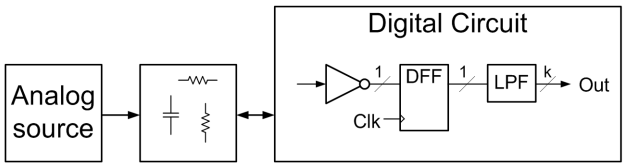

Figure 7. 1-bit oversampling ADC basic topology

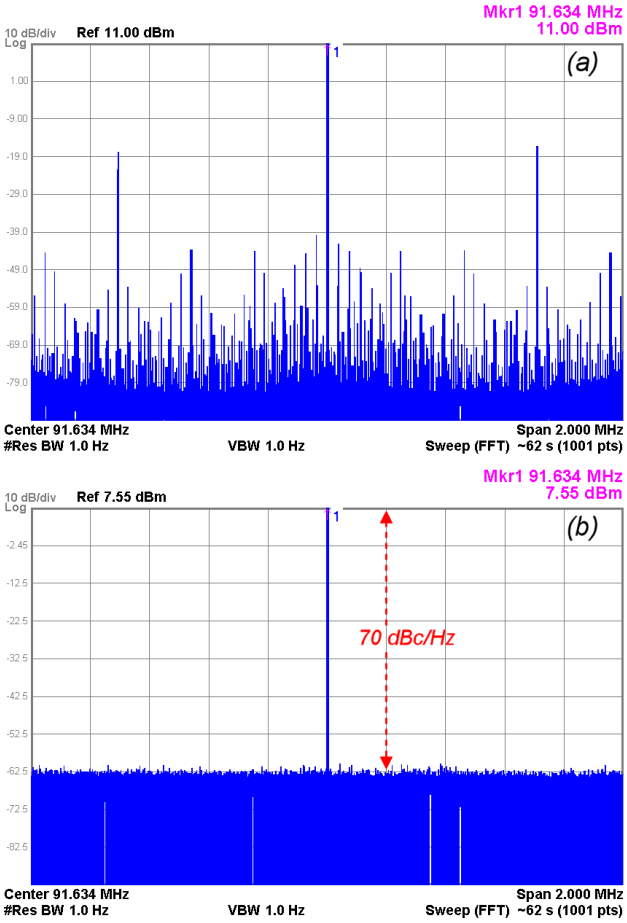

Figure 8. Spectrum mesurments of the implemented Dithered PDDS (f_{clk} = 200Mhz): a) Without Dithering, b) With phase dithering.

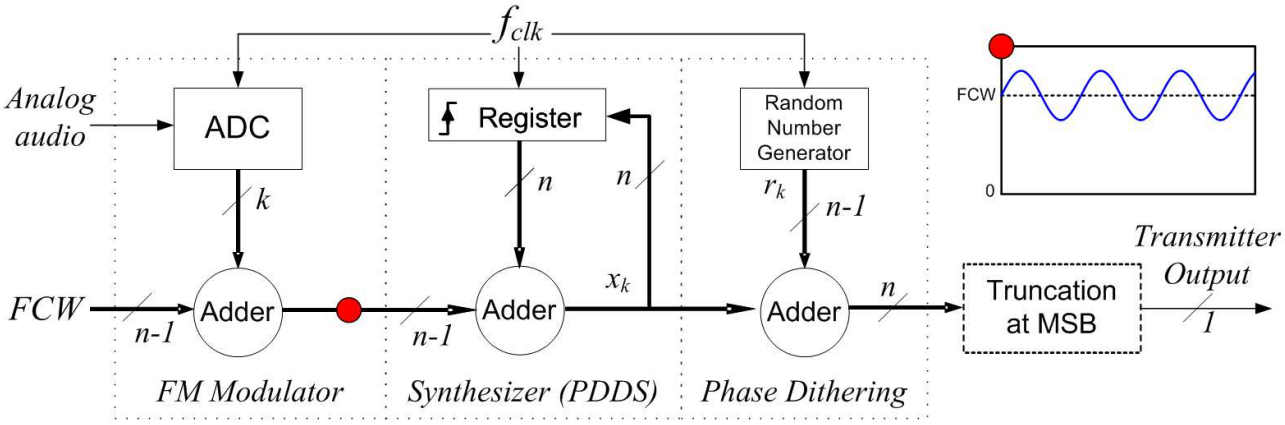

Figure 9. Compete circuit topology of the implemented All-Digital FM Radio transmiter.

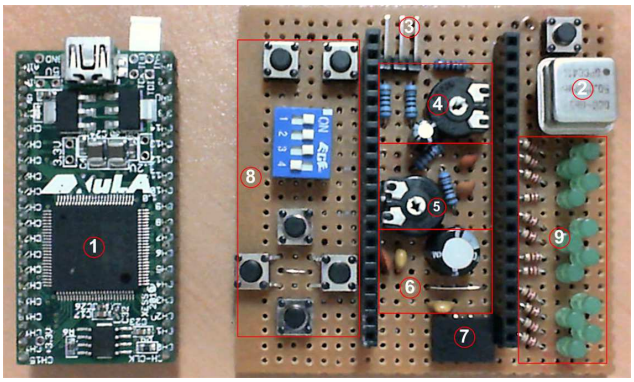

Figure 10. The board builded for the perpouse of the Live Demo

1. Xula-50 mini FPGA Board
2. System clock generator
3. Analog audio input
4. Analog audio handling
5. ADC external analog parts
6. Power decoupling
7. Antenna plug
8. Configuration controls
9. Led Display (configuration and signal power meter)

VII. LIVE DEMO BOARD

A demo board for the purpose of a live demonstration of the proposed architecture has been built as shown in Figure 10. It is based on Xula-50, a mini FPGA board that uses one of the smallest Xilinx FPGA chips of only 50k equivalent gates. The complete circuit topology implemented with this board is shown with Figure 9. The ADC implemented is that of Figure 7. As a result this FM Radio transmitter uses an external analog audio source and it is still implemented within a digital FPGA using only the minor addition of few external analog parts as shown with numbers 4 and 5 in Figure 10. The antenna of the transmitter (a simple wire of about 75cm) is fed with the signal directly from a digital output of the FPGA chip.

The Device utilization for this implementation is presented with Figure 11. Despite using this tiny FPGA chip, the transmitter uses only about 30% of the total available recourses. We should also note that these numbers also include the circuit of the ADC and various other circuits needed for having live reconfigurability and LED display driving. The actual core of the transmitter (Synthesizer, Dithering and modulation) only uses about 10-15% of the available recourses.

FM Radio Demo (with ADC and controls)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	336	1,408	23%
Number of 4 input LUTs	349	1,408	24%
Number of occupied Slices	258	704	36%

Figure 11. Device utilization of the tramsiter implementation.

VIII. CONCLUSIONS

A versatile purely digital FM transmitter architecture, that results in minimum chip-area, low-power and low-cost implementations, has been presented. It includes a nearly all-digital ADC to support both analog and digital modulation schemes. Measurements have demonstrated a dynamic range of about 70dBc/Hz.

REFERENCES

[1] Robert B. Staszewski, Poras T. Balsara, “All-Digital Frequency Synthesizer in Deep-Submicron CMOS”, Wiley-Interscience, 2006.

[2] J. Tierney, C. M. Radar, and B. Gold, A digital frequency synthesizer, IEEE Trans. Audio Electroaccoustics, vol. 19, pp. 48–57, Mar. 1971.

[3] V.S. Reinhardt, “Direct digital synthesizers”, Technical Report, Hughes Aircraft Co, Space and Communications Group, L.A., CA, Dec. 1985.

[4] Paul P. Sotiriadis, Kostas Galanopoulos, "Direct All-Digital Frequency Synthesis techniques, Spurs Suppression and Deterministic Jitter Correction", to appear in the IEEE Trans. on Circuits and Sys.-I.

[5] C. E. Wheatley, III and D. E. Phillips, “Spurious suppression in direct digital synthesizers,” in Proc. 35th Freq. Control Symp., May 1981, pp. 428–435.

[6] Earl W. McCune, Jr., “Number controlled modulated oscillator”, US Patent 4,746,880, filled: Feb 6, 1987

[7] F. Wang and R. Harjani, “Design of Modulators for Oversampling Converters”, Kluwer Academic Publishers, 1998.