A 60 GHz -1.2 Volt Receiver in a 90nm CMOS RF Technology

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Abstract—**In this paper the design of a high-data-rate receiver in the 60 GHz band using a QPSK modulation scheme is presented. The channel bandwidth is 1 GHz in order to achieve gigabit Ethernet wireless transmission at 1km distance. The receiver has 66 db of linearly controlled gain with a noise figure of 8 dB. The circuit consumes 620 mA from a 1.2 V power supply**.

I. INTRODUCTION

The evolution of new CMOS technologies that provide the IC designers with devices of improved performance has made feasible the design of the most demanding circuits [1]. Reducing the gate length of MOSFETS, results in the increase of unity gain frequency and the decrease of supply voltage. Taking this into account, the design of 60 GHz transceivers has been investigated.

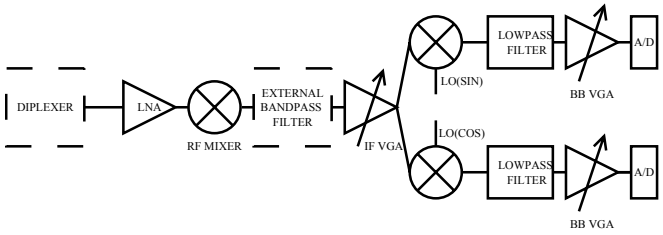

Figure 1 Block diagram of the receiver

In this paper the design of a (raw) 1GBps backhaul receiver is presented. The receiver uses a QPSK modulation scheme and a signal-bandwidth of 1 GHz. In order to achieve the aforementioned specifications, the receiver must have 60 dB of controllable gain and 12 dB of noise figure, assuming 40 dB of gain from the antenna. The system is integrated in a 90 nm CMOS technology.

In Fig.1 we see the architecture of the receiver. Between the antenna and the circuits, there is a diplexer that acts also as waveguide filter. That filter has the performance of a 5th order Chebyshev filter with an insertion loss of 2 dB. Moreover two PLLs are used to provide the necessary frequency signals to the RF and IF mixers. This allows for good flexibility in channel selection and frequency planning. Although the paper does not focus on the RF PLL is worth mentioning that it achieves a phase noise of -91 dBc/Hz at 60 GHz at 1MHz offset frequency with a differential output of 70 mVp at 50 Ohm.

In sections II and III the receiver and the IF PLL are analyzed respectively. In section IV simulation results are shown demonstrating the performance of the system.

II. THE RECEIVER

The receiver consists of three major systems. The RF front–end (RFFE), the IQ demodulator and the base-band section. It has a standard heterodyne architecture with two stages of down conversion. The first one is from the region of 60 GHz to 5.7 GHz and the second one to base-band. In order to achieve this, the two PLLs (RF & IF one) are centered at 54.3 and 5.7 GHz respectively.

Fig.1 shows the architecture of the receiver with the the low noise amplifier and the RF mixer at the beginning of the chain. We chose not to use image rejection RF mixer, since we have a waveguide filter at the input, which guarantees at least 60 dB of image rejection. Taking this into account we use a simple passive single balanced mixer with minimum capacitive loading at the output of the Low Noise Amplifier (LNA).

The LNA is a cascade of three stages. The first two stages have a common source topology, biased for optimum noise figure and gain respectively [2]. The third stage is a common gate amplifier, which provides isolation between the input and the output. Each stage is tuned and conjugate-matched to the next one using strip line components denoted as CPW1 to CPW5 in Fig.2.

The mixer consists of a tuned passive single balanced switching pair which allows us to attenuate the LO feed-through at the output which could desensitize the following stages of a receiver. A common drain buffer is also used in order to drive the 50 Ohm external band pass filter with the use

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of a custom made balun. In Fig.2 we see the schematic of the whole RFFE.

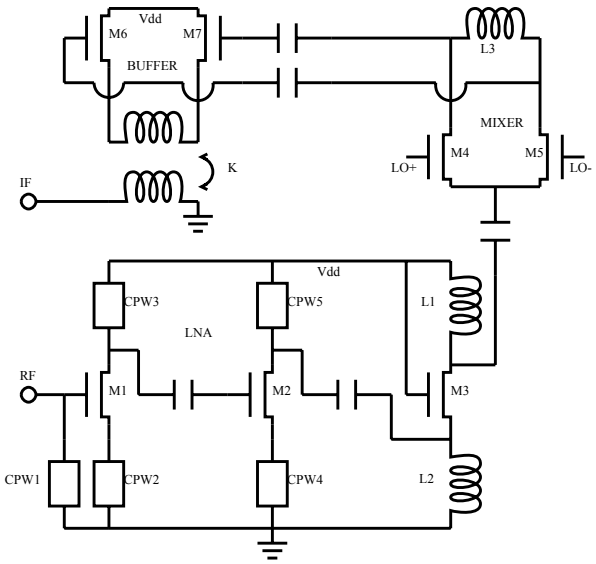

Figure 2. The RFFE

A variable gain amplifier (VGA) and the IQ demodulator follow the external filter. The core amplifier has a cascode topology with positive feedback [3] and the IQ mixer consists of two passive mixers driven by a quadrature LO signal. The two circuits are merged in order to minimize parasitics. The gain of the circuit should vary from 12.5 to -2.5 dB with the use of a ladder attenuator at the input. Taking into account that we use passive mixing maximum linearity performance results. In this case, the use of passive switching pairs is essential because the signal is down-converted to base-band and we have to minimize flicker noise.

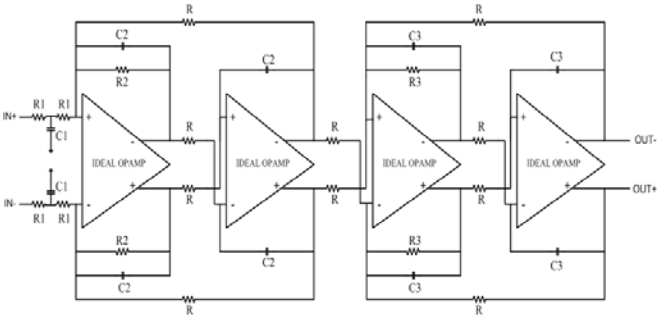

Figure 3: The 5th order filter

In each branch of I and Q signals a fifth-order 0.5 dB ripple Chebyshev active-RC LPF has been used. The 1-dB cut of frequency is at 500 MHz and the gain of the filter is 3 dB. In order to achieve this performance, a first order RC filter is used at the input that is followed by two cascaded Tow-Thomas biquads. In addition, common drain buffers are used at the input and the output. The filter is trimmable with digital control for process variations [4].

The optimum feasible gain-bandwidth product of the operational amplifier is calculated to be 25Grads/sec. This corresponds to about 30dB open-loop low frequency gain (A_0) and 4 GHz unity gain frequency (f_T) for the operational amplifier. To avoid potential instability due to complex dynamic behavior of the filter, we chose to use single-stage, folded cascode OTA architecture with output capacitance compensation, followed by a unity gain buffer [5].

The filter is followed by a second VGA. The gain of which varies from 8 to 36 dB with a flat bandwidth of 500 MHz. This performance is achieved with the use of three open – loop cascaded amplifiers and two resistor ladders. Each one of the amplifiers consists of a NMOS differential pair with PMOS active loads and a common-mode feedback circuit which stabilizes the output bias voltage at 600 mV. This characteristic is essential for the correct operation of the receiver because we can not use ac coupling and each amplifier biases the next one.

III. THE PLL

The architecture of the frequency synthesizer is shown in the diagram below. According to this, the local oscillator signal is twice the frequency than needed, at 11.4 GHz. Then, and after passing through a buffer amplifier, the signal is fed to a divider by 2, which reduces the frequency to the desired value and simultaneously generates a 4-phase I and Q signal. This signal is routed to a buffer, which is connected to the final amplifier in each mixer. The signal generated by the composer, has to be a compressed sine with at least 300 mv amplitude for each component I and Q.

Before the signal enters the divider by 2, it also goes through a divider by 16, so that the signal frequency becomes less than 1 GHz. This region is within the operating range of available (to us) digital circuits, and we can process the signal in the digital phase detector. After the detector, there is a charge pump that uses an external filter, to close the loop and lock the frequency at the output of the PLL.

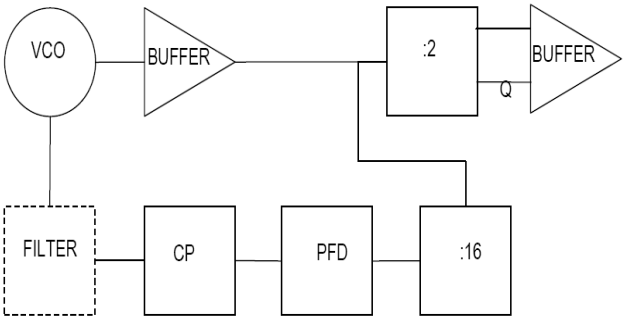

Figure 4: Architecture of the IF PLL

The topology we chose for the oscillator is a cross coupled pair with an LC resonance. In order to control the oscillation frequency, we used two analog and six digitally-controlled varactors. In this way we can have large frequency steps by switching on and of the digitally controlled capaciors and we can calibrate the final frequency with the varactors.

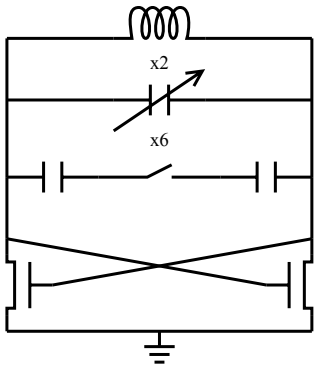

Figure 5. The core circuit of the VCO

One of the most important circuits of the PLL, is the divider generating the IQ signal for the IQ demodulator. It consists of two pairs of latches and amplifiers operating in a reverse way in each half of the clock controlling them. At each time moment the amplifier of the one pair and the latch of the other one are active. The operation flips according to the value of the clock.

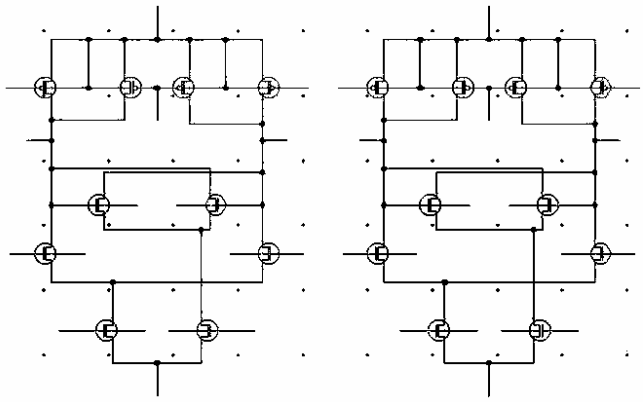

Figure 6: The frequency divider

IV. SIMULATION RESULTS

The circuits were simulated including extracted layout parasitics and models for the bond wires and the ESDs. The integrated circuit will be bonded directly to the PCB with ribbon bond wires and therefore we assumed a parastic inductance of 200 nH for each bond wire.

In the next figure we see the gain and the noise figure of the whole RFFE. The gain is almost stable from 58.5 to 61.2 GHz with a value of 14 dB. The noise figure varies from 7.4 to 7.8 in the same region. If we take into account that the RFFE is the major noise contributor of the receiver, it is obvious that the noise of the system including the diplexer will not exceed 10 dB.

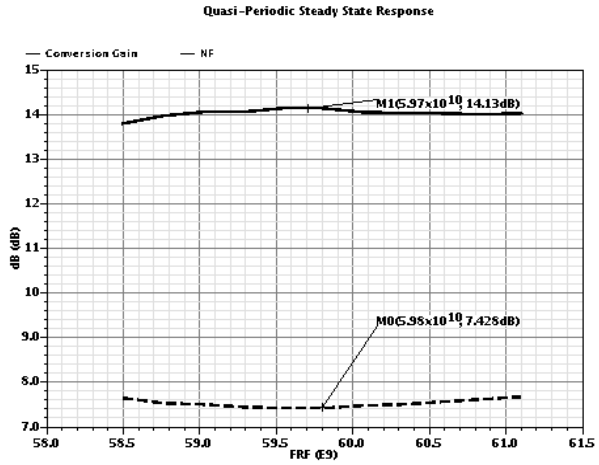

Figure 7. Noise figure and Conversion Gain of the RFFE

More over, we measured input and output matching of the circuit at 60 and 5.7 GHz respectively. The return loss at the input is about -15 dB and the one at the output is about -10 dB. The isolation between the RF and the LO input is 65 dB. These characteristics are essential because the passive mixer we use requires -5 dBm of LO power in order to achieve low noise performance.

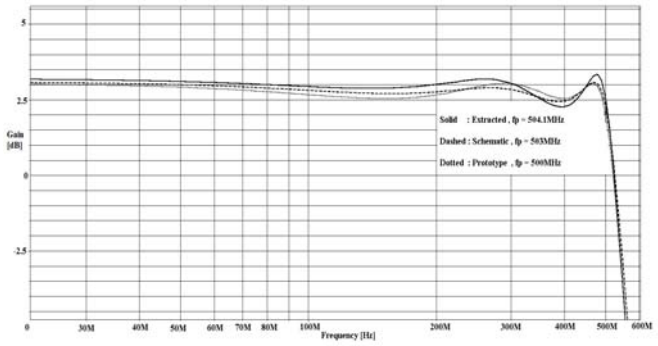

Figure 8: Frequency response of the filter

In Fig. 8 we see the frequency response of the low pass filter. In detail we can see the graph that corresponds to the ideal prototype, the design that was implemented with the folded cascode OTA's and the performance of the filter with the extracted parasitics from the layout. All the three plots are very close to each other and there are only negligible differences in ripple.

We also simulated the VGA, the IQ demodulator, the low pass filter and the base band amplifier of the receiver altogether, to measure the gain and the bandwidth. Assuming a 200 ohm differential load at the output of the base band amplifiers, the maximum gain is 64 dB and the 3-dB bandwidth exceeds 500 MHz. Taking into account that we matched the input at 50 Ohms, this results to a power gain of 58 dB for the receiver.

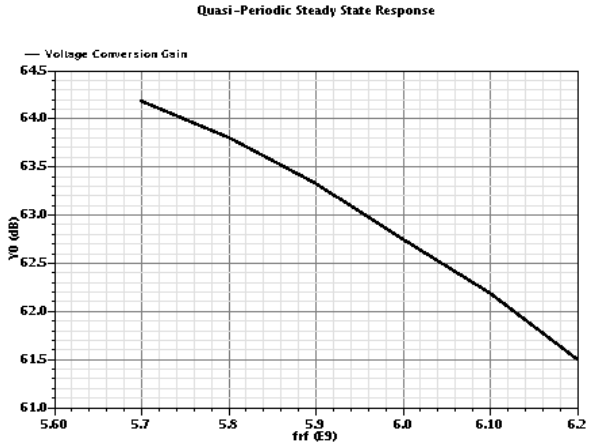

Figure 9. IF and Baseband Voltage Conversion Gain

In Fig. 10 the differential IQ outputs of the PLL are displayed. We can see that their waveform is a clipped sinusoid with a peak value of almost 450 mV. Those signals are going to be further amplified by limiters at the input of the mixer in order to have a final peak voltage of around 1 Volt. In passive mixers, such as the ones we adopted in the IQ demodulator, it is very important to have a strong LO signal because it minimizes noise, flicker and thermal and it maximizes linearity.

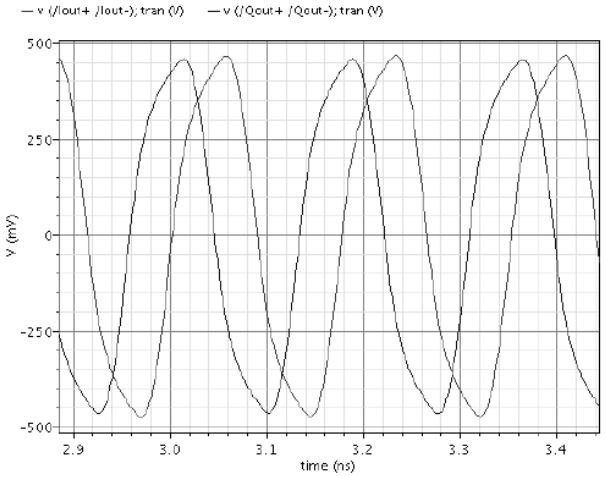

Figure 10: Output of the PLL

V. CONCLUSIONS - DISCUSSION

In this paper the design of a 60 GHz receiver was presented. Emphasis was given in the design of the RFFE and the PLL since they are the most challenging circuits. Simulation results, including extracted parasitics, prove that it is feasible to satisfy all the necessary specifications if we use an advanced technology with a f_T of 100 GHz.

REFERENCES

[1] Behzad Razavi, "A 60 – Ghz CMOS Receiver Front - End", IEEE Journal of Solid State Circuits, vol. 41, No. 1, pp. 17 – 22, Jan. 2006.

[2] Terry Yao, Michael Q. Gordon, Keith K. W. Tang, Kenneth H. K. Yau, Ming –Ta Yang, Peter Schvan and Sorin P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60 – GHz Radio", IEEE Journal of Solid State Circuits, vol. 41, No. 1, pp. 17 – 22, Jan. 2006.

[3] H-H. Hsieh and L-H Lu, "A 40-GHz low-noise amplifier with a positive-feedback network in 0.18-um CMOS,'' IEEE Trans. Microwave Theory Tech, vol. 57, no. 8, pp.1895-1902, Aug. 2009.

[4] A.Vasilopoulos,G.Vitzilaios,G.Theodoratos,Y.Papananos, "A Low-Power Wideband Reconfigurable Integrated Active-*RC* Filter With 73 dB SFDR,IEEE JSSC,vol. 41,NO. 9,September 2006

[5] Sudhir Mallya and Joseph Nevin, "Design Procedures for a fully Differential Folded-Cascode CMOS Operational Amplifier" ,IEEE JSSC,vol. 24,NO. 6,December 1989