An All-Digital Transmitter Live Demo

Introduction

RF transceivers are some of the few remaining analog-intensive super-blocks in modern Systems-On-Chips. Designing their RF/analog blocks, in contrast to digital blocks, requires significant amount of effort and time due to limited automation and porting capability in the design process. In addition, RF sub-blocks may require advanced fabrication technologies which are much more expensive than standard CMOS ones. Over the past decades, major effort has been dedicated in replacing many analog blocks by digital ones, e.g. frequency synthesizers and base-band signal processors, resulting in dramatic improvements in both cost and functionality.

An All-Digital Transmitter demo has been setup to operate on the FM radio band and be modulated by audio signal generated from an external source.

Pulsed Direct Digital Synthesizer

The core of the transmitter is a Pulsed Direct Digital Synthesizer (PDDS) [1]. It consists of an phase accumulator (of n bits wide), the Most Significant Bit of which is used as the output. This digital 0/1 out (RF) signal can be used to drive a highly efficient on/off RF power amplifier or directly drive a narrow-band antenna via the output digital inverter of the PDDS. The carrier frequency of the PDDS output, based on the clock frequency forkl, is set by an input Frequency Control Word (FCW n bits wide) and can range within (0, fclk/2) with very high resolution.

Output timing irregularities:

Output timing irregularities: fundamental output period

Output timing irregularities: average output period

Output Jitter and spurs performance

The PDDS is a synchronous FSM so output only changes its value at the rising edges of the system clock. As a result the output has timing irregularities (deterministic jitter) for most generated frequencies. This deterministic jitter is always less or equal to ½ Clock Cycle. These timing irregularities also cause strong undesirable spurs on the frequency domain.

Spurs reduction using Dithering

Basic Dithered PDDS topologies

Frequency dithering: A random sequence is added to the FCW.

Random Number Generator

For this demo an advanced type of random phase dithering is used to totally suppress the otherwise strong unwanted frequency spurs of the single-bit output of the PDDS. The algorithms are available for licensing.

Real Implementation measurements (clk=200MHz)

Without dithering: With dithering:

A~70dBc/Hz Noise Floor is Achieved.

1bit oversampling S/D ADC and the demo board

A versatile All-Digital transmitter architecture for low power, small area and low cost implementations has been setup to operate on the FM radio band and be modulated by audio signal generated from an external source.

Conclusions and Future Work

A versatile All-Digital transmitter architecture for low power, small area and low cost implementations has been presented with all of its components (frequency synthesizer, Modulator, ADC for analog Audio Data acquisition) implemented in a single FPGA chip (Xilinx Spartan 3A of 50k equivalent gates). It demonstrates a versatile architecture which can be implemented in digital FPGA or ASICs, providing an alternative to popular analog RF ones and offering extremely fast concept-to-market time, low cost, minimal chip-area and power requirements while achieving performance, adequate for many modern wireless applications. This architecture can be easily modified to accommodate most of the commonly used modulation schemes (PM, AM, QAM, BPSK, QPSK etc.) as well as to operate in any desirable frequency band supported by the FPGA or ASIC technology used.

For the purposes of the demo and due to the limitations of the particular FPGA board (maximum operating frequency: fclk = 200MHz), the transmitter has been set to operate on the FM radio band and be modulated by audio signal generated from an external source.

References: