All-Digital Transmitter

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An All-Digital Transmitter Live Demo

Introduction

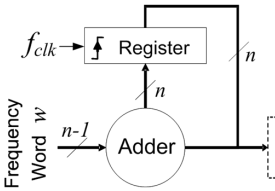
RF transceivers are some of the few remaining analog-intensive super-blocks in modern Systems-On-Chips. Designing their RF/analog blocks, in contrast to digital blocks, requires significant amount of effort and time due to limited automation and porting capability in the design process. In addition, RF sub-blocks may require advanced fabrication technologies which are much more expensive than standard CMOS ones. Over the past decades, major effort has been dedicated in replacing many analog blocks by digital ones, e.g. frequency synthesizer and base-band signal processors, resulting in dramatic improvements in both cost and functionality.

An All-Digital Radio transmitter demo is presented with all of its components (frequency synthesizer, Modulator, ADC for analog Audio Data acquisition) implemented in a single FPGA chip (Xilinx Spartan 3A of 50k equivalent gates). It demonstrates a versatile architecture which can be implemented in digital FPGA or ASICs, providing an alternative to popular analog-RF ones and offering extremely fast concept-to-market time, low cost, minimal chip-area and power requirements while achieving performance, adequate for many modern wireless applications. This architecture can be easily modified to accommodate most of the commonly used modulation schemes (PM, AM, QAM, BPSK, FSK, QPSK etc.) as well as to operate in any desirable frequency band supported by the FPGA or ASIC technology used.

For the purposes of the demo and due to the limitations of the particular FPGA board (maximum operating frequency: fclk = 200Mhz), the transmitter has been setup to operate on the FM radio band and be modulated by audio signal generated from an external source.

Pulsed Direct Digital Synthesizer

The core of the transmitter is a Pulsed Direct Digital Synthesizer (PDDS) (an all-digital frequency synthesizer [1]). It consists of an phase accumulator (of n bits wide), the Most Significant Bit of which is used as the output. This digital 0/Vdd output (RF) signal that can be used to drive a highly efficient on/off RF power amplifier or directly drive a narrow-band antenna via the output digital inverter of the FPGA. The carrier frequency of the PDDS's output, based on the clock frequency fclk, is set by an input Frequency Control Word (FCW n-1 bits wide) and can range within (0 , fclk/2) with very high resolution.



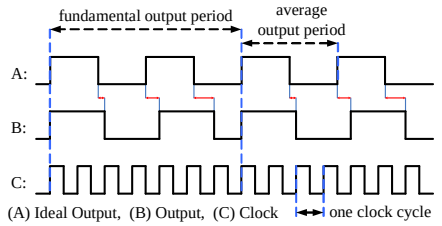
$$f_{ave} = \frac{w}{2^N} \cdot f_{clk}$$

$$f_{fund} = \frac{\gcd(w, 2^N)}{2^N} \cdot f_C \le f_{ave}$$

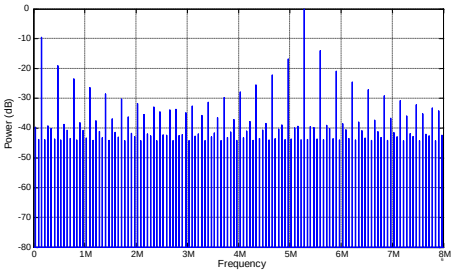
Output Jitter and spurs performance

The PDDS is a synchronous FSM so output only changes its value at the rising edges of the system clock. As a result the output has timing irregularities (deterministic jitter) for most generated frequencies. This(deterministic) Jitter is always less or equal to ½ Clock Cycle. These timing irregularities also cause strong undesirable spurs on the frequency domain.

Output timing irregularities:



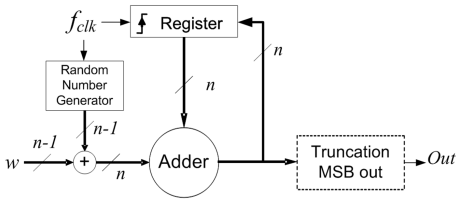
Output Spectrum:



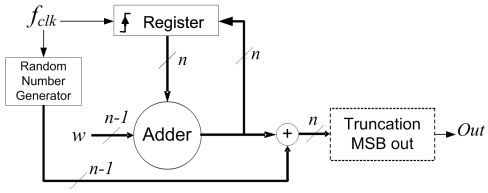
Spurs reduction using Dithering

Basic Dithered PDDS topologies

Frequency dithering: A random sequence is added to the FCW.

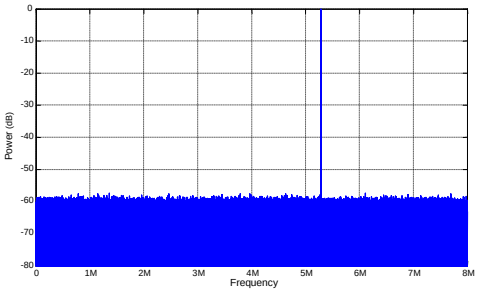


Frequency dithering: A random sequence is added to the Output of the Phase Accumulator (before truncation).



Random Number Generator

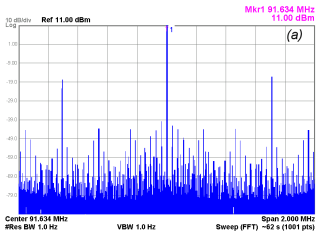
For the demo an advanced type of random phase dithering is used to totally suppress the otherwise strong unwanted frequency spurs of the single-bit output of the PDDS. The algorithms are available for licensing.



As we can see the output is now free of spurs but has an elevated noise floor.. This is a Matlab simulation using a 16Mhz System Clock. The Noise floor actually decreases as a higher system clock is used.

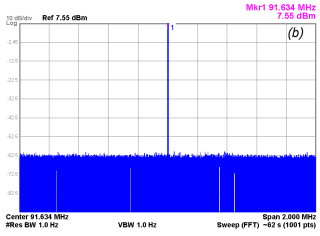
Real Implementation measurements (clk=200Mhz)

Without dithering:



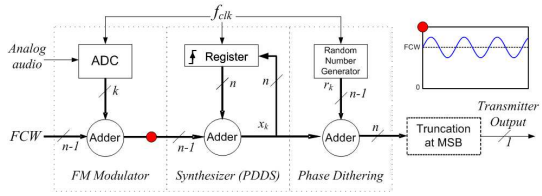
With dithering:

A **~70dBc/Hz** Noise Floor is Achieved.

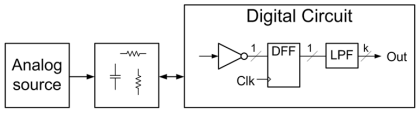


1bit oversampling S/D ADC and the demo board

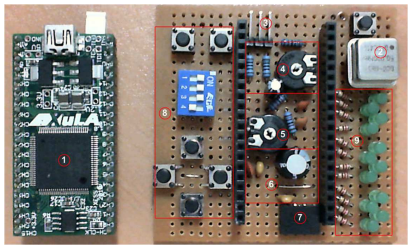
Complete Block diagram of the demo



FM modulation is done by adding signed data to the FCW. Any ADC could be used, but we preferred a nearly All-Digital 1bit oversampling ADC. Its better fitted for this All-Digital application as it uses only a few external Rs & Cs analog components .



The Demo Board



1) Xula-50 mini FPGA Board
2) System clock generator
3) Analog audio input
4) Analog audio handling
5) ADC external analog parts
6) Power decupling
7) Antenna plug
8) Configuration controls
9) Led Display

Device utilization

FM Radio Demo (with ADC and controls)			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	336	1,408	23%
Number of 4 input LUTs	349	1,408	24%
Number of occupied Slices	258	704	36%

Conclusions and Future Work

A versatile All-Digital transmitter architecture for low power, small area and low cost implementations has been presented. At this point we mainly focus on low power, short range applications.

Our team works on new architectures to:

- Further reduce the noise floor of the output.
- Increase the maximum operating frequency.
- Implement an All-digital receiver in order to offer a complete all-digital transceiver solution.

References :

- P. Sotiriadis, "Spurs Suppression and Deterministic Jitter Correction in All-Digital Frequency Synthesizers, Current State and Future Directions", IEEE International Symp. on Circuits and Systems 2011.
- Paul P. Sotiriadis, Kostas Galanopoulos, "Direct All-Digital Frequency Synthesis techniques, Spurs Suppression and Deterministic Jitter Correction", to appear in the IEEE Trans. on Circuits and Systems-I.
- V.S. Reinhardt, "Direct digital synthesizers", Technical Report, Hughes Aircraft Co, Space and Communications Group, L.A., CA, Dec. 1985.
- C. E. Wheatley, III, "Digital Frequency Synthesizer with Random Jittering for Reducing Discrete Spectral Spurs", U, S. Patent 4,410,954, October 18, 1983.
- V.F. Kroupa Direct Digital Frequency Synthesizers, 1998, Wiley-IEEE Press.