Design of a 1.2-V 60 GHz Transceiver in a 90nm CMOS RF Technology

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Abstract—**In this paper the design of a high-data-rate transceiver in the 60 GHz band using a QPSK modulation scheme is presented. The channel bandwidth is 1 GHz in order to achieve gigabit Ethernet wireless transmission at 1km distance. The receiver has 66 db of linear controlled gain with a noise figure of 8 dB. The transmitter is capable of delivering -12 dBm of power at the external power amplifier. Both circuits operate under a 1.2 V power supply**.

I. INTRODUCTION

The evolution of new CMOS technologies that provide the IC designers with devices of improved performance has made feasible the design of the most demanding circuits [1]. Reducing the gate length of MOSFETS, results in the increase of unity gain frequency and the decrease of supply voltage. Taking this into account, the design of 60 GHz transceivers has to be investigated.

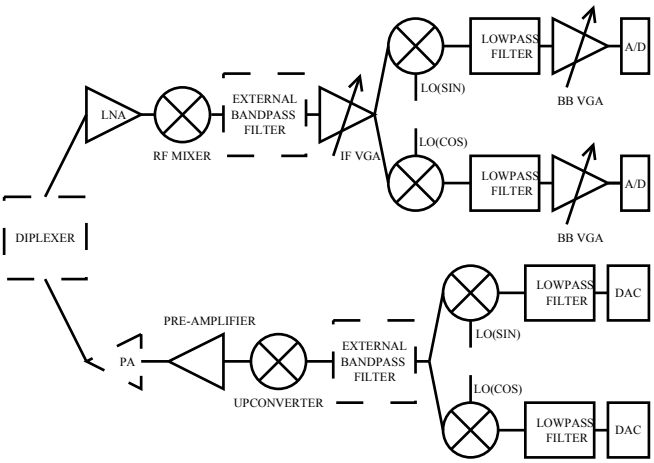

Figure 1 Block diagram of the transceiver

In this paper the design of a 1GBps backhaul transceiver will be analyzed with a radius of 1 km. The transceiver uses a QPSK modulation and therefore the signal spectrum has to be 1 GHz. In order to achieve the aforementioned specifications, the receiver must have 60 dB of controllable gain and 12 dB of noise figure, assuming 40 dB of gain from the antenna. The transmitter has to deliver 12 dBm of power. The system will be integrated in a 90 nm CMOS technology.

In Fig.1 we can see the architecture of the whole system. Between the antenna and the circuits, there is diplexer that acts also as waveguide filter. That filter has the performance of a 5th order Chebyshev filter with an insertion loss of 2 dB. More over a high and a low frequency PLL are used from the receiver and the transmitter for frequency synthesis of the necessary local oscillator signals. This ensures maximum flexibility in channel selection and frequency planning. Even though those circuits will not be further analyzed, it must be mentioned that the high frequency PLL achieves a phase noise of -91 dBc/Hz at 60 GHz, and a differential output swing of 70 mV at 50 Ohm.

In sections II and III the receiver and the transmitter will be analyzed respectively. In section IV simulation results will be displayed that verify the performance of the system. Finally in section V conclusions will be derived.

II. THE RECEIVER

The receiver consists of three major systems. The RF front – end (RFFE), the IQ demodulator and the base band. Its architecture is quite simple since it uses two down conversions. The first one is from the region of 60 GHz to 5.7 GHz and the second one to base band. In order to achieve that it demands two PLLs at 54.3 and 5.7 GHz for each down conversion respectively.

In Fig.1 we can see the architecture of the receiver. In the beginning we can see the low noise amplifier and the mixer. We decided not to use image rejection mixing, since we have a waveguide filter at the input, which ensures at least 60 dB of attenuation for the image. Taking that into account we can use a very simple passive single balanced mixer with minimum capacitive loading at the output of the Low Noise Amplifier (LNA).

The LNA is a three stage structure. The first two stages have a common source topology, biased for optimum noise performance and gain respectively [2]. The third stage is a common gate amplifier, which provides isolation between

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the input and the output. Each stage is tuned and conjugate matched with the next one, by using strip line components denoted as CPW1 to CPW5 in Fig.2.

The mixer is consisted of a tuned passive single balanced switching pair. In this way we can attenuate the LO feed through at the output that could desensitize the following stages of a receiver. A common drain buffer is also utilized in order to drive the 50 Ohm external band pass filter with the use of a custom made balun. In Fig.2 we can see the schematic of the whole RFFE.

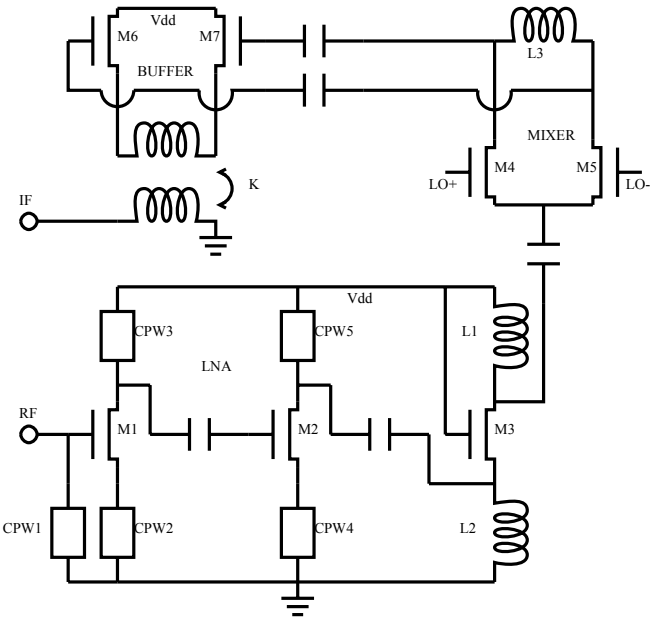

Figure 2. The RFFE

After the external filter there is a variable gain amplifier (VGA) and the IQ demodulator. The core amplifier has a cascode topology with positive feedback [3] and the IQ mixer consists of two passive mixers driven by a quadrature LO signal. The two circuits are merged in order to minimize parasitics. The gain of the circuit should vary from 12.5 to -2.5 dB with the use of a ladder attenuator at the input. This ensures maximum linearity performance, if we also take into account, that we use passive mixing. In this case, the use of passive switching pairs is essential because the signal is down converted to base band and we have to minimize flicker noise.

In each branch of I and Q signals a fifth-order 0.5 dB Chebyshev active-RC LPF has been used. The 1-dB cut of frequency is at 500 MHz and the gain of the filter is 3 dB. In order to achieve this performance, a first order RC filter is used at the input that is followed by two cascaded Tow-Thomas biquads. In addition, common drain buffers were used at the input and the output. The filter is trimmable with digital control for process and temperature variations [4].

The optimum feasible gain-bandwidth product of the operational amplifier is calculated to 25Grads/sec.This corresponds to 30dB open-loop low frequency gain (A_0) and 4 GHz unity gain frequency (f_T) for the operational amplifier. We implemented this with a folded cascode operational transconductance amplifier topology followed by a source-follower output buffer [5].

The filter is followed by a second VGA and the A/D. The gain of the amplifier varies from 8 to 36 dB with a flat bandwidth of 500 MHz. This performance is achieved with the use of three open – loop cascaded amplifiers and two resistor ladders.

A 6-bit 850-MS/s Flash ADC bridges the RF Analog Front End and the base band, on the receiver side. The ADC consists of a reference voltage ladder, 64 comparators followed by a D-Flip-Flop and a thermal-to-binary. The block diagram of the comparator is shown in Fig.3.

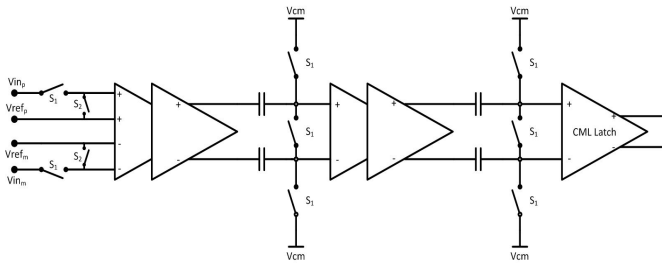

Figure 3. Block diagram of the A/D comparator

To minimize the offset of the comparator, a set of switches are utilized [7]. While at phase S_1 the amplified input signal is sampled by the first set of capacitors. At the same time the other set of capacitors samples the output offset of the second amplifier stage. At phase S_2 the sampled voltage is shifted by the amount of offset of the first amplifier, effectively eliminating it, while the second stage further amplifies the output voltage. This switching scheme, advantageous to other "output offset autozeroing" found in literature, accomplishes elimination of the comparator offset, while in the same time samples and holds the input signal, thus increasing the A/D converter high speed specifications.

III. THE TRANSMITTER

The architecture of the transmitter is displayed in Fig.1. After the DAC we have a low pass filter similar to the one in the receiver and the IQ modulator. The signal is up converted to 5.1 GHz and is fed to an external band pass filter. After the filter we have the up converter and the pre-amplifier. At the output an external power amplifier is used with 24 dB of gain and CP1 at the output of 17 dBm. The transmitter uses two PLLs similar to the ones of the receiver.

An 8-bit 850-MS/s Segmented Current Steering DAC acts as a bridge between the baseband and the RF Analog Front End on the transmitter side. It consists of a binary-to-thermal decoder, the current sources, the current switches and their drivers as displayed in Fig4. The 8-bit input code is segmented in two parts improving the DNL of the converter. The 4 most significant bits (MSB) are converted into a 16-bit thermometer code, while the 4 least significant bits (LSB) are processed through a delay circuit equating the delay

between the segmented bits. The switch driver consists of a Current Mode Logic (CML) Master-Slave Flip-Flop followed by a driver circuit.

The analog part of the converter consists of the current sources and the current switches. For a good performance at high frequencies, a high output impedance switch is necessary. This is achieved using cascode current sources, switches and minimizing the capacitance of the output node

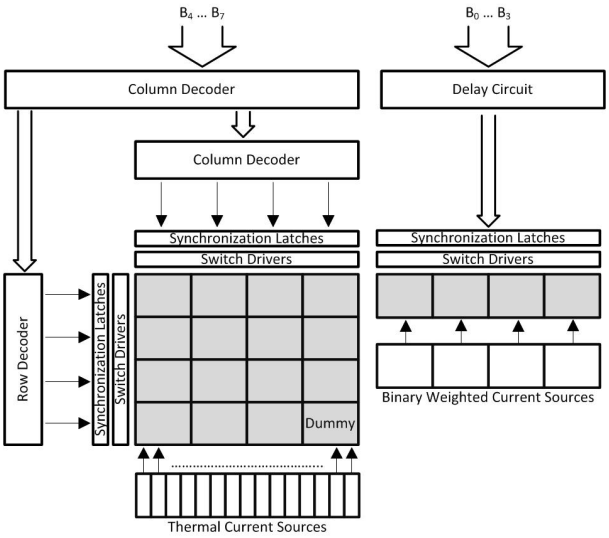

Figure 4. Architecture of the DAC

For the IQ modulator we used two double balanced mixers that were driven by a quadrature LO signal. Their outputs were combined to modulate the signal. We sized the transistors properly, to have low output impedance and we used a custom made balun to have a single ended output. The circuit has 5 db of conversion loss and an input compression point of 1 dBm.

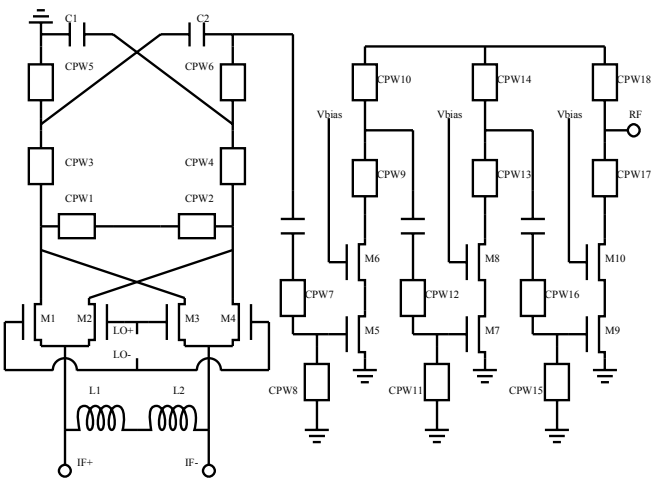

Figure 5. The upconverter with the preamplifier

In Fig.3 the schematic of the up converter and the pre-amplifier is displayed. The up converter is a passive ring mixer with differential input for the IF and the LO signal. The output is single ended and it drives the pre-amplifier. The input is matched at 100 Ohms.

The pre amplifier is a three stage amplifier. Each stage has a cascode topology for maximum isolation between the input and the output and is designed for optimum linearity [2]. We used strip lines to tune the circuit and we can vary its gain by changing the bias voltage of the cascade transistors

IV. SIMULATION RESULTS

The circuits of the two systems were simulated including extracted layout parasitics and models for the bond wires and the ESDs. The integrated circuit will be bonded directly to the PCB with ribbon bond wires and therefore we assumed a parastic inductance of 200 nH for each bond wire.

In the next figure we can see the gain and the noise figure of the whole RFFE. The gain is almost stable from 58.5 to 61.2 GHz with a value of 14 dB. The noise figure varies from 7.4 to 7.8 in the same region. If we take into account that the RFFE is the major noise contributor of the receiver, it is obvious that the noise of the system including the diplexer will not exceed 10 dB.

More over, we measured input and output matching of the circuit at 60 and 5.7 GHz respectively. The return losses at the input are about -15 dB and at the output -10 dB. The isolation between the RF and the LO input is 65 dB. This characteristic is essential, because the passive mixer we use requires -5 dBm of LO power in order to achieve low noise performance.

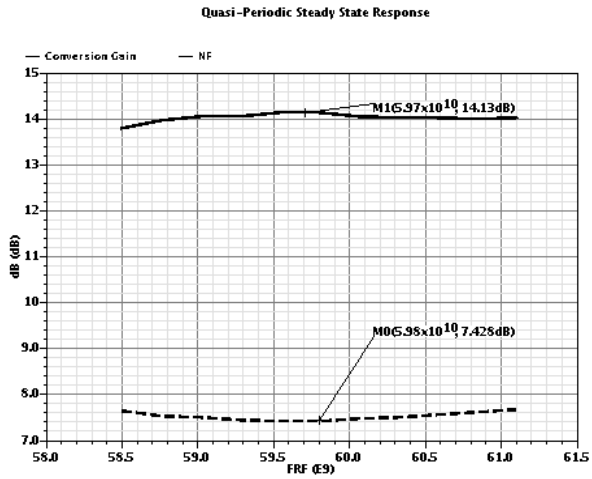

Figure 6. Noise figure and Conversion Gain of the RFFE

We also simulated the VGA, the IQ demodulator, the low pass filter and the base band amplifier of the receiver altogether, to measure the gain and the bandwidth. Assuming a 200 ohm differential load at the output of the base band amplifiers, the maximum gain is 64 dB and the 3-dB bandwidth exceeds 500 MHz. Taking into account that we matched the input at 50 Ohms, this results to a power gain of 58 dB.

Finally the A/D converter achieved 33dB SNR and 43dB SFDR for 400Mhz input signal and 1.7GHz clock, while the sigma of the comparator reaches 1.6mV.

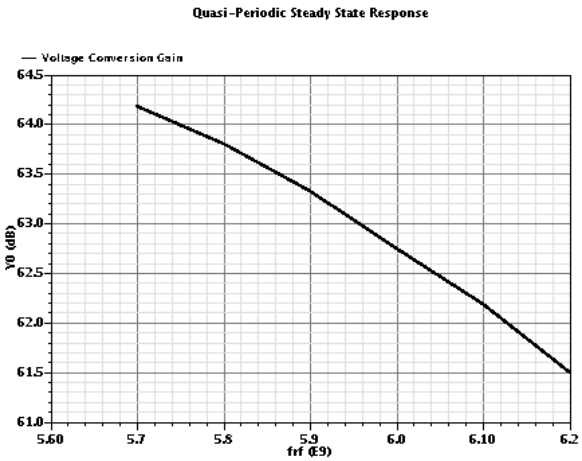

Figure 7. IF and Baseband Voltage Conversion Gain

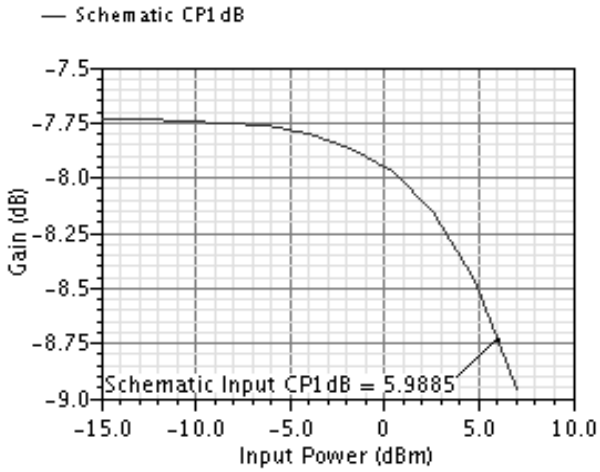

Figure 8: Power gain of the upconverter

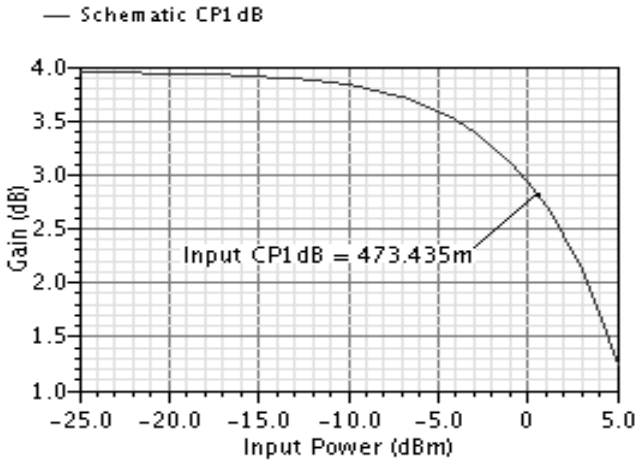

Figure 9: Gain for each stage of the pre - amplifier

The most challenging circuits of the transmitter are the upconverter and the pre – amplifier. In Fig. 8 we can see that the conversion loss of the upoconverter is 7.7 dB and it has an input compression point of 6 dBm. The mixer demands 0 dBm of LO power. More over isolation between the ports of the mixer exceeds 40 dB.

According to simulation results displayed in Fig.9, each one of the three stages of the preamplifier achieves 4 dB of gain with an input compression point of 0.5 dB. The gain is controllable with a range of 7 dB. The ourout return losses are -13 dB.

The conversion losses of the IQ modulator are -5 dBm and it has an input compression point of 1.5 dB. It achieves 75 dB of isolation between the LO and the output and the output matching is very good, since the simulated return losses are -20 dB.

In order to complete the simulations of the transmitter, we should mention that the low pass filters achieves 14 dB of gain and a 1-dB cutt of frequency, as it was defined in the specification. Finally the D/A converter achieved 48dB SNR and 57dB SFDR for 400Mhz input signal and 1.7GHz clock.

V. CONCLUSIONS - DISCUSSION

In this paper the design of a 60 GHz transceiver was presented. Emphasis was given in the design of the RFFE and the upconverter at 60 GHz since they are the most challenging circuits. Simulation results, including extracted parasitics, prove that it is feasible to satisfy all the necessary specifications if we use an advanced with a f_T of 100 GHz.

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