All-Digital Frequency and Clock Synthesis Architectures from a Signals and Systems Perspective, Current State and Future Directions

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***Abstract*— Modern nano-scale CMOS technologies favor all-digital architectures for frequency synthesizers in wireless and other mixed-signal applications. This paper is a short introduction to the topic presenting contemporary approaches from a signal and systems perspective as well as directions for future research.**

I. INTRODUCTION

Recent research efforts have introduced a number of new frequency and clock synthesis paradigms that make minimal or no use of analog circuit blocks. The effort to develop all-digital architectures can be traced at least three decades in the past and has been motivated by the robust performance and design convenience of digital circuits. In modern technologies the replacement of analog blocks by digital ones is vital especially in wireless applications. This is because the most advanced nano-scale digital CMOS processes, used for the intensive digital signal processing, are incompatible with traditional RF circuits. This paper reviews the recent developments in all-digital frequency and clock synthesis from a signals and systems perspective in an effort to introduce the reader to the challenges and research opportunities in this field.

II. FREQUENCY SYNTHESIZERS WITHOUT VCOS

The class of all-digital frequency synthesizers (FS) *without* VCO (nor a phase locked delay line) is formed of FS that are essentially fractional dividers. Driven by a reference frequency f_c they produce an output signal of *average* frequency $f_o = (A/B) f_c$ where A and B are positive integers. It can be $A > B$ if the FS is driven by multiple phases of the reference clock. In most cases these FS produce output signals whose (exact – not average) period is a *multiple* of $1/f_o$ and contains cycles (or pulses) of unequal lengths. Such signals have no instantaneous frequency but have *average* frequency (based on their fundamental periods). All there will become clear in the following subsections.

Two representatives of this class are considered; the Pulse DDS (PDDS), which is an old concept, and, the Flying Adder (FA) synthesizer which is a recent one. It is interesting to note that PDDS' output average frequency is proportional to the frequency control word whereas FA's output average frequency is inversely proportional to it.

A. Pulse DDS

The Pulse DDS (PDDS) [12], shown in Figure 1, is a basic and very early all-digital FS. It can be considered as a 1-Bit-DAC regular DDS [21]. Driven by reference clock f_c, PDDS generates average output frequency $f_o = (w/2^N) f_c$ which is set by the *frequency control word* $w \le 2^{N-1}$. At the rising edge of the *j*–th clock pulse register's value becomes $X_j = (jw) \bmod 2^N$ (assuming circuit is rising-edge triggered, $X_0 = 0$). Output is $Y_j = X_j \text{ div } 2^{N-1}$.

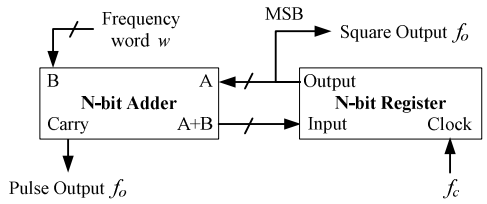

Figure 1: Pulse DDS (from [12])

The output of PDDS when $w = 12$ and $N = 5$ is shown in Figure 2(B). In (A) we have the desirable ideal periodic squarewave of frequency f_o. Both waveforms have the same *average* frequency f_o although the fundamental period of (B) is $2^N T / \gcd(w, 2^N)$ second long where $T = 1/f_c$. Note that all rising and following edges of (B) coincide with some rising edges of the clock (C).

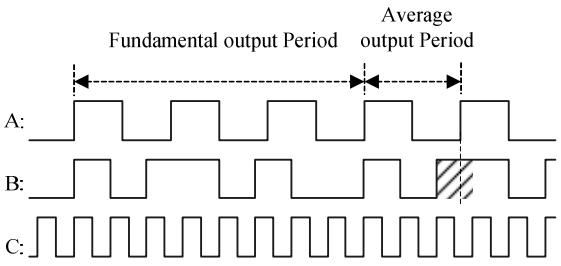

Figure 2: Pulse DDS: (A) Ideal Output, (B) Output, (C) Clock

This is always true because the rising edges of the clock are the times the circuit transitions from one state to another. Therefore output (B) is a *juxtaposition* of pulses that begin and end at times $i \cdot T$, $i = 0,1,2,\ldots$. This causes the timing irregularity of the output with respect to ideal signal (A) introducing frequency spurs at the harmonics $m \cdot f_c \cdot \gcd\left(w, 2^N\right)/2^N$, $m = 0,1,2,\ldots$.

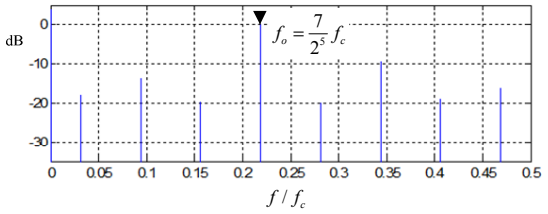

Figure 3: Pulse DDS Spectrum when $w = 7$ and $N = 5$.

To reduce the power of spurious frequency components Wheatley [22-23] introduced the random *jittering* (random phase dithering) technique shown in Figure 4.

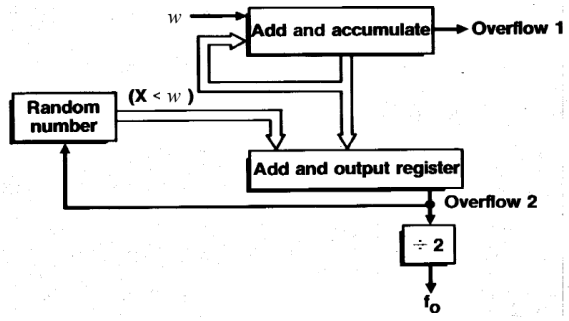

Figure 4: Wheatley's jittering technique for PDDS [22-23].

At every clock cycle the accumulator's value is perturbed by the addition of an integer random variable. This may randomly shift the edges of the output pulse, or, do nothing at all. The stochastic averages of the times the edges of the pulses appear equal those of the ideal signal (see the last pulse in (B) of Figure 2). This results in spreading the power of the spurs and converting it to phase-noise floor, as shown in Figure 5 using an approach similar to Wheatley's.

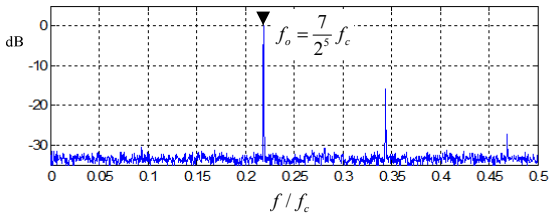

Figure 5: The result of Jittering on PDDS' Spectrum – Compare to.

B. *Flying Adder*

The Flying-Adder (FS) is a new, low-complexity all-digital architecture. It was introduced in [9,10] followed by a number of modeling and application papers [1,2,3,13,24,25] as well as a detailed theoretical analysis in [14,15].

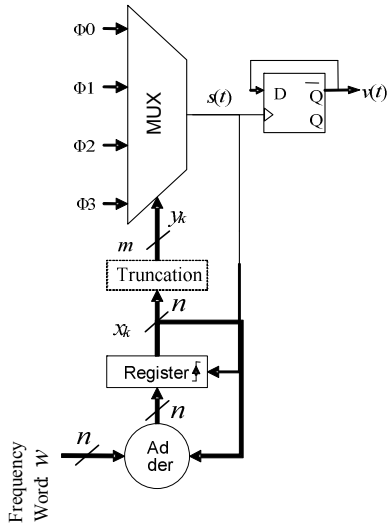

Figure 6: The Flying-Adder architecture with 4 input phases (from [14])

The basic structure of FA is shown in Figure 6. It is driven by a $M = 2^m$ ($m = 2$ here) - phase clock, typically generated by a ring oscillator with the corresponding number of stages as shown in Figure 7. The M phases are fed into an *M*-to-1 multiplexer (MUX) and the rising edges of the selected phase at the MUX's output trigger the *n*-bit register changing its value to $x_{k+1} = (x_k + w) \bmod 2^n$ from x_k. Here, *w* is the *n*-bit *frequency control word* (… although the name "period control word" is more accurate).

Note that the nonnegative integer variable *k* counts the rising edges of $s(t)$, it is the discrete-time reference of the FA, and is *not* a quantized version of (real) continuous time *t*.

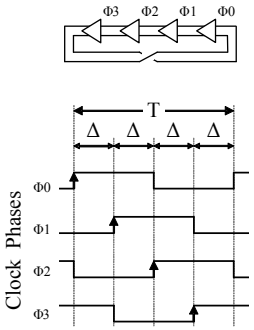

Figure 7: Clock Phases driving the FA

Register's value, x_k, is truncated by keeping the first *m* most significant bits. This defines the phase-selection variable $y_k = x_k \text{ div } 2^{n-m}$ which drives the MUX. Signal $s(t)$ is a sequence of pulses or/and spikes. It is fed to the D-Flip-Flop which acts as a frequency divider by 2 generating a cycle of output $v(t)$ for every two consecutive rising edges (or spikes) of $s(t)$. The average frequency, f_{ave}, of the output signal $v(t)$ is [14]

$$f_{ave} = \begin{cases} \frac{1}{2} f_c & \text{if} \quad w = 0 \\ \frac{2^{n-1}}{2^n - (2^m - 1)w} f_c & \text{if} \quad 0 < w < 2^{n-m} \\ \frac{2^{n-1}}{w} f_c & \text{if} \quad 2^{n-m} \le w < 2^n \end{cases} .$$

The output signal of the FA is shown in Figure 8(B) when $n = 4$, $m = 2$ and $w = 11$. These parameter values imply that the length of the fundamental period of the output is $11 \cdot \Delta$, where $\Delta = T / 2^m$ is the time offset between two consecutive phases (see Figure 7).

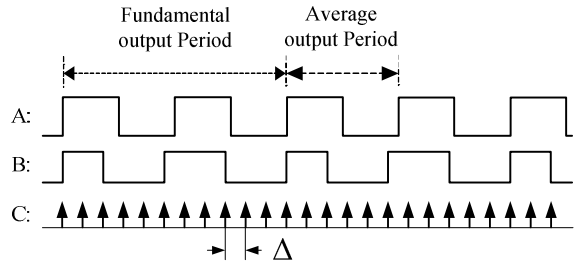

Figure 8: FA: (A) Ideal Output, (B) Output, (C) the Rising Edges of all Clock-phases combined. Parameters are $n = 4$, $m = 2$ and $w = 11$.

The spectrum for $n = 4$, $m = 2$ and $w = 11$ is shown in Figure 5. The desirable frequency f_o and the spurious frequency components are harmonics of the fundamental $(4/11) f_c = 1/(11\Delta)$ [14].

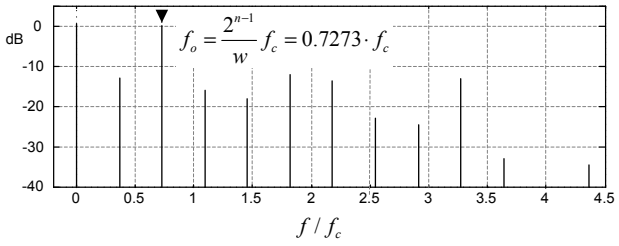

Figure 5 : The spectrum of $v(t)$ when are n=4, m=2 and w=11. The bold line corresponds to f_{ave} / f_c

The FA is a very convenient architecture for timing digital circuits capable of tolerating small and bounded deterministic jitter. More research is required however to suppress the strong spurious signals and make the FA useful in RF applications as well.

III. Frequency Synthesizers With VCOs

The spectra of VCO-less digital synthesizers we examined before are rich with spurious components because their output pulses are forced to begin and end at the edges of the reference clock. This major constraint can be alleviated using a VCO (any frequency controlled oscillator) to generate the output signal independently and relate its frequency and phase to that of the reference via a phase locking mechanism. The advantage in this case is that since the phase/frequency locking process is order(s) of magnitude *slower* that the output pulse rate, the short-term behavior (frequency, pulse shape) of the output is similar to its long-term average one. So, the output signal is much closer to an ideal periodic one.

A. *All Digital PLLs* (ADPLL)

There are two analog blocks in the classical integer-*N* PLL, the loop filter $H(s)$ and the VCO. The first is typically driven by the pulse-width modulated output of the phase frequency detector (PFD) and produces the analog frequency-control voltage for the VCO.

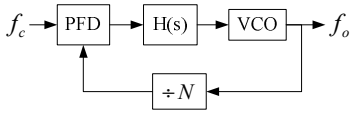

Figure 9 : Classical Integer-*N* PLL

Converting the PLL into a digital one involves the replacement of the PFD by a Time-to-Digital Converter (TDC) that produces a sequence of digital numbers which are (roughly) proportional to the phase (time to be accurate) difference of the two signals. The TDC drives a digital filter, which drives the digitally controlled VCO.

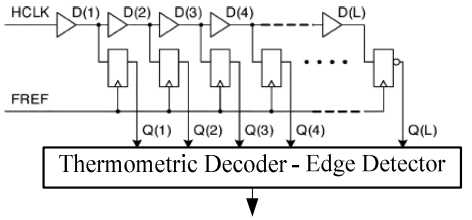

Figure 10: Time to Digital Converter (from [16]).

The VCO's clock (HCLK in Figure 10) is delayed by a chain of delay elements whose outputs are "sampled" by D-Flip-Flops clocked by the reference signal. The signals involved and their relative timing are shown in Figure 11.

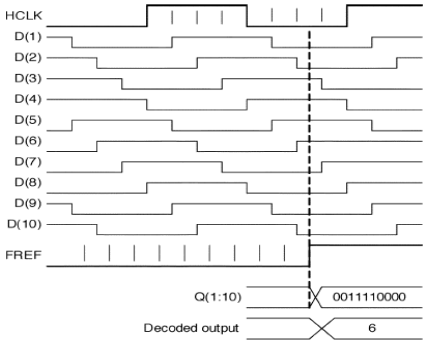

Figure 11: Timing of the signals in the TDC [17].

The thermometric decoder (Figure 10) provides a digital output corresponding to the time (phase) offset between the two clocks with accuracy of $\pm \Delta T / 2$, were, ΔT is the delay of the delay elements. Note that the TDC is the digital (and quantized) equivalent of the simple S-R-Flip-Flop type phase detector [6] that has limited lock-in range capability. The TDC can be combined with a pulse counter and a comparator [16], as shown in Figure 12, to yield the digital (and quantized) equivalent of the standard phase-frequency detector [6].

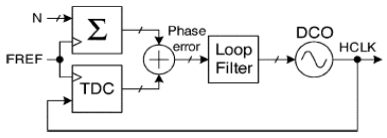

Figure 12: ADPLL with TDC combined with Pulse Counter-comparator [16].

The VCO can be designed based on a standard LC oscillator with an array of switchable capacitors (where the states of the switches form the digital frequency control word), e.g. [8,16,17,18], or it can be a ring oscillator with controllable delay elements, e.g. [4,5,11].

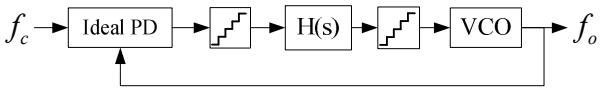

Figure 13: Quantization in the All-Digital PLL

A model of the all-digital PLL in Figure 12 is shown in Figure 13 where the two quantizers capture the quantization in the TDC and the digitally controlled VCO. The flat steps of the quantizers are likely to introduce limit cycles or chaotic behavior in the PLL. Adding Σ-Δ modulation helps alleviating this problem, and, improves the frequency resolution as well. It can be done in several ways [18], one of which is based on a fractional divider as in Figure 14.

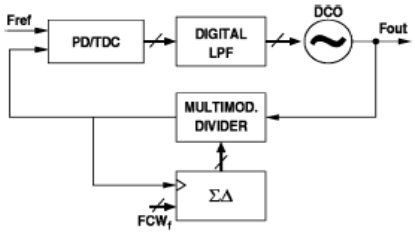

Figure 14: Fractional ADPLL with Σ-Δ modulation [20].

Variations of the above architectures, as well as a lot of technical information regarding the design aspects of the ADPLL can be found in [5,4,8,11,16,18,20]. Finally, advances in the design of Σ-Δ modulators and related MASH architectures offer improved phase-noise shaping and compact circuit implementations [7].

ADPLLs have attracted significant research interest over the past few years and some understanding of their behavior has been achieved, e.g. [8,19]. However ADPLLs are nonlinear dynamical systems, potentially with complicated behavior. More research from a systems and control perspective is required to understand better their dynamical behavior and trade-offs.

IV. Conclusions

A brief survey of all-digital architectures for frequency synthesis has been presented introducing the reader to this contemporary area of research and suggesting future research directions.

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