Timing and Spectral Properties of the Flying-Adder Frequency Synthesizers

Paul P. Sotiriadis

Sotekco Electronics LLC
Baltimore, MD, USA
pps at ieee dot org

Abstract—**The Flying-Adder frequency synthesizer architecture is modeled and analyzed mathematically. Its fundamental discrete and continuous-time periods, average output frequency, and strict bounds of its deterministic jitter measures are given. Examples of its output spectrum are given and discussed. The analytical results have been verified with MATLAB simulations.**

INTRODUCTION

Most of the modern electronic products and advanced systems have an imbedded frequency synthesizer of some form. Depending on the application the synthesizer may be simple or complex. In all cases, the best signal quality is desirable for the smallest possible cost, power consumption, chip-area or physical size, etc.

Flying-Adder frequency synthesizer [1] is a relatively new, elegant architecture that belongs to the general class of period (vs. frequency) digital synthesizers [2-4]. It is very simple, it offers good frequency (period) resolution, it can be directly combined with a ring oscillator (that is very often present in integrated designs) and has the advantages of digital circuits in terms of design convenience and fabrication.

This paper presents results of mathematical modeling and analysis of the Flying-Adder and it was motivated by the request for such theoretical development in [5].

Specifically, analytical expressions are given of the discrete and the continuous-time periods and of the average output frequency. Also, strict bounds of several measures of output's determinist jitter are provided along with strict bounds of the output pulse lengths. Finally, the spectrum of the Flying-Adder is derived numerically and discussed for certain combinations of its parameters.

THE FLYING ADDER SYNTHESIZER

The Flying-Adder is driven by a family of clock phases, like the one in Figure 1, containing $M = 2^m$ (m=2 here) periodic, 50% duty-cycle square waves (of the same frequency) and relative phase-offsets forming an arithmetic progression with step $-2\pi / M$ rads which corresponds to time shifts equal to $\Delta = T / 2^m$. A convenient way to generate these signals is by using a ring oscillator with the corresponding number of stages as shown in Figure 1a.

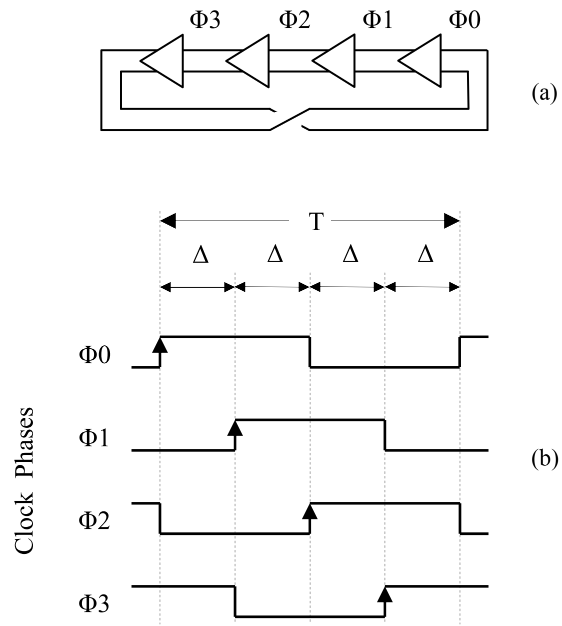

Figure 1: Clock Phases Driving the Flying-Adder

The basic structure of the Flying-Adder architecture is shown in Figure 2. It is driven by the $M = 2^m$ clock phases, one of which is selected by the M-to-1 multiplexer (MUX). The rising edges of MUX's output (signal $s(t)$) trigger the n-bit register changing its value from x_k to

$$x_{k+1} = (x_k + w) \bmod 2^n .$$

where w is the n-bit long frequency (period) control word. The integer variable k here counts the rising edges of $s(t)$ and it is

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the discrete-time reference for the Flying-Adder. The register's value, x_k, is then truncated by keeping the first *m* most significant bits. This defines

$$y_k = x_k \text{ div } 2^{n-m}$$

which controls the MUX and therefore chooses the input phase that passes through the MUX. The signals $s(t)$ which is a sequence of pulses, or spikes or both, is fed to the D-Flip-Flop which acts as a frequency divider by-2 providing the output signal $v(t)$. Two consecutive rising edges of $s(t)$ result in an output pulse.

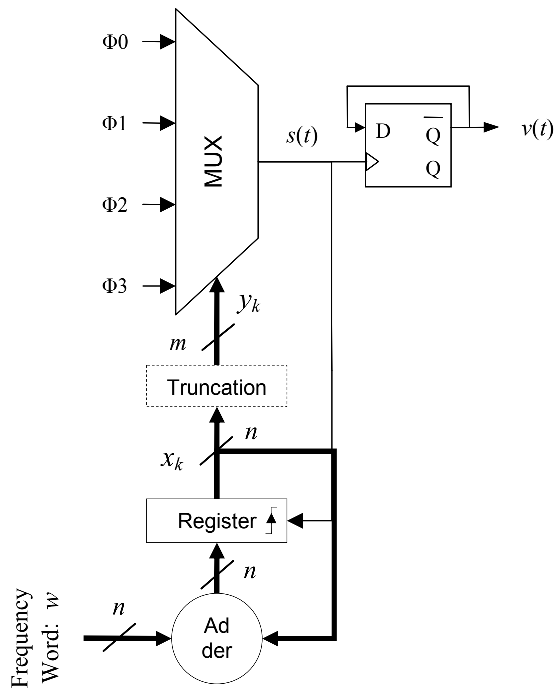

Figure 2: The Flying-Adder architecture shown here with 4 input phases

EXAMPLE: FLYING-ADDER WITH $n = 4, m = 2$ & $w = 15$

As an example of the Flying-Adder's operation we examine the case where $n = 4$, $m = 2$ and $w = 15$. MATLAB simulation results are shown in Figure 3 with all signals corresponding to the ones in Figure 2.

The x-axis in Figure 3 is the (real) time axis in multiples of Δ and the four input phases, Φ_i, $i = 1,2,3,4$, are shown in Figure 3a. The input phase, Φ_i, propagating to the output is selected by the MUX based on the value of $i(k) = y_k$. The time intervals in which the phases are selected are indicated with *thick* line segments.

The discrete-time *k*, shown in Figure 3f, is the result of counting the *rising* edges in $s(t)$. The discrete-time has value *k* between the kth and *k*+1 rising edges.

Sequence d_k, shown in part (d) of Figure 3, is defined as $d_k = (y_k - y_{k-1}) \bmod 2^m$ and is used to calculate the real-time length between consecutive rising edges (it is not proportional to it), details can be found in [6].

The D-Flip-Flop counts the rising edges (spikes or pulses) in $s(t)$ modulo-2, (frequency-division by 2) generating the output signal $v(t)$ shown in Figure 3g.

OUTPUT PERIOD AND AVERAGE FREQUENCY

The discrete-time period of the output has been derived based on the discrete-time counter – variable *k*. We have the following theorem whose proof can be found in [6].

Theorem 1: *The fundamental discrete-time period of the output signal* $v(t)$ *is*:

$$L_v = \max\left\{2\,, \frac{2^{n-m}}{\gcd(w, 2^{n-m})}\right\}.$$

Note that this is the fundamental (minimum possible) discrete-time period of $v(t)$.

Calculating the real-time duration, Δ_k, of the *k*-th discrete-time period, for all $k = 1,2,3,\ldots$ and using Theorem 1 we can derive the length of the continuous-time period of the output $s(t)$, $T_v = \sum_{k=1}^{L_v} \Delta_\kappa$. It can be shown that [6], the continuous-time period of output $v(t)$ is

$$T_v = \Delta \cdot \begin{cases} \dfrac{2^n - (2^m - 1)w}{2^{n-m}} \cdot L_v & \text{if } 0 < w < 2^{n-m} \\ \dfrac{w \cdot L_v}{2^{n-m}} & \textit{otherwise} \end{cases}$$

The average frequency, f_{ave}, of the output $v(t)$ is defined as the number of cycles in $v(t)$ within a period T_v divided by T_v (see [6,7]). It can be shown that [6],

$$f_{ave} = \begin{cases} \dfrac{2^{n-1}}{2^n - (2^m - 1)w} f_{clk} & \text{if } 0 < w < 2^{n-m} \\ \dfrac{2^{n-1}}{w} f_{clk} & \text{if } 2^{n-m} \le w < 2^n \end{cases}$$

where by definition $f_{clk} = 1/T = 1/(2^m \Delta)$.

OUTPUT JITTER

For most of the values of *w*, the output signal $v(t)$ of the Flying-Adder is irregular, especially when $w < 2^{n-m}$. Its period is composed of a number of pulses of unequal lengths as in the case of Figure 3. Therefore, the FA's output has deterministic jitter (except for very few values of *w*).

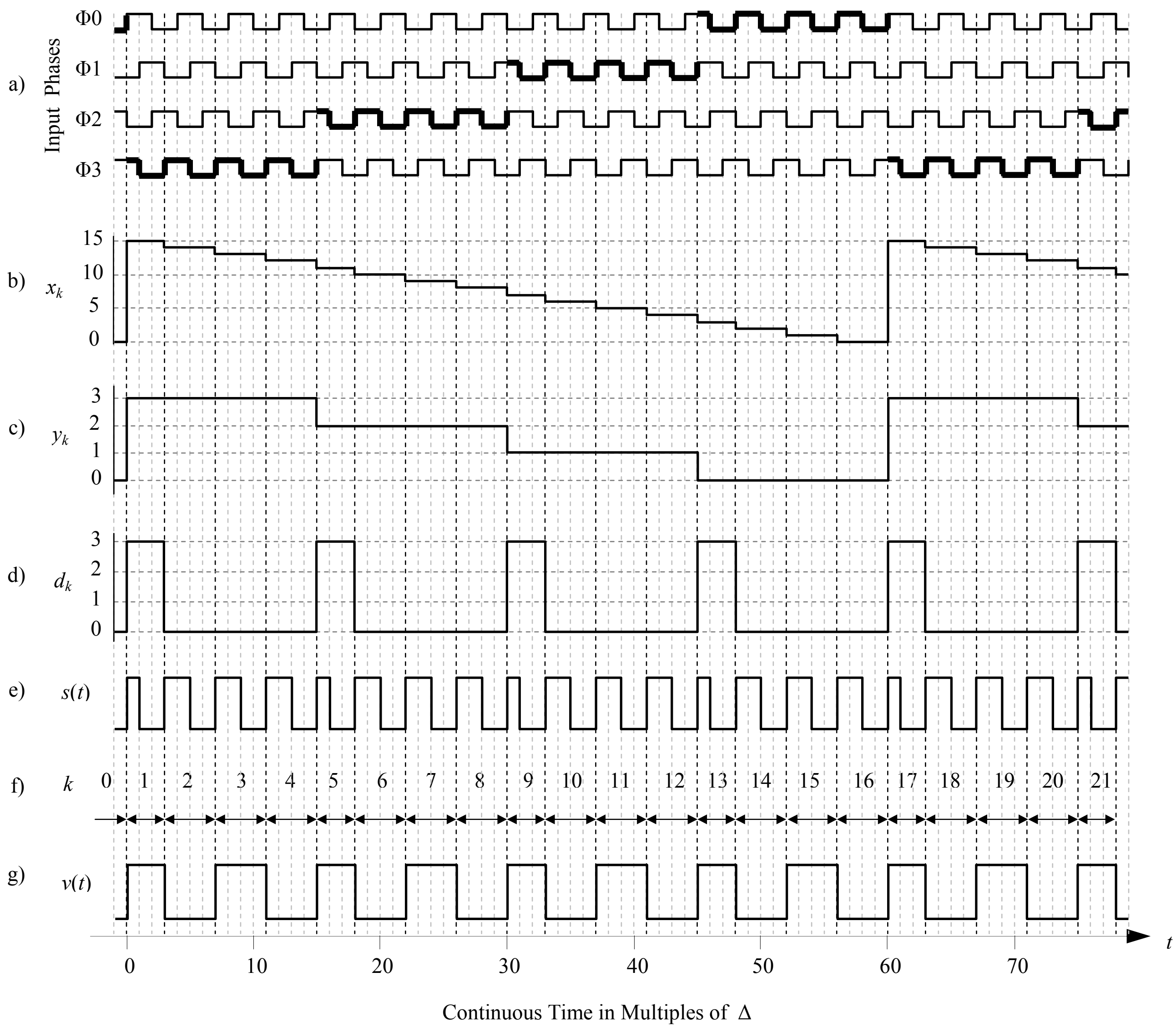

Figure 3 : The signals of the Flying-Adder synthesizer for $n=4$, $m=2$ and $w=15$.

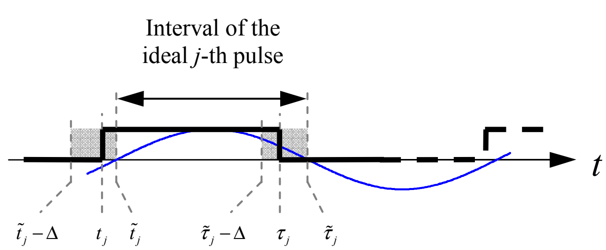

Figure 4 : The j^{th} pulse in $v(t)$ and the j^{th} pulse in the ideal squarewave of the average frequency, f_{av}, when $2^{n-m} < w < 2^n$ and $L > 1$.

To derive analytic estimates of the timing errors and jitter we compare the output $v(t)$ to the ideal 50% duty-cycle periodic squarewave of average frequency f_{ave}, whose first rising edge coincides with that of $v(t)$ at time $t=0$. The situation for the j-th pulse is shown in Figure 4.

Here, t_j and τ_j be the times of the j-th rising and falling edges of $v(t)$ respectively. It can be shown that it is

$$t_j = \left\lceil \frac{2(j-1)w}{2^{n-m}} \right\rceil \cdot \Delta$$

and

$$\tau_j = \left\lfloor \frac{(2j-1)w}{2^{n-m}} \right\rfloor \cdot \Delta$$

Moreover, for the ideal squarewave we have that

$$\tilde{t}_j = \frac{2(j-1)w}{2^{n-m}} \cdot \Delta$$

and

$$\tilde{\tau}_j = \frac{(2j-1)w}{2^{n-m}} \cdot \Delta$$

From the above we conclude that $\tilde{t}_j - \Delta < t_j \leq \tilde{t}_j$ and $\tilde{\tau}_j - \Delta < \tau_j \leq \tilde{\tau}_j$.

Using this result and some further analysis we derive strict upper bounds for different jitter measures. Specifically it can be shown that [6], a) *Absolute Jitter* $\leq \Delta$, b) *Absolute Cycle-to-Cycle Jitter* $\leq \Delta$, c) *Accumulated Jitter* $\leq \Delta/2$, d) *Cycle Average Jitter* $\leq \Delta/2$, and, d) *Cycle-to-Cycle Average Jitter* $\leq \Delta$. All jitter estimates are based on the rising edge of $v(t)$ (as well as those of the ideally squarewave).

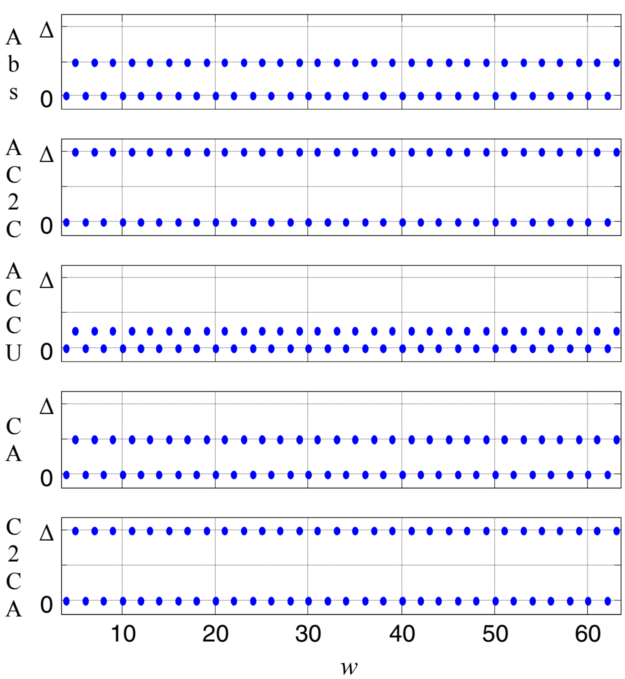

Figure 5 : Jitter measures when n = 6, m = 4 and w = 4, 5 ,6 , …, 63. JA: *Absolute Jitter*, JAC2C: *Absolute Cycle-to-Cycle Jitter*, JACCU: *Accumulated Jitter*, JCA: *Cycle Average Jitter* and JC2CA: *Cycle-to-Cycle Average Jitter.*

Figure 5 shows the numerical values of five measures of the deterministic jitter of the output $v(t)$ when n = 6, m = 4 and w = 4, 5 ,6 , …, 63. (Note that we deliberately excluded the cases of $w < 2^{n-m}$ as they result in very irregular waveforms.)

In addition to jitter, one can comment on the size of the pulses in $v(t)$. Specifically, if $2^{n-m} \leq w < 2^n$ then the length of every 0 or 1 interval in equals one of the two values

$$\left\lfloor \frac{w}{2^{n-m}} \right\rfloor \cdot \Delta, \quad \left\lfloor \frac{w}{2^{n-m}} \right\rfloor \cdot \Delta + \Delta$$

and within every continuous-time period T_v there exist two intervals (0 or 1 or both) of length equal to each of the above values. In addition, the length of every cycle (0-interval followed by 1-interval, or, vice versa) equals one of the values

$$\left\lfloor \frac{2w}{2^{n-m}} \right\rfloor \cdot \Delta, \quad \left\lfloor \frac{2w}{2^{n-m}} \right\rfloor \cdot \Delta + \Delta$$

and within every continuous-time period T_v there exist at least two cycle of length equal to each of these two values.

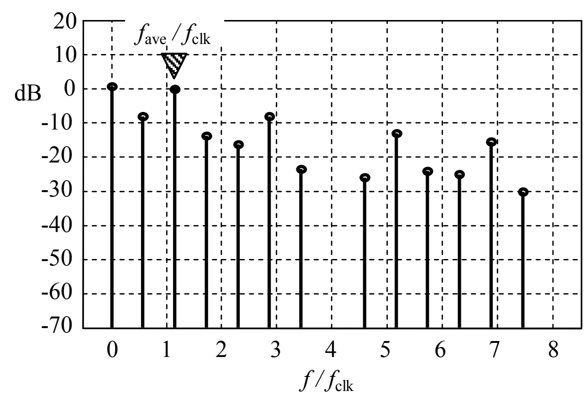

Figure 6 : The spectrum of $v(t)$ for n = 4, m = 2, w = 7

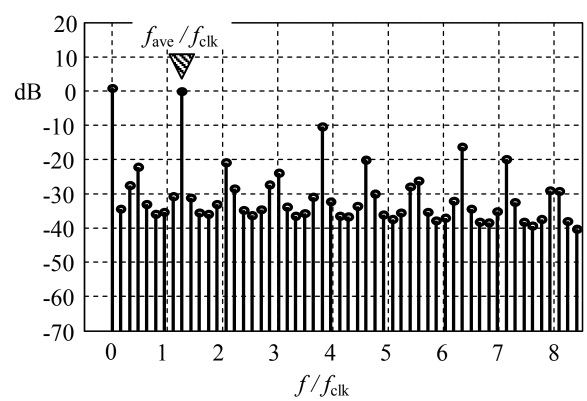

Figure 7 : The spectrum of $v(t)$ for n = 8, m = 4, w = 101

OUTPUT SPECTRAL CHARACTERISTICS

Since the fundamental continuous-time period of the output signal is T_v, the spectrum of $v(t)$ consists of (some of the) harmonics at frequencies $f_\ell = \ell / T_v$, $\ell = 0,1,2,\ldots$. Output $v(t)$ can be expressed as a Fourier series accordingly. Since the analytic expression of T_v is known the discrete spectrum can be easily derived numerically. Given the digital structure of the FA one should not expect significant deviation between numerical results and actually measurements – with the exception of high-order harmonics whose amplitude may be altered due to bandwidth limitations of the implementation or excessive imbalance between the clock phases of the (ring) oscillator.

Figure 6 shows the spectrum in the case of n = 4, m = 2 and w = 7 which implies that $L = 4$, $f_{ave} \cong 1.14 \cdot f_{clk}$ and f_{ave} is the second harmonic in the spectrum. Moreover, it is $T_v = 7 \cdot \Delta$. The SFDR is about 8dB.

Figure 7 shows the spectrum in the case of n = 8, m = 4 and w = 101 which implies that $L = 16$, $f_{ave} \cong 1.27 \cdot f_{clk}$ and f_{ave} is the eight harmonic in the spectrum. Moreover, it is $T_v = 101 \cdot \Delta$. The SFDR is about 20dB if we exclude the harmonics of f_{ave}, or about 10dB otherwise.

CONCLUSSIONS

Results of detailed mathematical modeling and analysis of the Flying-Adder frequency synthesizer have been presented, including the discrete and continuous-time period, the average output frequency and strict bounds of several measures of output's determinist jitter.

Based on the presented results it appears that the Flying-Adder can be very useful for digital circuits that can tolerate certain deterministic timing irregularity. Use of the Flying-Adder in analog / RF applications is expected to be limited due to very low spurious free dynamic range, which could potentially be improved through some form of random dithering at the cost of higher noise floor.

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