

# Almost-Digital Multiphase Frequency Mixing

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**Abstract**—This work presents a compact, almost-digital frequency mixer that produces a sinusoidal signal at frequency  $\omega_1 \pm \omega_2$  when driven by two digital periodic signals of frequencies  $\omega_1$  and  $\omega_2$ . The mixer uses multiple phases of the input signals to suppress higher order intermodulation products and increase the spurious free dynamic range of the output. A circuit implementation has been realized using an FPGA and it was used to derive spectral measurements demonstrating the feasibility and performance of the architecture.

## I. INTRODUCTION

Frequency mixing is a fundamental part of frequency synthesis which is used in a broad range of applications including wireless communications, radars, metrology, instrumentation, etc.

There are several types of mixers which, for the purpose of the discussion in this paper, we can classify into three major categories:

A) The multipliers that are driven by two sinusoidal signals and produce a sinusoidal at the sum or the difference frequency, after their output is filtered appropriately [1].

B) The switches, like the diode mixers, that are essentially driven by a sinusoid of frequency  $\omega_1$ , and a digital signal at frequency  $\omega_2$  that controls the switch. They produce the frequency components of the form  $k\omega_2 \pm \omega_1$  and the desirable one is filtered out [2]-[3].

C) The fully digital-input mixers that are driven by two digital periodic signals at frequencies  $\omega_1$  and  $\omega_2$  and produce a sinusoidal or square periodic output at one of the frequencies  $\omega_1 \pm \omega_2$  (other intermodulation products can be extracted as well). Common mixers of class (C) are the EXOR gate and the D-Flip-Flop.

In moving from class (A) to class (C), the purity of the output spectrum typically worsens, but the circuitry becomes simpler. Mixers in class (C) are especially easy to integrate in a standard CMOS technology and can be migrated to new technologies if needed without any effort.

Although the proposed architecture belongs to class (C), it aims to offer the best of both (A) and (C) classes: compact almost-digital implementation and high spurious free dynamic range (SFDR). It does so by using multiple phases of the input digital signals to suppress higher order intermodulation products and advances over previous work based on similar concepts [4]-[5].

Structurally, the mixer with  $P$  input phases is composed of 2 identical finite state machines (FSM) and  $P$  read-only memories (ROM) that generate the approximate output sinusoid in a digital non-binary representation.  $P$  simple nonlinear DACs [6] convert the sinusoidal output into analog form.

## II. IMPROVING MIXER SPECTRAL PURITY THROUGH MULTIPHASE COMBINING

Let  $a(t)$  be a periodic signal of frequency  $\omega_1$  and period  $T_1$  and  $b(t)$  be a periodic signal of frequency  $\omega_2$  and period  $T_2$ . Consider their Real Fourier series representation:

$$a(t) = \sum_{k=1}^{\infty} A_k \cos(k\omega_1 t + \theta_k)$$
$$b(t) = \sum_{m=1}^{\infty} B_m \cos(m\omega_2 t + \phi_m)$$

Suppose we are interested in the frequency component  $\omega_1 - \omega_2$  in the product  $a(t)b(t)$ . In general, the product  $a(t)b(t)$  contains undesirable intermodulation products at frequencies  $k\omega_1 \pm m\omega_2$ . It can be shown that the signal

$$y(t) = \sum_{n=0}^{P-1} a(t + \frac{nT_1}{P}) b(t + \frac{nT_2}{P})$$

also contains the desired component  $\omega_1 - \omega_2$  but has many fewer undesired intermodulation products than  $a(t)b(t)$  [5]. In fact, this sum of multiphase products can be expressed as

$$y(t) = \sum_{k=1}^{\infty} \sum_{m=1}^{\infty} \frac{PA_k B_m}{2} \left[ \cos((k\omega_1 + m\omega_2)t + \theta_k + \phi_m)s(k+m) + \cos((k\omega_1 - m\omega_2)t + \theta_k - \phi_m)s(k-m) \right] \quad (1)$$

where

$$s(n) = \begin{cases} 1 & \text{if } n \text{ is integer multiple of } P \\ 0 & \text{otherwise} \end{cases}$$

As seen from this equation, many intermodulation products formed from multiplying  $a(t)$  with  $b(t)$  are cancelled by the multiphase combining. In the single-phase product  $a(t)b(t)$ , an intermodulation product  $k\omega_1 \pm m\omega_2$  will be present (in almost all cases) if both  $A_k$  and  $B_m$  are nonzero. However, in the multiphase-combined signal (1), the presence of an intermodulation product  $k\omega_1 \pm m\omega_2$  requires also that  $k \pm m$  be an integer multiple of  $P$ , the number of phases. Thus for larger numbers of phases, fewer undesired intermodulation products will be present. However, the desired component  $\omega_1 - \omega_2$  will always be present.

Fig. 1 shows the locations of intermodulation products in single phase product  $a(t)b(t)$ , assuming that  $a(t)$  and  $b(t)$  possess odd harmonics but no even harmonics. The axes are the indices of the intermodulation products. The presence of

a “ $\Delta$ ” at a point on the plot indicates the presence of a difference intermodulation product  $k\omega_1 - m\omega_2$ ; the presence of a “+” indicates the presence of a sum intermodulation product  $k\omega_1 + m\omega_2$ . Thus, the single phase product will possess all intermodulation products of the form  $k\omega_1 \pm m\omega_2$ , where  $k$  and  $m$  are odd.

However, fig. 2 shows the locations of intermodulation products of the multiphase-combined signal, for the same inputs  $a(t)$  and  $b(t)$ . Here, we see far fewer undesired products.

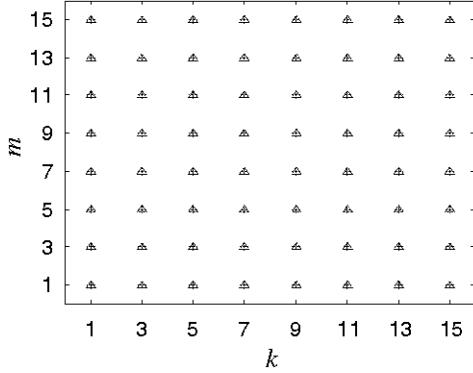


Fig. 1. Locations of intermodulation products for a single phase mixer

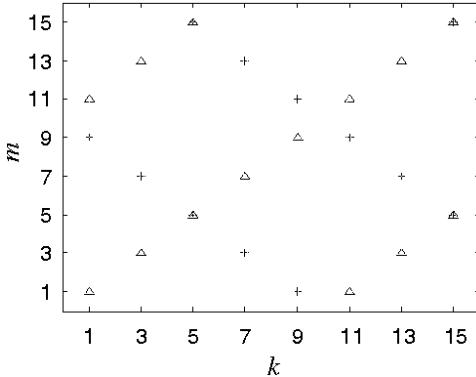


Fig. 2. Locations of intermodulation products for a 5-phase mixer

Additionally, the sum frequencies  $k\omega_1 + m\omega_2$  are large enough to be regarded as outside the passband of the system, leaving only uncancelled difference frequency terms.

It can also be shown that this multiphase combining technique can be modified to obtain a multiphase-combined signal with the  $\omega_1 - \omega_2$  component cancelled and the  $\omega_1 + \omega_2$  component present. This is achieved with this alternate pairing of products:

$$\sum_{n=0}^{P-1} a(t + \frac{nT_1}{P}) b(t - \frac{nT_2}{P})$$

While (1) shows that most intermodulation products are cancelled, we can further improve the spectral purity of the mixer by selecting  $a(t)$  and  $b(t)$  to have as many coefficients  $A_k$  and  $B_k$  equal to zero as possible. In this work, we consider

$a(t)$  and  $b(t)$  taking the following form:

$$a(t) = p_i, \quad t \in \left[ \frac{iT_1}{N}, \frac{(i+1)T_1}{N} \right], \quad (2)$$

with

$$p_i = \cos\left(\frac{2\pi i}{N} + \theta\right), \quad (3)$$

with  $\theta \in [0, 2\pi/N]$ . Thus  $a(t)$  has constant values on  $N$  uniform intervals in each period  $T_1$ . The function  $b(t)$  is defined similarly, with  $T_2$  replacing  $T_1$  (thus  $b(t)$  is only a time-scaled version of  $a(t)$ ).

It can be shown that signals  $a(t)$  and  $b(t)$  of this form possesses non-zero harmonics only at indices  $k = (rN + 1)$  and  $k = (rN - 1)$ , for integers  $r$ :

$$A_k = B_k = 0, \quad \text{if } k \neq (rN + 1), (rN - 1).$$

Note that if  $N$  is even, then

$$p_i = -p_{i+N/2}.$$

### III. HIGH-LEVEL ARCHITECHTURE OF THE MIXER

Now that we have discussed a mathematical basis by which one can use piecewise-constant functions to generate a spectrally pure frequency mixer, we will present its physical implementation using mostly digital circuitry.

#### A. Digital Synthesis of Sinusoidal Products

To illustrate the concepts behind digital sinusoidal product generation, we discuss the synthesis of products for products  $a(t)b(t)$  when  $a(t)$  and  $b(t)$  have  $N = 4$  divisions per period.

The signal  $a(t)$  can be represented digitally using a finite state machine with four states (2 bits) with the following order of transitions:

$$\text{state } 0 \rightarrow \text{state } 1 \rightarrow \text{state } 2 \rightarrow \text{state } 3 \rightarrow \text{state } 0$$

At the active edge of a clock of angular frequency  $4\omega_0$ , the state transitions to the next state. When the state machine is at the last of the four states, it will transition to the first state at the active clock edge. Since the signal  $a(t)$  has fundamental frequency  $\omega_0$ , the digital output of the state machine also has fundamental frequency  $\omega_0$ . Additionally, since  $a(t)$  is sampled four times per period of it, the Nyquist sampling theorem is satisfied.

We can similarly construct a finite state machine to generate a digital representation of  $b(t)$ . The product  $a(t)b(t)$  can then be computed by inputting  $a(t)$  and  $b(t)$  into a digital ROM. The ROM then outputs a digitally coded form of the product  $a(t)b(t)$ . This digital representation of the product is then converted to the analog form  $a(t)b(t)$  through a digital-to-analog converter (DAC).

The circuit described so far is depicted in fig. 3, where we have added a yet unspecified DAC to generate the analog approximation of  $a(t)b(t)$ .

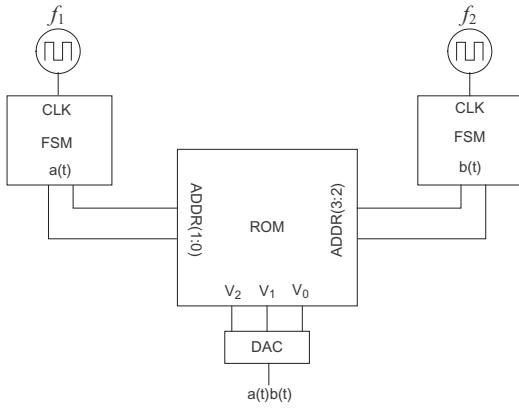


Fig. 3. Generating the digital representation of product  $a(t)b(t)$

### B. Nonlinear Digital-to-Analog Conversion

First examine the circuit of figure 4. This figure depicts a nonlinear DAC. In this figure, the circuit converts the digital vector  $(V_2, V_1, V_0, W_2, W_1, W_0)$  into analog value  $V_{out}$ :

$$V_{out} = c \left( \frac{V_2}{R_2} + \frac{V_1}{R_1} + \frac{V_0}{R_0} + \frac{W_2}{R_2} + \frac{W_1}{R_1} + \frac{W_0}{R_0} \right),$$

where

$$c = \frac{1}{\frac{2}{R_0} + \frac{2}{R_1} + \frac{2}{R_2}}$$

is a constant that depends on the choice of the resistors.

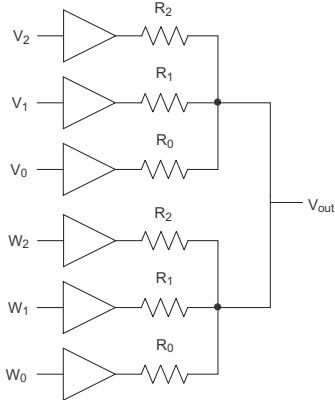


Fig. 4. Nonlinear DAC, for the case  $B = 3$

Since this DAC can only generate positive voltages, generating negative values requires placing a DC offset on the output. The proposed DAC, with  $2B$  resistors, can generate an output of the following form:

$$c \sum_{i=0}^{B-1} \frac{s_i}{R_i} + c \sum_{i=0}^{B-1} \frac{1}{R_i} \quad (4)$$

where  $s_i \in \{-1, 0, 1\}$  and

$$c = \frac{1}{\sum_{i=0}^{B-1} \frac{2}{R_i}}$$

This can be seen as follows. First let  $V = 00 \dots 0$  and  $W = 11 \dots 1$ . This produces an analog output of

$$c \sum_{i=0}^{B-1} \frac{1}{R_i}$$

This is the DC offset of the DAC that corresponds to a desired analog value of 0. If we now choose  $V_i = 1$ , while keeping  $W$  unchanged, we have made  $s_i = 1$  and  $s_j = 0$  for all  $j \neq i$ . If we now choose  $V_i = 0$  and  $W_i = 0$ , we have made  $s_i = -1$ . Similarly, choosing  $V_i = 0$  and  $W_i = 1$ , we have made  $s_i = 0$ .

We can do the same for any  $V_j$  and  $W_j$  to choose  $s_j$  to be 1, -1, or 0. Thus, we arrive at (4). An important property of this DAC is that its possible outputs occur in exactly oppositely signed pairs. This is a desirable property considering that the coefficients  $p_i$  of (3) occur in oppositely-signed pairs for even  $N$ .

Thus, we can generate all values  $p_i p_j$ ,  $i, j = 0, 1, \dots, N-1$  of the product  $a(t)b(t)$  by choosing the appropriate encoding for the ROM and the appropriate resistor values. The complete mixer is shown in fig. 5.

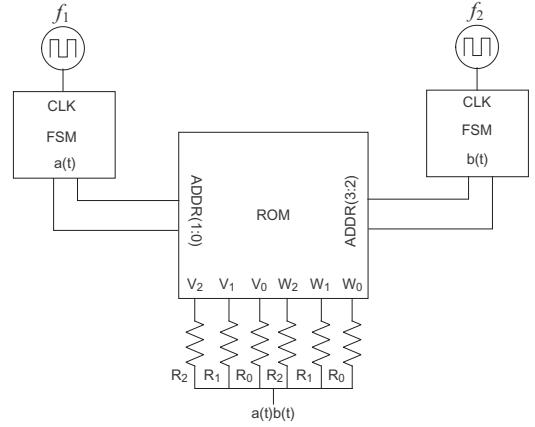


Fig. 5. Complete single-phase mixed-signal mixer

### IV. EXPERIMENTAL VERIFICATION

The proposed frequency mixer was tested using a commercial FPGA board driving a resistor network on a custom PCB. Our choice of parameters for the sinusoidal approximation signals were  $N = 10$  and  $P = 5$ , with the DAC to be constructed with  $2B = 8$  resistors, with the values of resistor ratios summing to less than or equal to 60. With these choices, we employed a numerical optimization algorithm to locate an optimal phase shift  $\theta$  and resistor values. We constrained resistances to be integer multiples of 50 Ohms with the objective of minimum mean square error in approximating the product  $a(t)b(t)$ . Our optimization algorithm arrived at a solution of  $\theta = 0.314159$  rad and the resistor ratios given in table I.

Table II lists, in normalized form, all the non-negative products generated by multiplying pairs of amplitudes of  $a(t)$ . These four values are closely approximated using our chosen resistor network. These values are also listed in table II. As can

resistor	multiple of reference (50 Ohm)	resistance
$R_0$	6	300
$R_1$	7	350
$R_2$	12	600
$R_3$	23	1150

TABLE I

RESISTOR VALUES FOR TEST CIRCUIT

be seen, the approximation products produced by the resistor network closely approximate the ideal products (the accuracy of negative product approximations is the same as the accuracy of the positive ones). Additionally, the resistor values used are only integer multiples of a reference value.

exact product (normalized)	resistor network approximation of product (normalized)
0	0
0.1714118	0.1714133
0.2773501	0.2773489
0.4487619	0.4487623

TABLE II

ALL POSSIBLE NON-NEGATIVE PRODUCTS OF THE APPROXIMATION  
FUNCTION FOR TEST CIRCUIT

Figure 6 shows the output spectrum of a single phase of the multiphase mixer (i.e., here we have only one of the five ROMs and its eight resistors). Figure 7 show the (total) output spectrum of the multiphase mixer. In both cases, the input frequencies are  $f_1 = 755$  kHz and  $f_2 = 1$  MHz, and, the resulting output frequency  $f_{out} = 245$  kHz.

From comparison with figures 6 and 7, it can be seen that the magnitudes of spurious signals have been reduced in the multiphase circuit by about 12dB due to suppression of intermodulation products. The resulting SFDR is 50dB (or 59dB if the presence of the 3rd and 5th harmonics are acceptable).

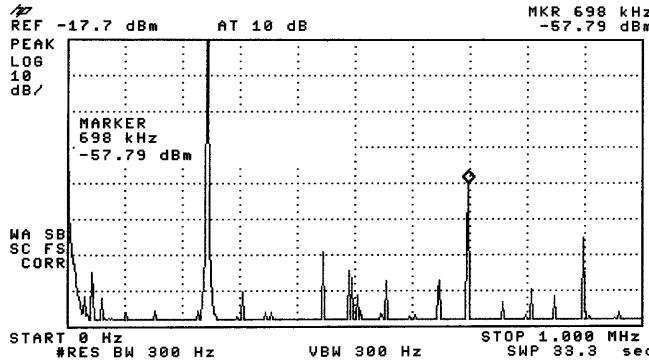


Fig. 6. Spectrum of a single phase mixer for input frequencies 7.55/10 MHz and 10/10 MHz

## V. CONCLUSIONS

A compact, wideband, almost digital, multiphase frequency mixer architecture has been presented. It produces a sinusoidal

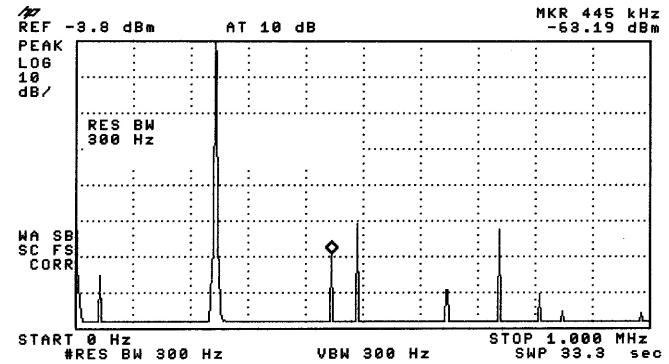


Fig. 7. Spectrum of 5-phase mixer for input frequencies 7.55/10 MHz and 10/10 MHz

output at frequency  $\omega_1 \pm \omega_2$  when driven by two digital periodic signals of frequencies  $\omega_1$  and  $\omega_2$ . This allows the mixer to be driven directly from digital frequency sources without the need of filtering the harmonics. Also, this architecture is very easy to integrate in a standard CMOS technology and migrate to another technology if needed, without any effort.

The mixer is composed of small finite state machines, a ROM look-up-table and simple nonlinear digital-to-analog converters. An FPGA-PCB test circuit demonstrated the feasibility of the proposed architecture and a 50dB (or 59dB) spurious free dynamic range, which is acceptable in many communication and signal processing applications.

The primary source of error was the drivers (inverters) and the resistor network in the nonlinear digital-to-analog converters. The secondary source of error was mismatch in signal delays. It is expected that an integrated circuit implementation with careful circuit component matching and digital-to-analog converters based on current source architectures will lead to significantly higher spurious free dynamic range.

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