Intrinsic Jitter of Flying-Adder Frequency Synthesizers

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Abstract—Motivated by the “open problem” questions stated recently in [1], this work provides mathematical estimates of the Flying-Adder frequency synthesizer’s deterministic jitter. The analytical results have been verified using MATLAB.

INTRODUCTION

Frequency synthesis is important for most digital and high-frequency analog circuits and systems. Digital circuits are driven by the clock that is required to have minimal jitter and frequency and duty cycle within desirable range. Analog circuits, especially communication ones, require a reference-frequency signal with minimal spurs and phase noise.

Chip space and power constraints typically force the use of the simplest frequency synthesizer possible that can meet the requirements.

A new, low-complexity architecture, the Flying-Adder frequency synthesizer [2] has been introduced in the literature recently. It is an elegant loop-less methodology using pulse-swallowing [3-5] to achieve improved frequency resolution.

This paper presents a mathematical approach to the estimation of the intrinsic (deterministic) jitter of the Flying-Adder synthesizer, considered as irregularity of its output pulse sequence. Derivations of the period and average frequency of the synthesizer’s output signal are also derived to allow for the fractional jitter derivation and provide some information about the spectrum of the synthesizer.

OPERATION OF THE FLYING ADDER SYNTHESIZER

We briefly review the operation of the Flying-Adder synthesizer. Starting from Figure 1b, a family of $M = 2^n$ periodic, 50% duty-cycle square waves of the same frequency and relative phase-offsets, that form an arithmetic progression with phase step $-2\pi / M$ (which corresponds to time offset $\Delta$), are generated, typically using a ring oscillator with the corresponding number of stages as shown in Figure 1a.

The $M = 2^n$ phases are fed into the $M$-to-1 multiplexer (MUX) of the Flying-Adder in Figure 2 and the rising edges of MUX’s output, signal $s(t)$, trigger the $n$-Bit Register changing its value from $x_k$ to

$$x_{k+1} = (x_k + w) \mod{2^n}.$$ where $w$ is the $n$-bit long frequency control word. To simplify the analysis we can assume that $x_0 = 0$. Note that the nonnegative variable $k$ counts the rising edges of $s(t)$ and it is the discrete-time reference for the Flying-Adder.

Figure 1: Input Phases to the Flying-Adder

Register’s value, $x_k$, is truncated by keeping the first $m$ most significant bits. This defines the phase-selection variable

$$y_k = x_k \div \text{div} 2^{n-m}$$ which drives the MUX. Signal $s(t)$, a sequence of spikes and pulses, is fed to the D-Flip-Flop which acts as a frequency divider by-2 generating an output clock-cycle in $v(t)$ for every two consecutive rising edges (or spikes) of $s(t)$.

A. Example of Flying-Adder’s Operation

Consider the case where $n = 4$, $m = 2$ and frequency word is $w = 7$. Figure 3 presents the signals in the Flying-Adder. The x-axis is the (real) time axis in multiples of $\Delta$. The four input phases, $\Phi_i, i = 1,2,3,4$, are shown in Figure 3a.
The input phase, $\Phi_i$, propagating to the output is selected by the MUX and it is $s(t) = \Phi_{y_k}(t)$. The time intervals within which each of the phases $\Phi_i$, $i = 1, 2, 3, 4$ is selected are indicated with thick line segments in Figure 3a.

By definition, the discrete-time $k$, shown in Figure 3f, is the result of counting the rising edges in $s(t)$. All activity in the Flying-Adder takes place at the rising edges of $s(t)$. The discrete-time has value $k$ between the $k$th and $k+1$ rising edges.

The sequence $d_k$, shown in part Figure 3d, is defined as

$$d_k = (y_k - y_{k-1}) \mod 2^m$$

and has the property that $d_k > 0$ if and only if the $k$th rising edge of signal $s(t)$ results in a change of value from $y_{k-1}$ to $y_k$. Such a change results in a change of the selected phase, and, a $k+1$ rising edge appearing $d_k \cdot \Delta$ seconds later. E.g. the 2nd rising edge of $s(t)$ appears at $t = \Delta$ in Figure 3e. Also, since $y_1 = 1$ and $y_2 = 3$, it is $d_2 = 2$ and the next rising edge appears at $t = 3\Delta$.

![Figure 2: The Flying-Adder architecture (following [5] - with 8 input phases)](image)

The average frequency, of the output $v(t)$, defined as the number of cycles in $v(t)$ within a period $T_v$ divided by $T_v$ (see [6]), is derived using the above results. It is

$$T_v = \Delta \cdot \left\{ \begin{array}{ll} \frac{2^n - (2^m - 1) w \cdot L}{2^{n-m}} & \text{if } 0 < w < 2^{n-m} \\
\frac{w \cdot L}{2^{n-1}} & \text{if } 2^{n-m} \leq w < 2^n \text{ and } L = 1 \\
\frac{w \cdot L}{2^n} & \text{if } 2^{n-m} \leq w < 2^n \text{ and } L > 1 \\
\end{array} \right.$$
B. Example of Sequencies and Periods

For the case of $n = 4$, $m = 2$ and $w = 7$, see also the graphs in Figure 3, the discrete-time period is $L = 4$.

Starting with initial value $x_0 = 0$ we calculate, $x_1 = 7$, $x_2 = 14$, $x_3 = 5$, $x_4 = 12$, $x_5 = 3$, $x_6 = 10$, ..., using $x_{k+1} = (x_k + w) \mod 2^4$. From these values we derive $y_0 = 0$ we calculate, $y_1 = 1$, $y_2 = 3$, $y_3 = 1$, $y_4 = 3$, $y_5 = 0$, $y_6 = 2$ and so on, using equation $y_k = x_k \div 2^2$.

Then we derive sequence $d_1 = 1$, $d_2 = 2$, $d_3 = 2$, $d_4 = 2$, $d_5 = 1$, $d_6 = 2$, .... using $d_k = (y_k - y_{k-1}) \mod 2^2$. Note that since $d_k > 0$ it is $d_k = \delta_k$ as well.

Figure 3: The signals of the Flying-Adder synthesizer for the case where $n = 4$, $m = 2$ and $w = 7$. 
expressed as a Fourier series. Since the spectrum can be easily derived numerically.

Finally, the period of the output signal is

\[ \text{output signal} = \Delta \cdot \Delta \cdot \Delta \]

and within every continuous-time period \( T_v \) of \( v(t) \) there is at least one cycle of length equal to each of these two values.

The lemma allows us to determine upper bounds of pulse-to-pulse jitter. Moreover, it allows to bound the fractional jitter (jitter / period of signal) using the expression for \( f_{ave} \). The next lemma provides the long-term deterministic jitter.

Lemma 2: Let \( 2^{n-m} \leq w < 2^n \) and let \( \hat{t}_j \) and \( \bar{\tau}_j \) be the times of the \( j \)-th rising and falling edges respectively of a 50% duty-cycle periodic square wave of period equal to \( f_{ave} \) and zero initial phase, and, let \( t_j \) and \( \tau_j \) be the times of the \( j \)-th rising and falling edges respectively of \( v(t) \). Then,

\[ \hat{t}_j - \Delta < t_j \leq \hat{t}_j \quad \text{and} \quad \bar{\tau}_j - \Delta < \tau_j \leq \bar{\tau}_j. \]

CONCLUSIONS

The Flying-Adder frequency synthesizer has been studied mathematically and its deterministic jitter has been estimated. Moreover, its average frequency and its spectrum have also been derived. The analytical results have been verified using MATLAB.

REFERENCES