Design and Implementation of a Forward Two-PLL Diophantine Frequency Synthesizer with $500\times$ Resolution Improvement

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***Abstract*— The design, implementation and measurements of a Forward two-PLL Diophantine Frequency Synthesizer are presented. This case study illustrates how the Diophantine Frequency Synthesis (DFS) methodology[1], introduced at the IEEE Frequency Control Symposium of 2006, is used to design a two-PLL synthesizer with frequency resolution 500 times finer than that of the two constituent PLLs while maintaining the PLLs' phase-comparator frequencies, loop-bandwidths, frequency ranges and spectral purity. The Diophantine frequency synthesizer is driven by a $30\,MHz$ input reference and provides an output frequency range of $0-30\,MHz$ with $60\,Hz$ resolution when the output-frequency resolutions of the two constituent PLLs are $29\,kHz$ and $31\,kHz$.**

I. Introduction

The Diophantine Frequency Synthesis (DFS) methodology was introduced in [1] and expanded in [2] for designing frequency synthesis architectures with fast frequency hopping, very high resolution (small frequency step) and low spurs, especially near-in. These combined properties made DFS a potential alternative to Fractional-N PLLs and Direct Digital Synthesizers in cases where spectral purity cannot be traded-off for frequency resolution [3], [4].

DFS is based on mathematical properties of integer numbers and can be implemented by employing two or more frequency synthesis blocks like Integer-N PLLs[2] that are driven by the same reference, and, whose output frequencies are added (or subtracted) to give the output frequency of the synthesizer. DFS results in modular implementations with lower circuit complexity than conventional multi-loop architectures [5], [6], and distributes the synthesizer's frequency resolution among the constituent PLLs.

The paper presents the design, implementation and measurements of a Forward two-PLL DFS synthesizer with output-frequency range $0-30\,MHz$ and frequency step (constant and) approximately $60\,Hz$. The phase-comparator frequencies of the constituent PLLs are approximately $59\,kHz$ and $61\,kHz$, and, their output-frequency steps are about $29\,kHz$ and $31\,kHz$ respectively (due to an additional output frequency divider). Therefore the resolution of the DFS synthesizer is about $\times 500$ that of the constituent PLLs.

Some basic facts of the DFS theory are summarized in the following section, details are available in [2], to make this work more accessible to the reader. Spectral measurements of the synthesized frequency signals support the above statements.

[1]Patent Pending

[2]Although practically any frequency synthesis architecture can be used as a constituent block of DFS, Integet-N PLL is perhaps the simplest and most convenient choice.

II. Basic Concepts of DFS

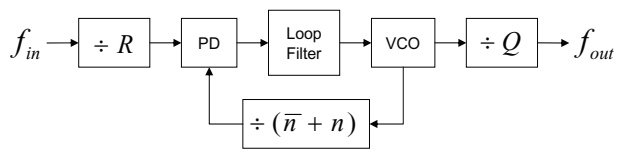

Fig. 1. Basic PLL

DFS uses two or more basic frequency synthesis blocks, and, it is easiest to explain when these blocks are Integer-N PLLs, like that in Fig. 1. The frequency dividers of the PLL should have the following properties: the prescaler divider R, is fixed, the feedback divider is $\bar{n}+n$ where integer $\bar{n}$ is fixed and $\bar{n}>R$, and, the integer variable n can take every value in the range $-R, -R+1, \ldots, R$. Note that it is always $\bar{n}+n>0$. An output divider, Q, may also be present and the output frequency of the PLL is

$$f_{out} = \frac{\bar{n}+n}{Q\times R}\, f_{in}.$$

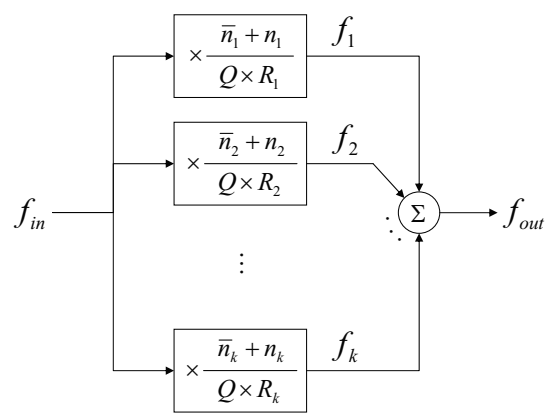

Fig. 2. Abstract high-level k-PLLs DFS scheme.

Fig. 2 shows the general abstract high-level k-PLL DFS architecture. The PLLs, with parameters Q, R_i, n_i and $\bar{n}_i$, $i=1,2,\ldots,k$, are driven by the same signal and their output frequencies are added (or subtracted) resulting in the output

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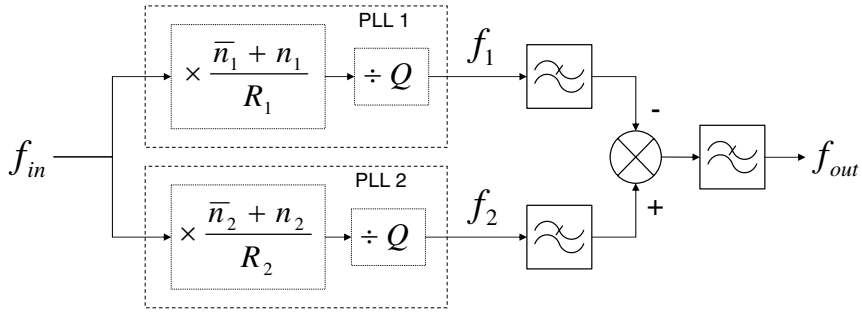

Fig. 3. Architecture of the two-PLL Diophantine synthesizer

frequency f_{out} of the synthesizer.

$$f_{out} = \bar{f}_{out} + \left(\sum_{i=1}^{k} \alpha_i \frac{n_i}{R_i} \right) \frac{f_{in}}{Q} \tag{1}$$

where $\bar{f}_{out}$ is fixed and equal to

$$\bar{f}_{out} = \left(\sum_{i=1}^{k} \alpha_i \frac{\bar{n}_i}{R_i} \right) \frac{f_{in}}{Q} \tag{2}$$

and $\alpha_i \in \{-1, 1\}$, $i = 1, 2, \ldots, k$, are the frequency - weighting coefficients, whose values correspond to whether a frequency is added or subtracted from the general sum in the mixing process.

Now we focus on the first term in the right side of (1), which is variable. DFS' main theorem follows [2].

Theorem 2.1: [2] If $R_1, R_2, \ldots, R_k$ are pairwise relatively prime positive integers (i.e., no pair of them has common divider other than ± 1) then, for every integer n, such that $-R_1 R_2 \cdots R_k \leq n \leq R_1 R_2 \cdots R_k$ we can find $n_1, n_2, \ldots, n_k$ with $-R_i \leq n_i \leq R_i$, for all $i = 1, 2, \ldots, k$, for which

$$\sum_{i=1}^{k} \alpha_i \frac{n_i}{R_i} = \frac{n}{R_1 R_2 \cdots R_k}. \tag{3}$$

Theorem 2.1 along with equation (1) imply that by appropriately adjusting the feedback dividers, n_i's (and therefore the PLL frequencies), the output frequency, f_{out}, can take all values within the range

$$\left[\bar{f}_{out} - \frac{f_{in}}{Q} \ , \ \bar{f}_{out} + \frac{f_{in}}{Q} \right] \tag{4}$$

with *uniform* frequency step equal to

$$f_{step} = \frac{f_{in}}{Q\, R_1 R_2 \cdots R_k}. \tag{5}$$

A significant advantage of DFS, implied by (4) and (5), is that with small values of k, $R_1, R_2, \ldots, R_k$ and Q, the frequency step, f_{step}, can be made very small, while at the same time, the phase-comparator frequencies of the PLLS, f_{in}/R_i, $i = 1, 2, \ldots, k$, can be large.

The *Resolution Gain*, R_G, of a DFS scheme measures the improvement in resolution resulting by applying DFS. It is defined as the geometric mean of the output-frequency steps of the constituent PLLs divided by the frequency step of the (whole) DFS scheme. It is

$$R_G = \left(R_1 R_2 \cdots R_k \right)^{\frac{k-1}{k}} \tag{6}$$

III. Forward Two-PLL DFS Synthesizer

The high level schematic of the synthesizer is shown in Figure 3. The reference frequency is $f_{in} = 30\,MHz$, the output frequency range is $f_{out} = 0, \ldots, 30\,MHz$ and the output frequency step is $\delta f_{out} \approxeq 60\,Hz$.

The frequency ranges of the two PLLs are $f_1 = 75\,MHz, \ldots, 105\,MHz$ and $f_2 = 90\,MHz, \ldots, 120\,MHz$, and, their frequency steps are $\delta f_1 \approxeq 29\,kHz$ and $\delta f_2 \approxeq 31\,kHz$ respectively. The resolution gain of the synthesizer is about 500.

The two PLLs are part of the (single-chip) triple-PLL device CDCE706 by Texas Instruments and the mixer is realized using the multiplier AD835 by Analog Devices. The worst case spurious free dynamic range of the PLLS is $50 - 55\,dBc$. The ranges of the prescaler, feedback and output dividers are shown in Table I.

Divider	Min	Max
$\bar{n}_i + n_i$	1	4095
R_i	1	511
Q	1	127

TABLE I
Ranges of the Frequency Dividers

A. Selection of the DFS Parameters

The desirable output-frequency range of the synthesizer is $0 - 30MHz$. DFS theory implies the output-frequency range given by (4). Therefore, we would like to have

$$\bar{f}_{out} - \frac{f_{in}}{Q} = 0\,Hz$$
$$\bar{f}_{out} + \frac{f_{in}}{Q} = 30\,MHz.$$

Since $f_{in} = 30\,MHz$, these two equations give

$$\bar{f}_{out} = 15MHz\ , \quad Q = 2 \tag{7}$$

The additional advantage of using an even value for Q is that it reduces the even-order harmonics at the outputs of the PLLS.

From Fig. 3 we have that, for each PLL $i = 1, 2$,

$$f_i = \frac{n_i + \bar{n}_i}{R_i} \left(\frac{f_{in}}{Q} \right) \tag{8}$$

Expressions (3) and (8) along with $f_{out} = f_2 - f_1$ (see Fig. 3) and Theorem 2.1 give that

$$f_{out} = \left(\frac{\bar{n}_2}{R_2} - \frac{\bar{n}_1}{R_1} \right) \frac{f_{in}}{Q} + \frac{n}{R_1 R_2} \frac{f_{in}}{Q} \tag{9}$$

where n can take any value from $-R_1R_2$ to R_1R_2 by appropriately programming the values of n_1 and n_2 within their ranges $-R_1 \leq n_1 \leq R_1$ and $-R_2 \leq n_2 \leq R_2$, respectively.

The output-frequency step (resolution) is derived from (5),

$$f_{step} = \frac{f_{in}}{QR_1R_2} = \frac{15MHz}{R_1R_2}. \tag{10}$$

We want $f_{step} \approxeq 60Hz$, therefore from (10) it should be $R_1R_2 \approxeq 15MHz/60Hz = 250,000$. Since $500^2 = 250,000$ one could try setting $R_1 = R_2 = 500$, however, Theorem 2.1 requires that R_1, R_2 are relatively prime, i.e. $gcd(R_1, R_2) = 1$, and, in addition, it is desirable that R_1, R_2 are sufficiently different so that neither the phase-comparator frequencies of the PLLs, f_{in}/R_1 and f_{in}/R_2 nor their harmonics "resonate" [3].

To this end, we can choose the maximum value for $R_1 = 511$ and we "try" $R_2 = \lceil 250,000/511 \rceil = 490$ in order to have resolution equal to or better than $60\,Hz$. But $gcd(490, 511) = 7$ which makes this choice of (R_1, R_2) unacceptable. We can choose $R_2 = 491$ instead since $gcd(491, 511) = 1$. Therefore

$$R_1 = 511\ , \quad R_2 = 491 \tag{11}$$

implying that

$$f_{step} = \frac{30MHz}{2 \cdot 511 \cdot 491} = 59.784..\,Hz \tag{12}$$

Now, from (9) the central output frequency here is

$$\bar{f}_{out} = \left(\frac{\bar{n}_2}{R_2} - \frac{\bar{n}_1}{R_1} \right) \frac{f_{in}}{Q}.$$

Since the given input-reference frequency is $f_{in} = 30\,MHz$, and, $\bar{f}_{out} = 15\,MHz$ and $Q = 2$, from (7), we need to find $\bar{n}_1$, $\bar{n}_2$ satisfying

$$\frac{\bar{n}_2}{R_2} - \frac{\bar{n}_1}{R_1} = 1. \tag{13}$$

Since $gcd(R_1, R_2) = 1$, the general solution of Diophantine equation (13) is, [2],

$$\bar{n}_2 = (m+1)R_2\ , \quad \bar{n}_1 = mR_1. \tag{14}$$

for $m = 0, \pm 1, \pm 2, \ldots$. Also, for the feedback dividers $\bar{n}_i + n_i$, $i = 1, 2$, we have $-R_i \leq n_i \leq R_i$, and so their values are bounded as

$$\begin{array}{rcccl} (m-1)R_1 & \leq & \bar{n}_1 + n_1 & \leq & (m+1)R_1 \\ mR_2 & \leq & \bar{n}_2 + n_2 & \leq & (m+2)R_2 \end{array}$$

From the limits of the sizes of the feedback dividers in Table I these inequalities imply that

$$2 \leq m \leq \min\left(\frac{4095}{R_1} - 1, \frac{4095}{R_2} - 2\right) = 6$$

The higher the value of m is, the closer the ratio f_2/f_1 is to 1, which may result in lower spur generation in the mixer (of course, very large m means also large f_1, f_2 and perhaps unnecessarily increased phase noise at the output of the synthesizer).

Lets choose $m = 6$ and verify this is an appropriate choice. The VCO frequencies are (see Fig. 3)

$$f_{VCO_i} = \frac{\bar{n}_i + n_i}{R_i} f_{in}$$

and so from (14), $\max f_{VCO_1} = (m+1)f_{in} = 210MHz$ and $\max f_{VCO_1} = (m+2)f_{in} = 240MHz$ which are both within the specifications of the CDCE706 device which has a maximum VCO frequency of $300MHz$. Also, from (14) and $m = 6$ we get $\bar{n}_1 = 3066$ and $\bar{n}_2 = 3437$.

Our derivations and choices are summarized below:

$$\begin{array}{lll} R_1 = 511\ , & \bar{n}_1 = 3066\ , & Q = 2 \\ R_2 = 491\ , & \bar{n}_2 = 3437 & \end{array}$$

which imply

$$\bar{f}_1 = \frac{\bar{n}_1}{R_1 Q} f_{in} = \frac{3066}{511 \cdot 2}\, 30\,MHz = 90\,MHz$$

and

$$\bar{f}_2 = \frac{\bar{n}_2}{R_2 Q} f_{in} = \frac{3437}{491 \cdot 2}\, 30\,MHz = 105\,MHz.$$

Finally, following the DFS guidelines, the ranges of the feedback dividers are

$$\begin{array}{rcccl} 3066 - 511 & \leq & \bar{n}_1 + n_1 & \leq & 3066 + 511 \\ 3437 - 491 & \leq & \bar{n}_2 + n_2 & \leq & 3437 + 491 \end{array} \tag{15}$$

The above choices of the prescalers and output dividers and the ranges of the feedback dividers result in the DFS scheme with frequencies given in Table II.

	Min	Central	Max	Step
f_{in}	-	30,000,000	-	-
f_1 (PLL 1)	75,000,000	90,000,000	105,000,000	29,354
f_2 (PLL 2)	90,000,000	105,000,000	120,000,000	30,550
f_{out} (DFS)	0	15,000,000	30,000,000	60

TABLE II

FREQUENCY RANGES & RESOLUTIONS OF SIGNALS (HZ) OF THE DIOPHANTINE SYNTHESIZER (VALUES ARE ROUNDED TO 1HZ).

IV. RESULTS

By programming the two PLLs with the DFS parameters derived in Section III-A and using the DFS algorithm [2] along with equation (9), we can generate all predicted frequencies

$$\begin{array}{rcl} f_{out} & = & 15\,MHz + n \cdot 59.784..\,Hz \\ n & = & -250,901 \ldots 250,901. \end{array} \tag{16}$$

Given a desirable value of n, parameters n_1 and n_2 are derived using the DFS algorithm in [2].

The frequency ranges and resolutions (steps) of the PLLs and of the output signal are shown in Table II.

The two-PLL DFS scheme achieves frequency resolution of about $60\,Hz$ with phase-comparator frequencies of the constituent PLLs being

$$\begin{array}{rcl} f_{PC_1} & = & 58,708.41 \ldots\,Hz \\ f_{PC_2} & = & 61,099.79 \ldots\,Hz. \end{array}$$

	n_1	n_2	n	f_1	f_2	$f_2 - f_1$
D_1	372	1	$-182,141$	$100,919,765$	$105,030,550$	$4,110,785$
D_2	91	-269	$-182,140$	$92,671,233$	$96,782,077$	$4,110,845$
D_3	321	-48	$-182,139$	$99,422,701$	$103,533,605$	$4,110,904$
D_4	40	-318	$-182,138$	$91,174,168$	$95,285,132$	$4,110,964$
D_5	270	-97	$-182,137$	$97,925,636$	$102,036,660$	$4,111,024$

Fig. 4. Frequency Ranges and Frequency Steps (Resolutions) of the signals in the DFS scheme. All Frequencies are in Hz (rounded).

This allows for *fast frequency hopping* and easy suppression of the potential phase-comparator spurs in the PLLs. Along with careful frequency choices and circuit design clean output spectrum is achieved.

The spectra of the output signal, for five consecutive frequencies, are graphically superimposed in Fig. 6. Note that the triangular shapes are due to the limitation of $10\,Hz$ resolution bandwidth of the Spectrum Analyzer (smallest BW resolution of the instrument).

The five frequencies in Fig. 6 are the differences $f_2 - f_1$ in the table of Fig. 4. Figure 5 shows graphically the triplets $(f_1, f_2, f_2 - f_1)$ illustrating that small (minimal here) steps in $f_2 - f_1$ are the result of large but "simultaneous" changes in f_1 and f_2.

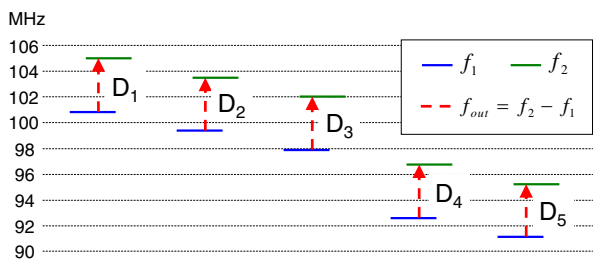

Fig. 5. Graphical representation of the results in the table of Fig. 4

The achieved frequency step is $60\,Hz$, compared to the $29\,kHz$ and $30\,kHz$ frequency steps of the two PLLs. The resolution gain (see Section II) of the Diophantine synthesizer is $R_G = \sqrt{R_1 R_2} \approxeq 501$.

V. Conclusions

The design of a forward two-PLL Diophantine frequency synthesizer has been presented and application aspects of the Diophantine Frequency Synthesis (DFS) methodology have been discussed.

The achieved frequency resolution is $\times 500$ times better than that of the two constituent PLLs without any sacrifice in their loop bandwidths or spectral purity. This is part of the properties of DFS which allows for independent choices of the output frequency step (resolution) and the phase-comparator frequencies of the PLLs leading to very fine resolution and fast frequency hopping architectures with low spurs, especially in the vicinity of the carrier.

Spectral measurements demonstrate the resolution of the architecture and the spectral purity of the output signal.

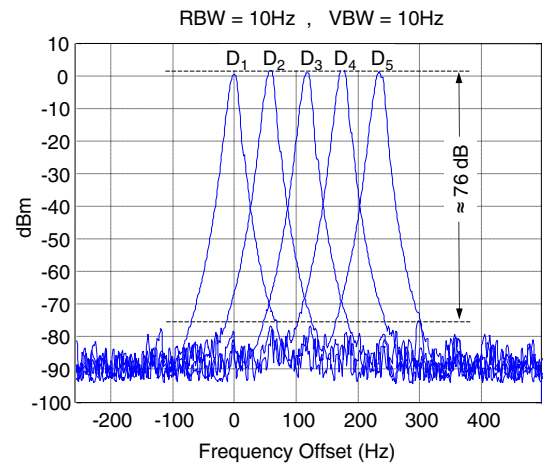

Fig. 6. Five consecutive synthesized frequencies, D_1-D_5 corresponding to values shown in the table of Fig. 4. The frequency step is $60\,Hz$ while the frequency steps of the two PLLs are about $29\,kHz$ and $31\,kHz$. PLLs' phase-comparator frequencies are $59\,kHz$ and $61\,kHz$ respectively. For the measurement: RBW=$10\,Hz$, VBW=$10\,Hz$ - the five spectra have been graphically superimposed. Note that the triangular shapes are due to the limitation of $10\,Hz$ resolution bandwidth of the Spectrum Analyzer (smallest RBW available).

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