# Two-PLL Forward Diophantine Frequency Synthesizer

Paul P. Sotiriadis, Andradige Silva

Electrical and Computer Engineering, Johns Hopkins University

***Abstract*— Diophantine Frequency Synthesis[1] (DFS) is a new approach to high-resolution, fast-hopping, low-spurs frequency synthesis. DFS is based on mathematical properties of integer numbers and employs two or more Phase-Locked Loops (PLL)s to achieve frequency resolution arbitrary smaller than the phase-comparator frequencies of the constituent PLLs. A two-PLL DFS synthesizer is presented that achieves frequency resolution about $100$ times finer than that of the two constituent PLLs. It has output frequency range $195 - 205\,MHz$ and frequency step $542\,Hz$. Measurements demonstrate the resolution of the architecture and the spectral purity of the output signal.**

## I. Introduction

Most of the modern engineering systems involve a frequency synthesis block. It may be a simple Integer-N PLL, like the ones in digital processors or a complex one like those in timing systems and atomic clocks [1]-[2].

Diophantine Frequency Synthesis[1] (DFS) [3]-[4] is a new methodology for designing frequency synthesis architectures having fast frequency hopping, high resolution (small frequency step) and low spurs (especially in the vicinity of the carrier), simultaneously, with relatively low circuit complexity.

DFS is based on mathematical properties of integer numbers and Diophantine equations [5]. DFS architectures employ two or more basic phase locked loops (PLL)s whose output frequencies are added (or subtracted) to give the output frequency of the synthesizer.

DFS *distributes* the frequency resolution among the PLLs. Some basic facts of DFS theory are presented in the following section. More details are available in [3].

The paper presents a forward two-PLL DFS architecture and a circuit implementation. It illustrates how the high-level DFS methodology can be realized using commercially available multi-PLL devices to form a frequency synthesizer with much higher resolution than those of the constituent PLLs, with affecting their hopping speed or loop bandwidths.

Specifically, the output-frequency steps of the constituent PLLs, are about $43\,kHz$ and $67\,kHz$ while the steps of the synthesizer are $542\,Hz$. The (used) frequency ranges of the PLLs are $10\,MHz$ wide and the output frequency range of the synthesizer is $195 - 205\,MHz$.

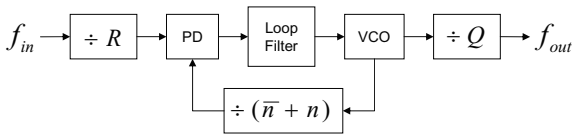


Fig. 1. Basic PLL

## II. Basics of DFS

DFS uses two or more basic PLLs like that in Fig. 1[2] that have fixed *prescaler* divider $R$. The feedback divider is the sum $\bar{n} + n$, of a fixed value $\bar{n}$, and, a variable $n$ which can take both *negative* and *positive* values within a predefined range. For all values of $n$, the sum $\bar{n} + n$ is positive. An output divider may be present and the output frequency of the PLL is

$$f_{out} = \frac{\bar{n} + n}{Q \times R} f_{in}.$$

The general high-level $k$-PLL DFS architecture is shown in Fig. 2. The PLLs, with parameters $R_i$, $n_i$ and $\bar{n}_i$, $i = 1, 2, \ldots, k$, are driven by the same signal and their output frequencies are added (or subtracted) to provide the output

[1]Patent Pending

[2]The Phase Detector (PD) could also be a Phase-Frequency Comparator or equivalent circuit-block. An output divider, $Q$, may be present but it is not necessary for DFS.

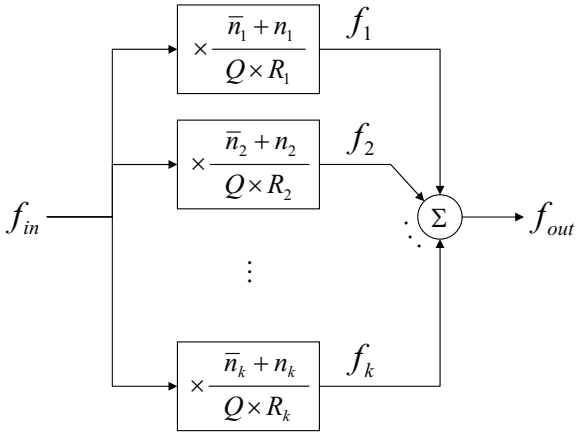


Fig. 2. Abstract $k$-PLLs DFS scheme.

frequency of the synthesizer,

$$f_{out} = \left(\frac{n_1}{R_1} + \frac{n_2}{R_2} + \ldots + \frac{n_k}{R_k}\right)\frac{f_{in}}{Q} + \left(\frac{\bar{n}_1}{R_1} + \frac{\bar{n}_2}{R_2} + \ldots + \frac{\bar{n}_k}{R_k}\right)\frac{f_{in}}{Q} \quad (1)$$

The second term in the RHS of (1) is fixed. We set

$$\bar{f}_{out} = \left(\frac{\bar{n}_1}{R_1} + \frac{\bar{n}_2}{R_2} + \ldots + \frac{\bar{n}_k}{R_k}\right)\frac{f_{in}}{Q} \quad (2)$$

Now we focus on the first term in the right side of (1), which is variable. DFS' main Theorem follows [3].

*Theorem 2.1:* [3] If $R_1, R_2, \ldots, R_k$ are pairwise relatively prime positive integers (i.e., no pair of them has common divider other than $\pm 1$) then, for every integer $n$, such that $-R_1R_2\cdots R_k \leq n \leq R_1R_2\cdots R_k$ we can find $n_1, n_2, \ldots, n_k$ with $-R_i \leq n_i \leq R_i$, for all $i = 1, 2, \ldots, k$, for which

$$\frac{n_1}{R_1} + \frac{n_2}{R_2} + \ldots + \frac{n_k}{R_k} = \frac{n}{R_1R_2\cdots R_k}. \quad (3)$$

Rephrasing Theorem 2.1 and using equation (1) we conclude that by appropriately adjusting the feedback dividers, $n_i$'s (and therefore the PLL frequencies), the output frequency, $f_{out}$, can take all values within the range

$$\left[\ \bar{f}_{out} - \frac{f_{in}}{Q}\ ,\ \bar{f}_{out} + \frac{f_{in}}{Q}\ \right]$$

with *uniform* frequency step

$$f_{step} = \frac{f_{in}}{Q\, R_1R_2\cdots R_k}.$$

Note that if some of the PLL frequencies, $f_1, f_2, \ldots, f_k$ were subtracted, instead of being added to the general sum, i.e. if $n_i/R_i$ were replaced by $-n_i/R_i$ for some indices $i$ in (3), the length of the output frequency range would also be $2f_{in}/Q$, i.e. exactly the same as before, because the ranges of $n_1, n_2, \ldots, n_k$ are symmetric with respect to 0. The output frequency step, $f_{step}$, would also remain unchanged.

An advantage of DFS is that with small values of $k$, $R_1, R_2, \ldots, R_k$ and $Q$, the frequency step, $f_{step}$, can be made very small, while at the same time, the phase-comparator frequencies of the PLLS, i.e. $f_{in}/R_i$, $i = 1, 2, \ldots, k$, and the output frequency range are large.

## III. A Two-PLL Forward-DFS Scheme

The purpose of the paper is to present a DFS example, and, not to repeat well-know facts regarding PLL and frequency mixer design. To this end, it was preferred to trade design time with performance and use Texas Instruments' programmable triple-PLL CDCE706 device which automatically adjusts its loop-filter parameters and VCO's tuning ranges. It is noted however that this design

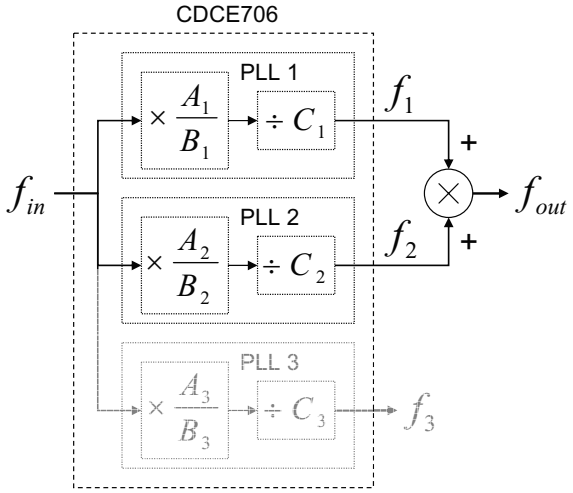


Fig. 3. High-level two-PLL DFS architecture

convenience is paid by SFDR of 50 to $55\,dB$, according to the specifications of the device.

Two of the three PLLs in CDCE706 were employed in the DFS scheme. The high level architecture is shown in Fig. 3. The range of the prescaler, feedback and output dividers are $A_i : 1 - 4095$, $B_i : 1 - 511$ and $C_i : 1 - 127$.

The total range of the VCO's is $80\ MHz - 300\ MHz$ therefore implying (see Fig. 3) that

$$80\ MHz \leq \frac{A_i}{B_i} f_{in} \leq 300\ MHz.$$

### A. Choosing the DFS Parameters

The desirable is to achieve frequency range $195 - 205\,MHz$ with high frequency resolution while maintaining relatively high phase-comparator frequencies in the constituent PLLs.

From Fig. 3 we have that, for each PLL $i = 1, 2$,

$$f_i = \frac{A_i}{B_iC_i}\, f_{in}, \quad (4)$$

the VCO's frequencies are

$$f_{VCO_i} = \frac{A_i}{B_i}\, f_{in} \quad (5)$$

and the phase-comparators frequencies are

$$f_{PC_i} = \frac{f_{in}}{B_i} \quad (6)$$

Now the frequency dividers in expressions (4) can be written as

$$B_iC_i = R_iQ, \quad (7)$$

$i = 1, 2$, where $Q = \gcd(B_1C_1, B_2C_2)$ implying $\gcd(R_1, R_2) = 1$, i.e. $R_1$, $R_2$ are relatively prime as it is required by Theorem 2.1. Moreover, we can express

$A_i = n_i + \bar{n}_i$ (and impose the constraint required from the Theorem, i.e., $-R_i \leq n_i \leq R_i$ ) so from (4) we have

$$f_i = \frac{n_i + \bar{n}_i}{R_i} \left( \frac{f_{in}}{Q} \right) \tag{8}$$

From (3) and (8), the fact that we have chosen $f_{out} \triangleq f_1 + f_2$ (see Fig. 3) and Theorem 2.1 we have

$$f_{out} = \left( \frac{\bar{n}_1}{R_1} + \frac{\bar{n}_2}{R_2} \right) \frac{f_{in}}{Q} + \frac{n}{R_1 R_2} \frac{f_{in}}{Q} \tag{9}$$

with $n$ ranging from $-R_1R_2$ to $R_1R_2$. Therefore $f_{out}$ ranges from $\bar{f}_1 + \bar{f}_2 - f_{in}/Q$ to $\bar{f}_1 + \bar{f}_2 + f_{in}/Q$.

Since the desirable output range of the synthesizer is $195 - 205\,MHz$, it is $\bar{f}_1 + \bar{f}_2 - f_{in}/Q = 195\,MHz$ and $\bar{f}_1 + \bar{f}_2 + f_{in}/Q = 205\,MHz$, and so

$$\frac{f_{in}}{Q} = 5\,MHz \tag{10}$$

The input (reference) frequency used is $f_{in} = 64MHz$, and so $f_{in}/5MHz = 12.8$. Therefore *the maximum value of $Q$ resulting in at least $10MHz$ of output range is*

$$Q = 12 \tag{11}$$

We choose to have the ranges of the constituent PLLs near $100\,MHz$. This along with the frequency limits of the VCO's in the PLLs allow $C_i$s to take any of the three values $\{1, 2, 3\}$. However, we don't want both of them to take the maximum possible value, because if $C_1 = C_2 = 3$ then they contribute only a factor of 3 to the product $R_1R_2Q$ and this "improves" frequency resolution (see Eq. (9)) only by 3. In contrast, we set

$$C_1 = 3 \text{ and } C_2 = 2 \tag{12}$$

which contribute[3] a factor of 6 to $R_1R_2Q$.

To simplify the rest of the derivation we assume that $C_1$ and $C_2$ are factors of $R_1$ and $R_2$ respectively, i.e. equivalently that the common divider, $Q$, of $B_1C_1$ and $B_2C_2$ is entirely a factor of $B_1$ and $B_2$ and so because of (11) it is

$$B_1 = 12X \text{ and } B_2 = 12Y \tag{13}$$

for some integers $X$ and $Y$. Note however that from the ranges of the feedback and prescaler dividers ( Section III) we have

$$X, Y \leq 511/12 = 42.583\ldots. \tag{14}$$

To maximize the product $R_1R_2Q$, and therefore the resolution of the synthesizer, we could try to give $X$ and $Y$ their maximum possible values, i.e. $X = 42$ and $Y = 41$, or, $X = 41$ and $Y = 42$.

In the first case we get $B_1C_1 = 1512$ and $B_2C_2 = 984$ which imply $Q = gcd(1512, 984) = 24$, $R_1 = 63$ and $R_2 = 41$ and so $R_1R_2Q = 61,992$; in the second case we get $R_1R_2Q = 41,328$.

In contrast if we choose $X = 41$ and $Y = 40$, i.e. slightly smaller values, we end up with $Q = 12$, $R_1 = 123$ and $R_2 = 80$ giving $R_1R_2Q = 118,080$. We finally get

$$B_1 = 12 \cdot 41 = 492 \text{ and } B_2 = 12 \cdot 40 = 480 \tag{15}$$

The following set of equations summarizes the derivations up to now:

$$\begin{aligned} B_1 = 492 \quad C_1 = 3 \quad R_1 = 123 \\ B_2 = 480 \quad C_2 = 2 \quad R_2 = 80 \end{aligned}$$

Now, we would like the output frequencies of the PLLs to be close to $100\,MHz$ but we have to make sure that their harmonics and dominant IMD products of the mixer are as far away of the output range of interest, i.e. $195 - 205\,MHz$, as possible. One choice that allows for $\geq 20\,MHz$ gap between the desirable output range and major spurs is the following:

$$\bar{n}_1 = 1903 \text{ and } \bar{n}_2 = 1762 \tag{16}$$

which give

$$\bar{f}_1 = \frac{\bar{n}_1}{B_1C_1} f_{in} = \frac{1903}{492 \cdot 3}\, 64\,MHz = 82,514,905.1\,Hz$$

and

$$\bar{f}_2 = \frac{\bar{n}_2}{B_2C_2} f_{in} = \frac{1762}{480 \cdot 2}\, 64\,MHz = 117,466,666.7\,Hz.$$

Finally, following the DFS guidelines, the ranges of the dividers $A_1$ and $A_2$ are

$$\begin{aligned} 1903 - 123 \leq A_1 \leq 1903 + 123 \\ 1762 - 80 \leq A_2 \leq 1762 + 80 \end{aligned} \tag{17}$$

The above choices of the prescalers and output dividers and the ranges of the feedback dividers result in the DFS scheme with frequencies given in Table I. Note that the frequency step of the whole architecture is about two orders of magnitude smaller than those of the constituent PLLs.

### *B. The Mixer*

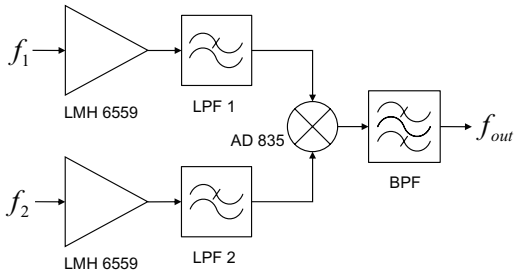


Fig. 4. Mixer, Low-Pass Filters and Buffers

[3]One has to decide how to "form" the greatest common divider of the pair $R_1Q_1$ and $R_2Q_2$...

The high-level schematic of the mixer is shown in Figure 4. The mixer is based on the four-quadrant multiplier AD835 chosen for its high linearity and appropriate bandwidth[4]. Two wide-band buffers, LMH6559, are used to isolate the PLLs from the filters and the multiplier and reduce backward signal leakage.

The two low-pass filters LPF1 and LPF2 are $7^{th}$ order Chebyshev Type-I with passive ladder implementations and $1\,dB$ ripple in the pass-band. They remove the harmonics of the square-wave signals coming from the PLLs and feed clean sinusoidals to the multiplier. The third filter, BPF, following the multiplier, is an $8^{th}$ order, $3\,dB$ ripple Elliptic band-pass one that removes the off-band spurs from the mixing and the harmonics of the PLLs leaking through the mixer.

## IV. Results

Programming the two PLLs using the DFS parameters derived in Section III-A and the DFS algorithms in [3], it was possible to generate all predicted frequencies

$$f_{out} \;=\; 199,981,572\,Hz + n \cdot 542\,Hz \qquad (18)$$

with integer $n$ ranging within (note that $123 \times 80 = 9840$)

$$n \;=\; -9840 \ldots 9840. \qquad (19)$$

Given the desirable value of $n$, parameters $n_1$ and $n_2$ are derived using the theory and algorithms in [3]. The frequency ranges of the PLLs and the output signal, along with their resolutions, are shown in Table I.

| | Min | Central | Max | Step |
|---|---|---|---|---|
| $f_{in}$ | - | 64.000,000 | - | - |
| $f_1$ (PLL 1) | 77,181,572 | 82,514,905 | 87,848,238 | 43,360 |
| $f_2$ (PLL 2) | 112,133,333 | 117,466,667 | 122,800,000 | 66,667 |
| $f_{out}$ (DFS) | 194,648,238 | 199,981,572 | 205,314,905 | 542 |

TABLE I
Frequency Ranges and Resolutions of the signals in the DFS scheme (in Hz).

Therefore this simple two-PLL DFS scheme achieved frequency resolution of $542\,Hz$ when the phase-comparator frequencies of the PLLs are

$$f_{PC_1} \;=\; 130,081.3\,Hz$$
$$f_{PC_2} \;=\; 133,333.3\,Hz$$

This allows for *fast frequency hopping* and easy removal of the side-band spurs introduced by the phase-comparator, leading to clean output spectrum.

Fig. 5 shows the spectrum of the (output) synthesized signal for four consecutive achievable frequencies. The achieved frequency step is only $542\ Hz$, compared to the $43\ kHz$ and $67\ kHz$ frequency steps of the two PLLs (note the divisions by 3 and 2).

[4]Better noise performance can be achieved by other types of mixers.

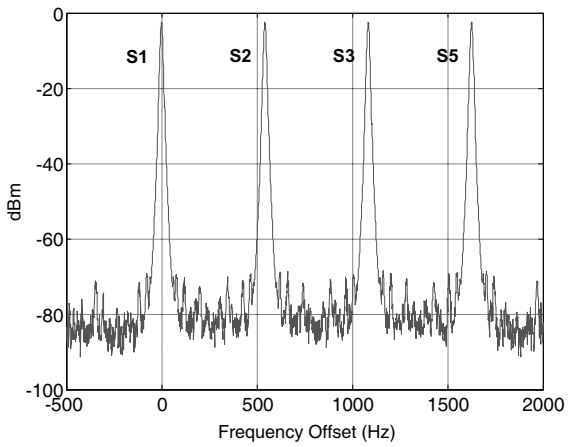


Fig. 5. Four consecutive frequencies, $S_1$: $202,691,599\,Hz$, $S_2$: $202,692,141\,Hz$, $S_3$: $202,692,683\,Hz$, $S_4$: $202,693,225\,Hz$. RBW=10Hz, VBW=10Hz.

The parameters of the synthesizer resulted to the frequencies shown in Fig. 5 are listed below in Table II.

| | $n_1$ | $n_2$ | $n$ | $f_1$ | $f_2$ |
|---|---|---|---|---|---|
| $S_1$ | 1 | 40 | 5,000 | 82,558,266 | 120,133,333 |
| $S_2$ | 21 | 27 | 5,001 | 83,425,474 | 119,266,667 |
| $S_3$ | 41 | 14 | 5,002 | 84,292,683 | 118,400,000 |
| $S_4$ | 61 | 1 | 5,003 | 85,159,892 | 117,533,333 |

TABLE II
Frequency Ranges and Frequency Steps (in Hz)

## V. Conclusions

Application aspects of the Diophantine Frequency Synthesis (DFS) methodology have been presented through the design of a forward two-PLL DFS frequency synthesizer. DFS is based on number theory and Diophantine equations, uses two or more basic PLLs and allows for independent choices for the output frequency step (resolution) and the phase-comparator frequencies of the PLLs.

## References


[1] Vadim Manassewitsch, "*Frequency Synthesizers*" , third edition, John Willey & Sons, 1987.

[2] William F. Egan, "*Frequency Synthesis by Phase Lock*", second edition, John Willey & Sons, 1999.

[3] Paul P. Sotiriadis, "Diophantine Frequency Synthesis, *EEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 53, No. 11, Nov. 2006, pp. 1988-1998.

[4] P. Sotiriadis, "Diophantine Frequency Synthesis; The Mathematical Principles", *IEEE Internat. Symp. on Circuits and Systems 2007*.

[5] Daniel E. Flath, "*Introduction to Number Theory*", John Willey & Sons, 1989.