Diophantine Frequency Synthesis The Mathematical Principles

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***Abstract*— Diophantine Frequency Synthesis[1] is a new approach to fine-step and fast-hopping frequency synthesis that is based on mathematical properties of integer numbers and Diophantine equations. Diophantine Frequency Synthesis overcomes the constraining relationship between frequency step and phase-comparator frequency inherent in conventional phase-locked loops. It leads to fine-step, fast-hopping, modular-structured frequency synthesizers with potentially very low spurs, especially near the carrier.**

I. Introduction

Fine frequency synthesis[2] is important in many applications ranging from scientific instrumentation, atomic clocks, timing systems and satellite navigation, to certain classes of communication and medical systems. Several fine frequency synthesis architectures have been proposed [1]-[2].

Diophantine Frequency Synthesis[1,3] (DFS) is a new approach to fine-step frequency synthesis. It is based on mathematical properties of integer numbers and Diophantine equations [3].

DFS uses two or more basic phase locked loops (PLL)s. The PLLs are driven by the same reference signal and their output frequencies are added (or subtracted) to give the output frequency of the synthesizer. DFS provides the mathematical algorithm for choosing the prescalers and for adjusting the feedback dividers.

DFS results in fractional resolution[4] of the synthesizer equal to the product of the fractional resolutions of the individual PLLs (10^{-10} is typical). Specifically, if $N_1, N_2, \ldots, N_k$ are the prescalers of the PLLs and f_{in} is their (common) input reference frequency, the output frequency step of the synthesizer is $f_{in}/(N_1 N_2 \cdots N_k)$ and the output frequency range is $2f_{in}$.

DFS offers a significant advantage: it leads to PLL-based architectures for which the output frequency step can be extremely small, while, at the same time, the prescalers are small and the phase-comparator frequencies are high. This allows for simultaneously having very high resolution and large loop bandwidths, i.e. fast frequency hopping. In a sense, DFS *distributes* the frequency resolution among the PLLs.

DFS offers the potential for very low spurs close to the carrier, in contrast to other high resolution frequency synthesis architectures like fractional-N synthesizers [2], that suffer from spurious signals or significant noise close to the carrier due to their inherent FM modulation, and the direct digital synthesis that also has spurious signals close to the carrier [4] and whose spectral purity is limited by the digital-to-analog converter.

[1]Patent Pending: Johns Hopkins Univ. Applied Physics Laboratory

[2]The terms "fine (frequency) step", "high resolution" and "fine-frequency synthesis" are used indistinguishably in this paper.

[3]More details can be found in [5].

[4] *Fractional Resolution* $\triangleq$ freq. step / center freq.

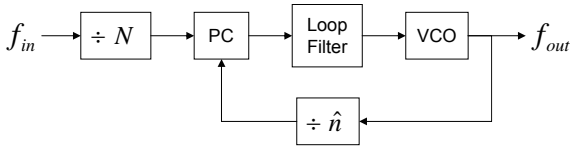

Fig. 1. Basic PLL

II. Notation

DFS uses two or more basic PLLs like the one[5] in Figure 1. Throughout the paper, the *prescaler* divider, N, is assumed fixed. The *feedback divider*, $\hat{n}$, is the sum $\hat{n} = \bar{n} + n$, of a fixed value $\bar{n}$, and, a variable n that can take both *negative and positive values* within a predefined range. For all values of n, $\hat{n}$ is positive. The output frequency of the PLL is $f_{out} = \frac{\hat{n}}{N} f_{in}$.

Since the paper focuses on the mathematical principles of DFS, and not in the technical details of the individual PLLs, Figure 2a is used for convenience instead of Figure 1.

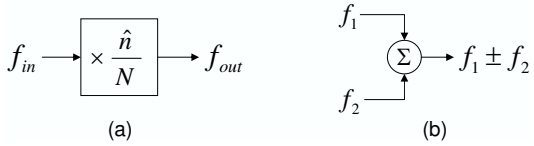

Fig. 2. (a) Simplified schematic of the basic PLL, (b) Mixer

The mixing of two signals at frequencies f_1 and f_2 is denoted as in Figure 2b where the outcome can be either $f_1 + f_2$ or $f_1 - f_2$; the context in the paper indicates whether the sum or the difference is considered. Mixing of three or more signals has a similar interpretation.

III. Inherent Limitations of Phase Locked Loops

Frequency synthesis using a single PLL, like that in Figure 1, implies frequency steps that are equal to the phase-comparator frequency f_{in}/N. This means that having small frequency steps (by using large N and/or small f_{in}) requires having low phase-comparator frequency f_{in}/N as well. The last one implies small loop bandwidth [1], [2] and therefore slow frequency hopping, and potentially increased spurious signals and noise.

DFS overcomes these constraints, allowing for both high phase-comparator frequency and very small frequency step simultaneously.

[5]"PC" may also be phase-frequency comparator or similar block.

IV. DFS: A MOTIVATING EXAMPLE

Consider the simple architecture in Figure 3 consisting of two PLLs whose output frequencies are summed giving

$$f_{out} = \left(\frac{n_1}{3} + \frac{n_2}{5} + \frac{12}{3} + \frac{16}{5} \right) f_{in} \tag{1}$$

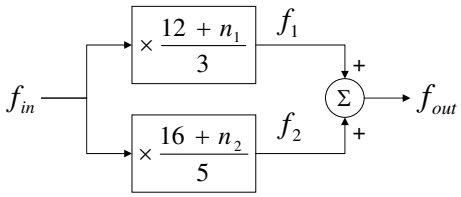

Fig. 3. A simple DFS scheme

The prescalers are 3 and 5 (fixed). Let the feedback dividers, $12 + n_1$ and $16 + n_2$, be variable with

$$-3 \le n_1 \le 3 \quad \text{and} \quad -5 \le n_2 \le 5$$

i.e. the range of each feedback divider is twice the size of the corresponding prescaler[6]. Then, f_1 can take any of the 7 values:

$$f_1 \in \left\{ \frac{9}{3} f_{in}, \frac{10}{3} f_{in}, \frac{11}{3} f_{in}, \ldots, \frac{15}{3} f_{in} \right\} \tag{2}$$

and f_2 can take any of the 11 values:

$$f_2 \in \left\{ \frac{11}{5} f_{in}, \frac{12}{5} f_{in}, \frac{13}{5} f_{in}, \ldots, \frac{21}{5} f_{in} \right\} \tag{3}$$

Table I shows a set of output frequencies f_{out} that can be synthesized by appropriately setting n_1 and n_2 *within their specified ranges*. Table I demonstrates three properties of the simple DFS scheme in Figure 3 that also extend to the general DFS architectures.

Property 1: The frequency step is *constant* and equals

$$frequency\ step = \frac{f_{in}}{15} = \frac{f_{in}}{3 \cdot 5} \tag{4}$$

The choice of prescalers results in much smaller frequency step than those of the individual PLLs, i.e., $f_{in}/3$ and $f_{in}/5$.

Property 2: The output frequency range is $2f_{in}$. More accurately, by defining $\overline{f_{out}} = f_{out}|_{n_1=n_2=0}$, we have

$$f_{out} = \overline{f_{out}} - f_{in} \ \ldots \ \overline{f_{out}} + f_{in} \tag{5}$$

Property 3: If the mixer provided the frequency difference, i.e. if $f_{out} = f_1 - f_2$, properties 1 and 2 would still hold because the ranges of n_1 and n_2 are symmetric with respect to 0.

Table I indicates that f_{out} can be expressed in the form

$$f_{out} = \overline{f_{out}} + \frac{a}{15} f_{in}$$

where a takes the values $-15, -14, -13, \ldots, 14, 15$, and the central frequency is $\overline{f_{out}} = \frac{108}{15} f_{in}$. In contrast, the output frequencies of the individual PLLs are

$$f_1 = \frac{12}{3} f_{in} + \frac{n_1}{3} f_{in} \quad \text{and} \quad f_2 = \frac{16}{5} f_{in} + \frac{n_2}{5} f_{in}.$$

[6]This partially specifies the required frequency range of the VCOs.

$$f_{out} = \left(\frac{n_1}{3} + \frac{n_2}{5} + \frac{12}{3} + \frac{16}{5} \right) f_{in}$$

n_1	n_2	$\frac{f_{out}}{f_{in}}$	=	$\left(\frac{n_1}{3} + \frac{n_2}{5}\right)$	+	$\left(\frac{12}{3} + \frac{16}{5}\right)$
-3	0	93 / 15	=	-15 / 15	+	108 / 15
-1	-3	94 / 15	=	-14 / 15	+	108 / 15
-2	-1	95 / 15	=	-13 / 15	+	108 / 15
-3	1	96 / 15	=	-12 / 15	+	108 / 15
-1	-2	97 / 15	=	-11 / 15	+	108 / 15
-2	0	98 / 15	=	-10 / 15	+	108 / 15
-3	2	99 / 15	=	-9 / 15	+	108 / 15
-1	-1	100 / 15	=	-8 / 15	+	108 / 15
-2	1	101 / 15	=	-7 / 15	+	108 / 15
-3	3	102 / 15	=	-6 / 15	+	108 / 15
-1	0	103 / 15	=	-5 / 15	+	108 / 15
-2	2	104 / 15	=	-4 / 15	+	108 / 15
-3	4	105 / 15	=	-3 / 15	+	108 / 15
-1	1	106 / 15	=	-2 / 15	+	108 / 15
-2	3	107 / 15	=	-1 / 15	+	108 / 15
0	0	108 / 15	=	0 / 15	+	108 / 15
-1	2	109 / 15	=	1 / 15	+	108 / 15
-2	4	110 / 15	=	2 / 15	+	108 / 15
0	1	111 / 15	=	3 / 15	+	108 / 15
-1	3	112 / 15	=	4 / 15	+	108 / 15
1	0	113 / 15	=	5 / 15	+	108 / 15
0	2	114 / 15	=	6 / 15	+	108 / 15
-1	4	115 / 15	=	7 / 15	+	108 / 15
1	1	116 / 15	=	8 / 15	+	108 / 15
0	3	117 / 15	=	9 / 15	+	108 / 15
2	0	118 / 15	=	10 / 15	+	108 / 15
1	2	119 / 15	=	11 / 15	+	108 / 15
0	4	120 / 15	=	12 / 15	+	108 / 15
2	1	121 / 15	=	13 / 15	+	108 / 15
1	3	122 / 15	=	14 / 15	+	108 / 15
3	0	123 / 15	=	15 / 15	+	108 / 15

TABLE I
FREQUENCIES SYNTHESIZED BY THE DFS ARCHITECTURE OF FIGURE 3

Table I shows how to chose the values of n_1 and n_2 resulting in a specific value of a, i.e. how to solve the Diophantine equation [5]

$$\frac{n_1}{3} + \frac{n_2}{5} = \frac{a}{15}$$

The relationship between n_1, n_2 and a is non-trivial and in some cases it is not "unique"; for example both $(n_1, n_2) = (-2, 3)$ and $(n_1, n_2) = (1, -2)$ result in $a = -1$.

Now let's consider the simple architecture in Figure 3 but with feedback dividers 6 and 15 instead of 3 and 5 respectively. Now, n_1 ranges from -6 to 6 and n_2 ranges from -15 to 15. In the line of the previous example one might expect that f_{out} would range from $\overline{f_{out}} - f_{in}$ to $\overline{f_{out}} + f_{in}$ with frequency step $f_{in}/(6 \cdot 15) = f_{in}/90$.

By calculating f_{out} for all 13×31 allowed pairs (n_1, n_2) we see that the output range $\overline{f_{out}} - f_{in} \ldots \overline{f_{out}} + f_{in}$ is indeed achievable. However, the frequency step (resolution) is $f_{in}/30$ and therefore three times larger that the "expected" $f_{in}/(6 \cdot 15)$. Note that[7] $\mathrm{lcm}(6, 15) = 30$.

Question: *What are the special qualities of the pair of numbers "3" and "5" leading to properties 1,2 and 3?*

Answer: *They are (pairwise) relatively prime integers, i.e.*[7] $\gcd(3, 5) = 1$. This is not true for the pair $(6, 15)$.

[7]lcm = least common multiple, gcd = greatest common divider

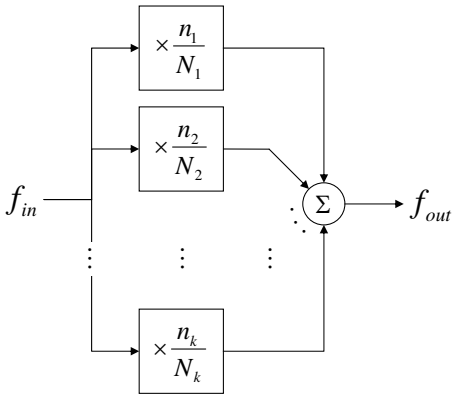

Fig. 4. k-PLLs DFS scheme. Parameters $\bar{n}_1$ to $\bar{n}_k$ are omitted.

The formal answer to the above question is given in Section V. Note also that for both presecalers pairs (N_1, N_2), the frequency step is $f_{in}/\text{lcm}(N_1, N_2)$.

The choice of the constants $\bar{n}_1$ and $\bar{n}_2$ ($\bar{n}_1 = 12$ and $\bar{n}_2 = 16$ in Figure 3) as well as the choice of $+$ or $-$ in the mixer defines the central frequency $\overline{f_{out}}$ and the frequency ratio f_1/f_2 in the mixer. These choices can be used to minimize the spurious signals generated by the mixer. Also, $\bar{n}_1$ and $\bar{n}_2$ along with N_1 and N_2 specify the required frequency ranges of the VCOs.

V. The Mathematical Principle of DFS

DFS achieves arbitrarily small frequency steps while using small prescalers, $N_1, N_2, \ldots, N_k$, at the same time. The example in the previous section is a special case of the general DFS theory for k-PLL architectures, [5], like the one in Figure 4.

We concentrate first on the (normalized) variable part of the output frequency of the k-PLLs DFS scheme in Figure 4.

Theorem 5.1: If $N_1, N_2, \ldots, N_k$ are pairwise relatively prime[8] positive integers, then for every integer a such that $-N_1N_2\cdots N_k \le a \le N_1N_2\cdots N_k$ the Diophantine equation (6) has a solution $(x_1, x_2, \ldots, x_k)$ with $-N_i \le x_i \le N_i$ for all $i = 1, 2, \ldots, k$.

$$\frac{x_1}{N_1} + \frac{x_2}{N_2} + \ldots + \frac{x_k}{N_k} = \frac{a}{N_1N_2\cdots N_k}. \tag{6}$$

The proof of the theorem can be found in [5]. Note that Theorem 5.1 guarantees the existence of solution within the specified bounds, $|x_i| \le N_i$ for all i's, but not its uniqueness.

Interpretation of Theorem 5.1: Rephrasing Theorem 5.1 we can say that given a set $N_1, N_2, \ldots, N_k$ of pairwise relatively prime positive integers, **all** rational numbers from -1 to 1 with uniform step (resolution) $1/(N_1N_2\cdots N_k)$ are generated by the sum $x_1/N_1 + x_2/N_2 + \ldots + x_k/N_k$ when the numerators $x_1, x_2, \ldots, x_k$ vary within the intervals $-N_i \le x_i \le N_i$, $i = 1, 2, \ldots, k$.

[8]i.e. $gcd(N_i, N_j) = 1$ for all $i \ne j$.

VI. Fixed Frequency DFS: An Example

There are applications requiring the generation of a periodic signal of a specific but fixed frequency f_{out} using a reference signal at a given frequency f_{in}. Consider the example:

The input frequency is $f_{in} = 10MHz$ and the desirable output frequency is $f_{out} = 9.285,739,4MHz$ which must be synthesized with accuracy of $0.1Hz$.

To achieve $0.1Hz$ resolution with only one PLL, a prescaler equal to or greater than $f_{in}/0.1Hz = 10^8$ is required. This is definitely impractical for most realistic situations. Although other techniques can be used to achieve this resolution [1]-[2], the Diophantine approach is straight forward.

Let's consider a DFS scheme with two basic PLLs and let the prescalers of the two PLLs be the pair of relatively prime integers N_1 and N_2. Moreover let's assume for simplicity that $N_1 \approxeq N_2$. From Section V we know that the output frequency resolution of the synthesizer is $f_{in}/(N_1N_2)$. Since an accuracy of $0.1Hz$, or better, is required while having input frequency of $10MHz$, it must be that $N_1N_2 \ge 10^8$. This implies that $N_1, N_2 \approxeq sqrt(10^8) = 10,000$, assuming that we want to keep the prescalers minimal.

We can pick for example the pair of relatively prime integers $N_1 = 10,000$ and $N_2 = 10,003$ with $N_1N_2 = 100,030,000$. A DFS scheme based on these prescalers is shown in Figure 5.

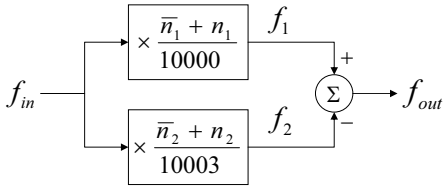

Fig. 5. Two PLLs DFS scheme

For now we ignore $\bar{n}_1$ and $\bar{n}_2$ ($\bar{n}_1 = \bar{n}_2 = 0$) and focus our attention on tuning f_{out} using n_1 and n_2. From section V we know that by choosing appropriate values for n_1 and n_2 (and ignoring $\bar{n}_1$ and $\bar{n}_2$), f_{out} can take any value

$$f_{out} = \frac{n}{100,030,000}\, f_{in} \tag{7}$$

where n ranges from $-100,030,000$ to $100,030,000$.

Choosing $n = 92,885,251$ results in output frequency $f_{out} = 9.285,739,378\ldots MHz$. This is the best possible approximation of the desirable frequency $9.285,739,4\,MHz$ by (7) and the frequency error is within the acceptable bounds.

To derive n_1 and n_2 corresponding to $n = 92,885,251$ we must solve the Diophantine equation[9]

$$\frac{n_1}{10000} + \frac{-n_2}{10003} = \frac{n}{100,030,000}. \tag{8}$$

Since $92,885,251/100,030,000$ is absolutely ≤ 1, Theorem 5.1 guarantees the existence of n_1 and n_2 such that $-N_i \le n_i \le N_i$, $i = 1, 2$ that solve equation (8).

[9]Note that the minus sign is due to frequency mixing in Figure 5 and it does not cause any complication since the ranges of n_1 and n_2 are symmetric with respect to zero.

Using the algorithms in [5] we get $n_1 = 8417$, $n_2 = -869$. It it verified directly that

$$\Big(\frac{8417}{10000} + \frac{-869}{10003}\Big) \cdot 10MHz = 9.285,739,378 \ldots MHz.$$

Now we concentrate on $\bar{n}_1$ and $\bar{n}_2$ and consider the complete expression for f_{out}, that is

$$f_{out} \quad = \quad \Big(\frac{\bar{n}_1}{N_1} - \frac{\bar{n}_2}{N_2}\Big) f_{in} + \Big(\frac{n_1}{N_1} - \frac{n_2}{N_2}\Big) f_{in}.$$

In this example the second summand equals the desirable frequency, therefore, we can set the first summand to zero. For this to happen it must be $\bar{n}_i = c\,N_i$, $i = 1, 2$ where c is an integer (a proof can be found in [5]). Moreover, c must be positive, and sufficient large, so that the frequency multiplication ratio of the PLLs i.e. $(\bar{n}_i + n_i)/N_i = c + n_i/N_i$, $i = 1, 2$, remains always positive.

The value of c can be chosen to minimize the mixing spurs [1], to minimize the phase noise introduced by the VCOs, or to optimize the circuit otherwise. One choice could be $c = 5$ which implies $f_1 \approxeq 58.417,000,0\,MHz$ and $f_2 \approxeq 49.131,260,6\,MHz$.

VII. Variable Frequency DFS: An Example

Suppose we want to design a DFS synthesizer that can generate frequencies from $2MHz$ to $4MHz$ with resolution of about $1Hz$. From the theory in Section V we know that the general architecture of Figure 4, with input frequency f_{in}, can generate all frequencies from $\overline{f_{out}} - f_{in}$ to $\overline{f_{out}} + f_{in}$ with resolution $f_{in}/(N_1 N_2 \cdots N_k)$. Since the frequency range is $2f_{in}$ we can choose

$$f_{in} = 1MHz. \tag{9}$$

Then, the resolution requirement is satisfied if

$$\frac{f_{in}}{1Hz} = N_1 N_2 \cdots N_k \geq 10^6. \tag{10}$$

Suppose we add the requirement that the phase-comparator frequencies in all PLLs are about $10kHz$. This means that

$$\frac{f_{in}}{N_i} \approxeq 10kHz\,, \quad i = 1, 2, \ldots, k. \tag{11}$$

Relations (9) and (11) imply that $N_i \approxeq 100$, $i = 1, 2, \ldots, k$. Therefore, the minimum number of PLLs that satisfies (10) is $k = 3$. Three convenient pairwise relatively prime numbers are $N_1 = 100$, $N_2 = 101$ and $N_3 = 103$.

The next step is to decide what the central frequencies of the three PLLs should be and how they will be mixed i.e. added or subtracted. Since the purpose of this paper is solely to present the mathematical principles of DFS, many technical issues[10] involved in these decisions are not discussed here.

A simple choice is $\overline{f_1} = 55MHz$, $\overline{f_2} = 40MHz$, and $\overline{f_3} = 18MHz$ (no effort has been made to optimize this choice) and the output frequency is chosen to be $f_{out} = -(f_1 - f_2) + f_3$ resulting in $\overline{f_{out}} = 3MHz$. Since $\overline{f_i} = (\bar{n}_i/N_i) f_{in}$, $i = 1, 2, 3$, we have $\bar{n}_1 = 5500$, $\bar{n}_2 = 4040$ and $\bar{n}_3 = 1854$. The DFS architecture is shown in Figure 6.

[10] like the pullability of the PLLs, the spurs generated by the mixing, the possible filtering of the PLLs' signals before mixing, the minimization of the output phase noise etc.

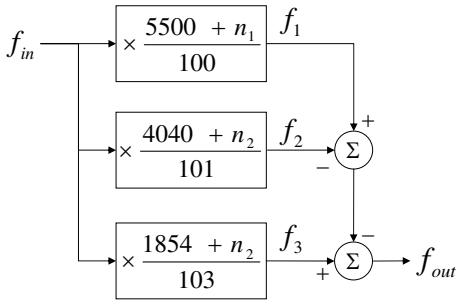

Fig. 6. 3-PLLs Variable Frequency DFS scheme

All frequencies are in MHz

	Min	Central	Max	Frequency step (resolution)
f_{in}	-	1	-	-
f_1	54	55	56	1 / 100
f_2	39	40	41	1 / 101
f_3	17	18	19	1 / 103
f_{out}	2	3	4	1 / 1,040,300

TABLE II
Frequency Ranges and Frequency Steps (Resolutions) of the signals in the DFS Scheme of Figure 6.

The frequency ranges of the PLLs and of the output signal, along with their resolutions, are shown in Table II. The output frequency can take all values

$$f_{out} = \Big(3 + \frac{n}{1,040,300}\Big)\, MHz,$$

where n ranges from $-1,040,300$ to $1,040,300$.

Given the desirable value of n, parameters n_1, n_2 and n_3 can be derived using the theory and algorithms in [5].

VIII. Conclusions

The Diophantine Frequency Synthesis (DFS) has been presented. It is based on number theory and Diophantine equations, uses two or more basic PLLs and allows for independent choices of the output frequency step (resolution) and the phase-comparator frequencies of the PLLs. The Diophantine Frequency Synthesis (DFS) leads to very small frequency steps, fast frequency hopping architectures with potentially very low output spurs, especially in the vicinity of the carrier.

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