

A Quadrature Sinusoidal Oscillator with Phase-Preserving Linear Frequency Control and Independent Static Amplitude Control

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Abstract—A $G_m - C$ architecture for a quadrature, sinusoidal oscillator with instantaneous, phase-preserving, linear frequency control and independent, static amplitude control is presented. The architecture is analyzed and closed-form expressions are given for both frequency and amplitude. An implementation of the architecture using general purpose discrete bipolar transistors has been tested. Simulation results and measurements are demonstrated and compared to theory. The wide frequency range of tunability and the low total harmonic distortion observed, as well as the inherent phase preservation make the architecture appropriate for use in analog communication schemes.

I. INTRODUCTION

Modulation schemes in various communications protocols demand oscillators featuring a wide range of frequency tuning, fast frequency control and low THD (Total Harmonic Distortion). Literature in this field is vast and several designs focusing on some or all of the above properties have been proposed.

Frequency control can be achieved by varying the bias voltage at a varactor in an LC-oscillator. However, LC-VCOs (Voltage Controlled Oscillators) usually do not offer tuning ranges greater than 1 octave and, therefore, the trend has shifted to current-mode implementations. Topologies based on CCCIs (Current Controlled Current Conveyors) ([1] - [4]), OTA-C blocks ([5] - [7]), current-mirror low-pass filters ([8], [9]) and translinear circuits ([10] - [12]) are the ones most commonly encountered. The oscillation frequency is usually linearly controlled by a bias current.

Although frequency tunability is an attribute existing in most current-mode oscillator designs, amplitude control is usually not present and the amplitude of oscillation is limited by the components' non-linearities. This leads to high harmonic distortion. Amplitude control is needed so that the devices operate in their linear region and the harmonic distortion of the output signal is kept low.

A few approaches have been presented for amplitude control that prohibit saturation of signals. The most commonly used method is to subtract the amplitude of oscillation, calculated by a peak detector, from a reference signal, integrate the difference and provide this signal as control to a negative resistance as shown in Fig. 1 (e.g. [7], [13], [14]). However, dynamic feedback for the amplitude control can result in instabilities ([15], [16]). Instabilities are interpreted as fluctuations of the amplitude of oscillation; the magnitude of these fluctuations is dependent on the initial conditions of the feedback system. A remedy to this problem has been proposed in [15] where the feedback system controls both the quality factor, Q , and the amplitude of oscillation. Nonetheless, the range of frequency tunability remains small.

The proposed architecture in this work is based on a translinear approach and handles amplitude control using a static (non-dynamic) feedback, in this way avoiding any steady-state amplitude fluctuations. Static feedback has been also proposed in [17], where, a similar architecture based on operational amplifiers and multipliers had been presented. The feedback is such that the amplitude and frequency

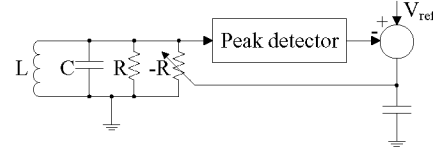


Fig. 1. Amplitude control through comparison of oscillation's amplitude with a reference value

controls are completely decoupled and non-interfering. Moreover, the frequency control is instantaneous, wide range and phase-preserving, making the architecture candidate for use in frequency modulation schemes such as continuous-phase FSK (Frequency Shift Keying). Due to amplitude control, THD is also kept at low values. Extensive simulation results and measurements were conducted and found to be in good agreement with theory, demonstrating the validity of the architecture.

II. THEORETICAL ANALYSIS

An ideal (i.e. lossless) second order $G_m - C$ quadrature oscillator (Fig. 2) can be represented in the state space domain as

$$\begin{aligned}\dot{V}_1(t) &= -\frac{G_m(t)}{C} V_2(t) \\ \dot{V}_2(t) &= \frac{G_m(t)}{C} V_1(t)\end{aligned}\quad (1)$$

where the state variables of the system, $V_1(t)$ and $V_2(t)$, are the voltages on the capacitors. Consider the transformation of the state variables into polar coordinates

$$\begin{aligned}V_1(t) &= \|\mathbf{V}(t)\| \cos(\theta(t)) \\ V_2(t) &= \|\mathbf{V}(t)\| \sin(\theta(t))\end{aligned}\quad (2)$$

where $\|\mathbf{V}(t)\| = \sqrt{V_1(t)^2 + V_2(t)^2}$ is the norm and $\theta(t) = \angle(V_1(t), V_2(t))$ is the phase of vector $\mathbf{V}(t) = [V_1(t) \ V_2(t)]^T$. The solution of (1) can then be written as

$$\|\mathbf{V}(t)\| = A_0 \quad \text{and} \quad \omega(t) = \dot{\theta}(t) = \frac{G_m(t)}{C} \quad (3)$$

where A_0 is a constant and depends on the initial conditions $V_1(0)$ and $V_2(0)$, and $\omega(t)$ is the angular frequency of vector $\mathbf{V}(t)$, i.e. the frequency of oscillation.

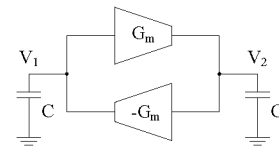


Fig. 2. A simple second order $G_m - C$ oscillator

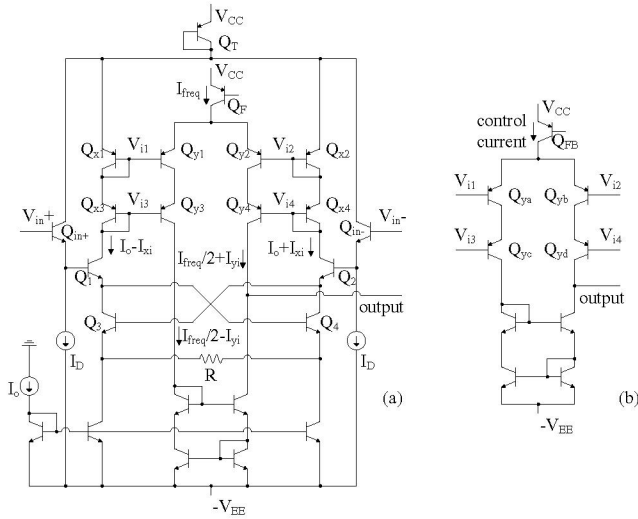


Fig. 4. Circuit implementation of (a) G_{mFREQ} and (b) G_{mFB1} and G_{mFB2} transconductors

and therefore adjustable through I_{freq} . A cascode implementation of the output stage was chosen so as to provide high output impedance.

In order to reduce circuit complexity and because the input stage of all transconductors is connected to either V_1 or V_2 , only the output stage of transconductors G_{mFB1} and G_{mFB2} is implemented (Fig. 4(b)). Nodes $V_{i1} - V_{i4}$ are attached to the corresponding nodes on transconductors G_{mFREQ} . The control (tail) currents (Fig. 4(b)) of transconductors G_{mFB1} and G_{mFB2} are I_{square} and $2I_{ref}$ respectively. Therefore, their gains will be

$$G_{mFB1} = \frac{I_{square}}{I_o R} \quad \text{and} \quad G_{mFB2} = \frac{2I_{ref}}{I_o R} \quad (15)$$

The “Sum of Squares” operation is implemented by the translinear circuit of Fig. 5. Again, inputs V_{11}, V_{12}, V_{21} and V_{22} are tied to nodes V_{i1} and V_{i2} of the two G_{mFREQ} transconductors. Since the biasing current of the input transistors $Q_{F11}, Q_{F12}, Q_{F21}$ and Q_{F22} is I_B , the differential currents $\pm I_{fi}$, $i = 1, 2$ will be given by $\pm I_{fi} = \pm \frac{I_B}{I_o} I_{xi}$, $i = 1, 2$. Using the translinear principle around the loops formed by transistors $Q_{1A} - Q_{1D}$ and $Q_{2A} - Q_{2D}$, we get that

$$I_{square} = I_{s1} + I_{s2} = I_B - \frac{I_{f1}^2 + I_{f2}^2}{2I_B} = I_B \left(1 - \frac{\|\mathbf{V}\|^2}{2I_o^2 R^2} \right) \quad (16)$$

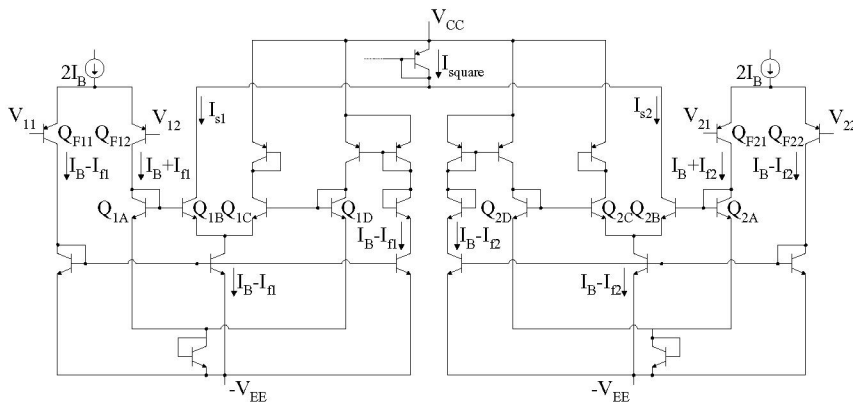


Fig. 5. Circuit design of the “Sum of Squares” block

Closed-form expressions can be derived for the calculation of the frequency as well as the amplitude of oscillation. According to (11), the frequency of oscillation will be

$$f = \frac{G_{mFREQ}}{2\pi C} = \frac{I_{freq}}{2\pi I_o R C} \quad (17)$$

Frequency is linearly and instantaneously controlled by current I_{freq} .

From Fig. 3, it can be readily deduced that the current fed back to the capacitors from transconductors G_{mFB1} and G_{mFB2} is

$$I_{FBVi} = (G_{mFB1} - G_{mFB2}) V_i, \quad i = 1, 2 \quad (18)$$

Combining equations (15), (16) and (18), the feedback current to capacitors C will take the form

$$I_{FBVi} = \frac{I_B}{I_o R} \left(1 - \frac{2I_{ref}}{I_B} - \frac{\|\mathbf{V}\|^2}{2I_o^2 R^2} \right) V_i, \quad i = 1, 2 \quad (19)$$

When the desired amplitude of oscillation A_{ref} is reached, $\|\mathbf{V}\| = A_{ref}$ and $I_{FBVi} = 0$. Substituting in (19), we are able to find a closed-form expression for the amplitude of oscillation at steady-state

$$A_{ref} = \sqrt{2} I_o R \sqrt{1 - \frac{2I_{ref}}{I_B}} \quad (20)$$

Two limitations are imposed on the values that I_{ref} can have. First, from (20), I_{ref} has to be less than half of I_B . Second, I_{xi} cannot be larger than I_o , which limits the maximum amplitude to $\max\{A_{ref}\} = I_o R$. This implies that I_{ref} has to be larger than $0.25I_B$. Combining the two constraints we get that

$$0.25I_B \leq I_{ref} \leq 0.5I_B \quad (21)$$

It should be noted that practical limitations due to the physics and dynamics of bipolar transistors must be also considered for both the amplitude and frequency of oscillation. At high frequencies, parasitics introduce a phase shift between input and output of the transconductors, destroying the quadrature relation between V_1 and V_2 and therefore prohibiting oscillation of the system. Also, the amplitude is limited to values of at most 400mV due to the use of *Caprio* quads at the transconductors [18].

IV. MEASUREMENTS AND SIMULATION RESULTS

The architecture shown in Fig. 3 and described in Section III was simulated, implemented and measured using the general purpose npn and pnp discrete bipolar transistors 2N3390 and 2N3702, 8nF capacitors and 1kΩ resistors. The power supply was set to $V_{CC}=3V$ and $V_{EE}=-3V$. The FREQ transconductors’ (Fig. 4(a)) biasing current

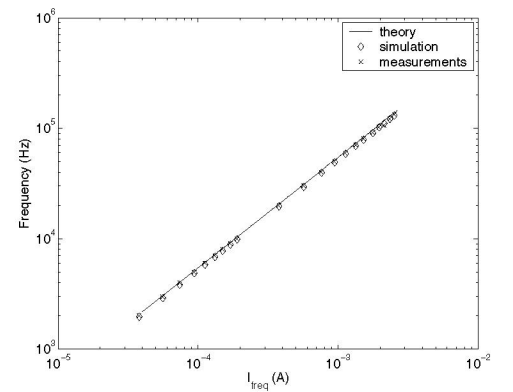


Fig. 6. Linear dependence of the oscillation frequency by I_{freq}

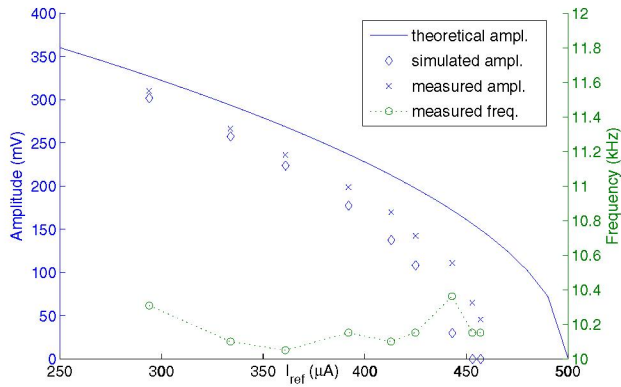


Fig. 7. Relation between the amplitude of oscillation and I_{ref}

I_o was adjusted to $360\mu A$, current I_B of the SoS block (Fig. 5) to $1mA$ and current I_D biasing transistors Q_{in+} and Q_{in-} of the FREQ transconductors (Fig. 4(a)) was set to $10\mu A$.

First, the relation between current I_{freq} (Fig. 4(a)) and the frequency of oscillation as well as the range of operating frequencies were tested. In Fig. 6, simulation and measurements are compared to theoretical results and are shown to be in very good agreement. Although the frequency of oscillation can be linearly controlled by I_{freq} for almost 2 decades (2kHz-130kHz), measurements showed that the desired independence between the amplitude and frequency controls was observed from 7kHz to 130kHz.

Next, the validity of equation (20) that relates current I_{ref} to the amplitude of oscillation was examined. Figure 7 shows results for the case where I_{freq} was set to $180\mu A$ corresponding to a frequency around 10kHz and I_{ref} was swept from $250\mu A$ ($0.25I_B$) to $500\mu A$ ($0.5I_B$). Frequency remained constant while the amplitude of oscillation varied from 0 to 300mV. Simulation results and measurements almost match and follow the same trend as the results predicted from theory. Simulation results and measurements of THD showed also that its value remained well below 2.5%.

The instantaneous frequency control property of the circuit is displayed in Fig. 8. Current I_{freq} is controlled externally from a pulse and instantaneous changes on its value are immediately reflected as instantaneous changes in frequency. Moreover, the instantaneous phase is preserved during frequency jumps.

Finally, simulations of the topology were performed using high f_T RF bipolar transistors, the npn BFG540 and the pnp BFT92. Simulation results showed that oscillations at 6.5MHz and with very low THD can be achieved.

V. CONCLUSIONS

A $G_m - C$ architecture for a quadrature sinusoidal oscillator has been theoretically analyzed, implemented and tested. The architecture features linear and instantaneous frequency control over a wide range, phase preservation during frequency changes, static amplitude control independent of the frequency control and low harmonic distortion. Measurements and simulation results are found to be in good agreement with theory.

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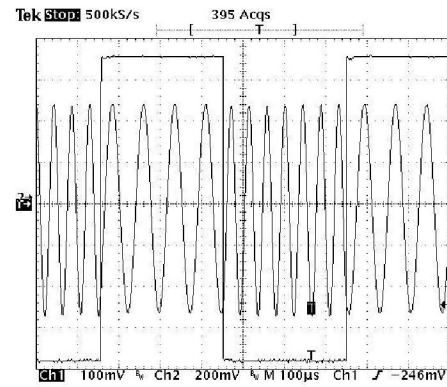


Fig. 8. Oscilloscope snapshot showing the instantaneous control of frequency - the amplitude is independent of the frequency control

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