Analogue Realization of a Fully Tunable Fractional-Order PID Controller for a DC Motor

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Abstract—This paper explores a new integrated-circuit architecture of an analog, active, tunable and selectively fractional or integer -order PID controller using operational amplifiers. Controller’s major parameters are tuned via appropriate DC currents to the desired values. The proposed architecture is validated in a case study of a DC motor control and it can be used as a building block in industrial and commercial control systems. Circuit and physical design (layout) have been done in TSMC 90nm CMOS process. Extensive circuit and post-layout simulation are carried out using the Cadence IC design.

Index Terms—Fractional calculus, fractional-order element, fractional-order controller, amplifiers.

I. INTRODUCTION

Fractional-order calculus is a branch of mathematical analysis. It is a generalization of the classical integer-order calculus and has applications in different fields. Researchers started exploring the concepts of fractional calculus for control systems engineering, due to the fact that it offers more degrees of freedom, in comparison with integer-order one. In addition, they achieve more accurate and sophisticated description of real-world systems [1]–[5]. The transfer function of a fractional-order PID controller in frequency domain is given by:

$$G_{PID}(s) = K_p + K_i s^{-\lambda} + K_ds^\mu$$

(1)

The orders of integration and differentiation are defined by positive real numbers $\lambda, \mu > 0$, rather than just positive integers in a classical sense.

In this paper, we explore a different approach of a controller, which we call fully tunable fractional-order PID controller. In specific circumstances our controller can be configured also as a classical PID controller, or a certain variation of a PID controller with a combination of integer and fractional-order elements. With such versatility, the order of the branches are considered arbitrary (integer or fractional). The basic concept is that we can implement our system by an analog realization of the fractional-order PID controller using operational amplifiers (opamps) and active elements.

The implementation of both integrators and differentiators terms $K_i s^{-\lambda}$ and $K_ds^\mu$ can be realized using FOEs (fractional-order elements) or CPEs (constant phase elements) in the form of fractional-order capacitors [6]–[10], having an impedance of:

$$Z_q(s) = (1/C_q)s^{-q}$$

(2)

where $0 < q < 1$ is the order and $C_q > 0$ is a pseudo-capacitance measured in F/s$^{1-q}$.

This paper is organized as follows: the proposed architecture is presented in Section II, while in Section III an application design example of the PID controller is discussed. The behavior of the proposed controller is evaluated in Section IV, in TSMC 90nm CMOS process. Section VI concludes the paper.

II. PROPOSED HIGH-LEVEL ARCHITECTURE

The proposed fully tunable fractional-order PID controller circuit is depicted in Fig. 1. The high-level architecture has two operational amplifiers, two resistors $R_x$ and $R_y$ and three arbitrary-order elements $C_{\mu}, C_{\nu}$ and $C_{\lambda}$ with orders $\mu, \nu, \lambda$, where $0 \leq \mu, \nu, \lambda \leq 1$.

![Fig. 1. Proposed Fractional-Order PID controller using op-amps as active elements.](image)

Performing a circuit analysis, the obtained transfer function is given by the following equation:

$$G_{GPID}(s) = \left(1 + \frac{R_x}{R_e}\right)^n \left(1 + \frac{C_{\mu}}{C_\lambda}s^{n-\lambda} + \frac{C_{\nu}}{C_\lambda}s^{n-}\right)$$

(3)

or

$$G_{GPID}(s) = \left(1 + \frac{R_x}{R_e}\right)^n \left(1 + \frac{C_{\mu}}{C_\lambda}s^{n-\lambda} + \frac{C_{\nu}}{C_\lambda}\left(1 + \frac{R_y}{R_e}\right)s^{n-}\right)$$

(4)

The corresponding op-amp schematic is depicted in Fig. 2 [10].

III. APPLICATION DESIGN EXAMPLE

In order to evaluate the performance of the proposed fractional-order PID controller, a DC motor system will be considered as plant. Its behavior can be modeled by the

$$U_{in} \rightarrow R_x \rightarrow C_{\lambda} \rightarrow \left(1 + \frac{R_x}{R_e}\right)^n \left(1 + \frac{C_{\mu}}{C_\lambda}s^{n-\lambda} + \frac{C_{\nu}}{C_\lambda}\left(1 + \frac{R_y}{R_e}\right)s^{n-}\right) \rightarrow U_{out}$$

where $0 < q < 1$ is the order and $C_q > 0$ is a pseudo-capacitance measured in F/s$^{1-q}$.
corresponding transfer function:

\[ G_p(s) = \frac{0.08}{s(0.05s + 1)} \]  

(5)

According to [4], the frequency span is from 100kHz to 10Hz and the appropriate fractional-order PID controller expression is given by:

\[ G_c(s) = 10 + \frac{12.5}{s^{0.3}} + 0.625s^{0.7} \]  

(6)

A. Controller

In order to implement the controller for the DC motor, we compare the transfer function (4) with (6). First of all, by setting \( \nu = 1 \) it is derived that \( \lambda = 0.3 \) and \( \mu = 0 \). This means that we have to use a capacitor \( C_\nu \), a fractional-order capacitor \( C_\lambda \) and a resistor \( R_\mu \) (zero pseudo-capacitor). In addition, the modified circuit is depicted in Fig. 3 and the realized transfer function is given by:

\[ G_{PID}(s) = 1 + \frac{R_s}{C_\nu R_m} + \frac{1}{C_\nu R_m(1 + \frac{R_s}{C_\nu R_m})} + \frac{C_\nu}{C_\lambda(1 + \frac{R_s}{C_\nu R_m})} \]  

(7)

B. Implementation of Fractional-Order Capacitor

Since fractional-order capacitors are not yet available for massive production, their behavior is approximated by active and passive elements. In this subsection, we present an architecture for the implementation of fractional-order capacitor. Owing to the fact that the frequency span is from 100kHz to 10Hz the employment of the 5th-order Continued Fraction Expansion (CFE) approximation is a satisfactory solution in order to achieve the appropriate results [7], [8].

The expression of the 5th-order CFE approximation is described by

\[ (\tau s)^{\alpha} \approx \frac{a_5s^{\alpha} + a_4s^{\alpha} + a_3s^{\alpha} + a_2s^{\alpha} + a_1s + a_0}{b_5s^{\alpha} + b_4s^{\alpha} + b_3s^{\alpha} + b_2s^{\alpha} + b_1s + b_0} \]  

(8)

where:

\[ \alpha = 5 \quad = -\alpha - 15\alpha - 85\alpha - 225\alpha - 274\alpha - 120, \]
\[ \alpha = 4 \quad = 5\alpha + 45\alpha + 5\alpha - 1005\alpha - 3250\alpha - 3000, \]
\[ \alpha = 3 \quad = -10\alpha - 30\alpha + 410\alpha + 12300\alpha - 4000\alpha - 1200, \]
\[ \alpha = 2 \quad = 10\alpha - 30\alpha - 410\alpha + 12300\alpha + 4000\alpha - 12000, \]
\[ \alpha = 1 \quad = -5\alpha + 45\alpha + 5\alpha - 1005\alpha + 3250\alpha - 3000, \]
\[ \alpha = 0 \quad = 5\alpha^5 + 15\alpha^4 + 85\alpha^3 - 225\alpha^2 + 274\alpha - 120, \]

and \( \alpha \) is the order of fractional-order differentiator (all-pass filter) [7], [8].

In order to obtain the tunability of both impedance and order of the element, operational transconductance amplifiers (OTAs) are utilized to describe fractional-order capacitors. Fractional-order capacitor is designed using an all-pass filter, connected with a multiple-output OTA, which acts as a Voltage-to-Current (V/I) converter [7], [8]. The all-pass filter has a transfer function \( H(s) \). The complete architecture is shown in Fig. 4. The impedance of fractional-order capacitor is given by:

\[ Y_{cap}(s) = \frac{1}{g_m H(s)} \]  

(9)

where \( g_m \) is the transconductance of the V/I converter.

The transfer function \( H(s) \) is that of a 5th order all-pass filter, given by:

\[ H(s) = \frac{A(s)}{B(s)} \]  

(10)

where \( A(s) \) is expressed by:

\[ A(s) = G_5s^5 + G_4s^4 + G_3s^3 + G_2s^2 + G_1s + G_o \]  

(11)

and \( B(s) \) is described by:

\[ B(s) = s^5 + \frac{s^4}{\tau_1} + \frac{s^3}{\tau_1\tau_2} + \frac{s^2}{\tau_1\tau_2\tau_3} + \frac{s}{\tau_1\tau_2\tau_3\tau_4} + \frac{1}{\tau_1\tau_2\tau_3\tau_4\tau_5} \]  

(12)

The schematic of the corresponding OTA, which is used for the implementation of \( H(s) \) is depicted in Fig. 5 [8], [10].

**TABLE I**

PASSIVE ELEMENTS VALUES OF THE MODIFIED CONTROLLER IN Fig.3

<table>
<thead>
<tr>
<th>Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_s )</td>
<td>1M( \Omega )</td>
</tr>
<tr>
<td>( R_m )</td>
<td>9M( \Omega )</td>
</tr>
<tr>
<td>( C_\nu )</td>
<td>62.5n( \text{F} )</td>
</tr>
<tr>
<td>( C_\lambda )</td>
<td>1\mu( \text{F} )/sec(^{0.7})</td>
</tr>
<tr>
<td>( R_\mu )</td>
<td>800k( \Omega )</td>
</tr>
</tbody>
</table>

**Fig. 2.** Employed op-amp.

**Fig. 3.** Modified Fractional-order PID controller.

In order to calculate the controller’s elements’ values, we compare the transfer functions (4) and (7). All the passive elements’ values of the controller are summarized in Table I.
to the fact that all transistors are biased in the sub-threshold region, the transconductance is given by:

\[ g_m = \frac{5I_{\text{bias}}}{9nV_T} \]  

(13)

where \( 1 < n < 2 \), and \( V_T = 26 \text{ mV} \).

The main advantage of the proposed architecture is that we can implement a fully tunable fractional-order PID controller because we can achieve different expressions of the controller by the same core, just by adjusting the DC bias currents.

Both all resistors and fractional-order capacitor are tuned by programmable OTAs’ currents. In (10) both scaling factor \( G_j \), \( (j = 0, 1, 2, 3, 4, 5) \), which given by:

\[ G_j = \frac{g_{mj}}{g_m} \]  

(16)

and time constants \( \tau_i \), \( (i = 1, 2, 3, 4, 5) \), expressed by:

\[ \tau_i = \frac{C_i}{g_m} \]  

(17)

depend on the transconductance of the corresponding OTA. All the parameters have electronic tuning capability resulting from (13).

### IV. Simulation Results

The proposed architecture has been designed in TSMC 90 nm CMOS process, using the Cadence IC design suite. The power supply rails are set to \( V_{DD} = -V_{SS} = 0.75 \text{ V} \), and all transistors operate in the sub-threshold region. The dimensions
of the MOS transistors of the opamp and OTA are summarized in Table II.

<table>
<thead>
<tr>
<th>OP-AMP</th>
<th>W/L (µm/µm)</th>
<th>OTA</th>
<th>W/L (µm/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{n1}, M_{n2}$</td>
<td>4/0.4</td>
<td>$M_{p2}, M_{n3}$</td>
<td>2/1</td>
</tr>
<tr>
<td>$M_{n3}$</td>
<td>250/2</td>
<td>$M_{n8}$</td>
<td>1/2</td>
</tr>
<tr>
<td>$M_{n4}$</td>
<td>50/2</td>
<td>$M_{n5}$</td>
<td>0.5/4</td>
</tr>
<tr>
<td>$M_{n5}, M_{n6}$</td>
<td>25/2</td>
<td>$M_{n11}$</td>
<td>1/2</td>
</tr>
<tr>
<td>$M_{p1}$</td>
<td>37.5/1</td>
<td>$M_{p3}, M_{p4}$</td>
<td>10/5</td>
</tr>
<tr>
<td>$M_{p2}, M_{p3}$</td>
<td>225/1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$M_{p4}, M_{p7}$</td>
<td>125/1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$M_{p5}$</td>
<td>25/0.1</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$M_{p6}$</td>
<td>125/0.1</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

The value of the transconductance is $g_m = 0.539 \mu S$ and $g_{m,vi} = 0.604 \mu S$; as a result, the capacitors’ values are calculated by $C_i = \tau_i g_m$, $(i = 1, 2, 3, 4, 5)$, and summarized in Table III. The resistor’s value in Fig. 2 is $R_f = 221 \Omega$. The values of the resulting scaling factors are summarized in Table IV.

<table>
<thead>
<tr>
<th>Element</th>
<th>Value</th>
<th>Element</th>
<th>Value</th>
<th>Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$</td>
<td>1.80 nF</td>
<td>$C_2$</td>
<td>6.0 nF</td>
<td>$C_3$</td>
<td>30.81 nF</td>
</tr>
<tr>
<td>$C_4$</td>
<td>300.03 nF</td>
<td>$C_5$</td>
<td>3 µF</td>
<td>$C_7$</td>
<td>2 pF</td>
</tr>
</tbody>
</table>

The layout design of the controller is demonstrated in Fig. 7, where the area is 278X154. The layout includes all elements except capacitors $C_i$, $(i = 1, 2, 3, 4, 5)$. The open-loop gain and phase responses of the controller-plant are demonstrated in Fig. 8, along with the theoretically predicted ones, confirming the correct operation of the controller’s design. The sensitivity characteristics show that the proposed architecture has reasonable sensitivity characteristics.

Fig. 7. Layout design of the implemented fractional-order PID controller.

Fig. 8. Frequency responses of the open-loop controller-plant system.

V. CONCLUSION

The design of a tunable fractional-order PID controller and its application was presented in this paper. The proposed integrated circuit can be used as a basic circuitry block for the design of more complex and sophisticated control systems. The electronic tuning of the proposed scheme’s parameters has been verified through post-layout simulation results. Finally, the derived results of the Monte Carlo analysis show that the proposed architecture has reasonable sensitivity characteristics.

REFERENCES