Fractional-Order Instrumentation Amplifier Transfer Function for Control Applications

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Abstract—This paper explores a new architecture for a fractional-order instrumentation amplifier for control applications. The proposed architecture provides electronic tuning capability and is reconfigurable. It can be configured as either a classic integer-order or a fractional-order instrumentation amplifier, with appropriate tuning of the parameters that define the characteristics of the components involved. The proposed design can be used as a fundamental building block in the implementation of more complex control systems.

Index Terms—Fractional calculus, fractional-order element, fractional-order controller, amplifiers.

I. INTRODUCTION

The proportional-integral-derivative (PID) controller is one of the most studied and commonly used controllers in industrial control applications. In general, a PID controller has three branches: 1) the proportional branch; 2) the integral branch; and 3) the derivative branch. Resources and knowledge about PID controller are by no means scarce, with research papers, patents, whitepapers, scholarly outputs, and products available globally [1]–[6].

Over the past two decades, researchers have been exploring the concepts of fractional calculus for control systems engineering. As a result, many research works have been published on Fractional-Order PID (FOPID) controllers, also known as $PI^\lambda D^\mu$ controllers [1]–[6]. A FOPID controller is a PID controller whose integral and derivative branches are not necessarily of integer-order, but of order defined by positive real numbers $\lambda, \mu > 0$. Its transfer function is

$$G_{FOPID}(s) = K_p + K_I s^{-\lambda} + K_D s^\mu$$

where $K_p$, $K_I$, and $K_D$ are the proportional, integral and derivative gains, respectively.

In this paper, we introduce an architecture of a fractional-order PD controller, which is implemented using a fully tunable arbitrary-order instrumentation amplifier [7], [8]. The instrumentation amplifier typically has some important features like high input impedance, high common mode rejection ratio (CMRR), high gain and potentially low offset. Due to all of its aforementioned qualities, it has been proved to be very useful in implementing analog control systems for industry applications.

The rest of the paper is organized as follows. The proposed architecture with an application design example are presented in Section II, while Sections III and IV outline the implementation of the involved elements. The behavior of the proposed controller is evaluated in Section V, in TSMC 90 nm CMOS process. Finally, Section VI concludes the paper.

II. PROPOSED FRACTIONAL-ORDER INSTRUMENTATION AMPLIFIER HIGH-LEVEL ARCHITECTURE

Fractional-order controller schemes have been realized using different types of active elements such as operational amplifiers (op-amps) [4], operational transconductance amplifiers (OTAs) [5] and Current-Conveyors (CCII) [6]. To implement a fully tunable $PD^\mu$ controller with transfer function

$$G_{PD}(s) = K_p (1 + K_D s^\mu)$$

we combine elements from all these architectures.

We start by modifying the classic architecture of an instrumentation amplifier [7], [8]; resistor $R_g$ is replaced by a tunable fractional-order capacitor, $Y_g = 1/(C_g s^\alpha)$, where $C_g$ is the pseudo-capacitance expressed in Farad/sec$^1 - \gamma$ and $0 < g < 1$. All other resistors are replaced by floating OTA emulators, $R_x = 1/g_{mx}$, where $g = \alpha, \beta, \gamma$. The topology is depicted in Fig. 1, and the transfer function is given by

$$G_{FIA}(s) = \frac{U_{out}}{U_2 - U_1} = \frac{R_x}{R_2} (1 + 2C_g R_\alpha s^\delta)$$

The corresponding op-amp schematic is depicted in Fig. 2. The performance of the proposed fractional-order instrumentation amplifier is evaluated by a position control system [3]. The behavior of the plant is modeled by the transfer function

$$G_p(s) = \frac{1.52}{s(0.4s + 1)}$$

and the corresponding controller expression is given by

$$G_c(s) = 13.86 \left(1 + 0.368s^{0.844}\right).$$

The frequency range of practical interest for the corresponding system is between 1 Hz and 100 Hz. In order to implement the system, we compare (3) with the corresponding controller's expression in (5). A choice of values for the passive elements is summarized in Table I.
Table I
Passive Elements of the Instrumentation Amplifier of Fig. 1.

<table>
<thead>
<tr>
<th>Element</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_a$</td>
<td>9.2 $\Omega$</td>
</tr>
<tr>
<td>$R_b$</td>
<td>1 $\Omega$</td>
</tr>
<tr>
<td>$R_c$</td>
<td>13.9 $\Omega$</td>
</tr>
<tr>
<td>$C_g$</td>
<td>0.02 $\mu F$</td>
</tr>
</tbody>
</table>

III. Implementation of Fully Tunable Fractional-Order Capacitor Emulator

Since fractional-order elements are not yet commercially available, their behavior is approximated by active ones. There are many different designs for the implementation of fractional-order elements as well as tunable resistor emulators that we incorporate [9]–[14].

To approximate the impedance of the fractional-order capacitor we use a ladder RC-network, as depicted in Fig. 3 and derive the values of its components following [13], [14]. Furthermore, to achieve tunability, the elements in the RC-network are realized using active elements like OTAs and CCII.

Fig. 3. RC-network for approximating the behavior of fractional-order capacitors.

The impedance of the ladder of the RC-network is

$$Y_{tot}(s) = sC_p + \frac{1}{R_p} + \sum_{k=1}^{m} \frac{sC_k}{sR_kC_k + 1}.$$ (6)

The fractional-order capacitor is implemented by cascading integrators and connecting them with a fully differential OTA. The cascaded integrators have transfer functions $H_a(s)$ and $H_b(s)$ respectively. The complete architecture is shown in Fig. 5, and the total transfer function, $H(s)$, is given by $H(s) = H_a(s)H_b(s)$. The impedance of the fractional-order capacitor is

$$Y_{ap}(s) = \frac{1}{g_{mvi}H(s)}$$ (7)

where $g_{mvi}$ is the transconductance of the differential OTA.

The transfer function $H_a(s)$ is that of a 3rd order all-pass filter, given by

$$H_a(s) = \frac{G_3 s^3 + G_2 s^2 + G_1 s + G_0}{s^3 + \frac{1}{\tau_1} s^2 + \frac{1}{\tau_1\tau_2} s + \frac{1}{\tau_1\tau_2\tau_3}}.$$ (8)

while the transfer function $H_b(s)$ is that of a 1st order filter

$$H_b(s) = \frac{R_{r2}C_p s + R_{r1}}{R_{r1}}.$$ (9)

The schematic of the CCII used for the implementation of $H_b(s)$ is depicted in Fig. 4.

It has been shown that a phase accuracy of about 1.5° is sufficient in most fractional-order controller applications.
It turns out that the least order of RC-network achieving this accuracy, within the frequency range of 1 Hz to 100 Hz and following the approximation method in [13], [14], is $m = 3$ (center frequency is $f_o = 10$ Hz). Given the above, the impedance of the derived RC-network, approximating that of the fractional-order capacitor $Y_g = 1/(C_g s^g)$ is

$$Y_{ap}(s) = \frac{1.667 \cdot 10^8 s^3 + 1.256 \cdot 10^{13} s^2 + 8.220 \cdot 10^{12} s + 4.673 \cdot 10^{13}}{s^4 + 1002 \cdot s^3 + 1.042 \cdot 10^5 s^2 + 8.541 \cdot 10^3 s + 5.472 \cdot 10^2}.$$  \hspace{1cm} (10)

In order to implement the fractional capacitor, we compare (10) with (7) and choose the value of the transconductance $g_{m,vi}$ to be 0.1 $\mu$S. The resulting $H(s)$ is given by

$$H(s) = \frac{s^4 + 1002 \cdot s^3 + 1.042 \cdot 10^5 s^2 + 8.541 \cdot 10^3 s + 5.472 \cdot 10^2}{16.67s^3 + 1.042 \cdot 10^5 s^2 + 8.22 \cdot 10^3 s + 4.673 \cdot 10^2}. \hspace{1cm} (11)$$

All the values of the involved parameters are summarized in Section V. To implement a fractional-order capacitor with different pseudo-capitance $C_g$ and order $g$, we calculate the parameters of (11) and adjust the appropriate OTAs’ dc currents.

IV. IMPLEMENTATION OF TUNABLE RESISTOR

The implementation of the tunable resistor is achieved by utilizing a programmable OTA in the configuration of Fig. 6. The schematic of the corresponding OTA is depicted in Fig. 7 [11]. All transistors are biased in the sub-threshold region, and so the impedance of the effective resistance is given by

$$R_x = \frac{1}{g_{mz}} \hspace{1cm} (12)$$

where $x = \alpha, \beta, \gamma, \text{and}$

$$g_{mz} = \frac{5I_{bias,x}}{9nV_T} \hspace{1cm} (13)$$

where $1 < n < 2$, and $V_T = 26$ mV.

The main advantage of the proposed architecture is that we can implement a fully tunable fractional-order instrumentation.
amplifier because we can achieve different expressions of the controller, by the same core, just by adjusting the dc bias currents.

Both all resistors and fractional-order capacitor are tuned by programmable OTAs’ currents. In (8) both scaling factor 

\[ G_j = \frac{g_{mj}}{g_m} \]  

(14)

and time constants \( \tau_i \), (i = 1, 2, 3), which are expressed by

\[ \tau_i = \frac{C_i}{g_m} \]  

(15)

depend on the transconductance of the corresponding OTA. All the parameter have electronic tuning capability resulting from (13).

V. SIMULATION RESULTS

The proposed instrumentation amplifier has been designed in TSMC 90 nm CMOS process, using the Cadence IC design suite. The power supply rails are \( V_{DD} = -V_{SS} = 0.75 \) V, and all transistors operate in the sub-threshold region. The dimensions of the MOS transistors of the op-amp, the OTA and the CClI are summarized in Tables II and III.

| TABLE II |
| MOS TRANSISTORS DIMENSIONS – OP-AMP & OTA. |
| OP-AMP | W/L (\( \mu \)m/\( \mu \)m) |
| \( M_{n1},M_{n2} \) | 20/0.2 |
| \( M_{n3} \) | 25/0.2 |
| \( M_{n4} \) | 5/0.2 |
| \( M_{n5},M_{n6} \) | 2.5/0.2 |
| \( M_{p1},M_{p5} \) | 12.5/0.1 |
| \( M_{p2},M_{p3},M_{p6} \) | 2.5/0.1 |
| \( M_{p4} \) | 1.25/0.1 |
| \( M_{p7} \) | 5/0.1 |

| TABLE III |
| MOS TRANSISTORS DIMENSIONS – CClI. |
| CCII | W/L (\( \mu \)m/\( \mu \)m) |
| \( M_{p1},M_{p2},M_{p4} \) | 1.6/0.4 |
| \( M_{p3},M_{p9} \) | 3.2/0.4 |
| \( M_{p3} \) | 6.4/0.4 |
| \( M_{n1},M_{n9} \) | 0.8/0.4 |
| \( M_{p7} \) | 1.6/0.4 |

In order to calculate the values of scaling factors \( G_j \), \( j = 0, 1, 2, 3 \) and time-constants \( \tau_i \), (i = 1, 2, 3), we compare expression (11) with (8) and (9). The value of the transconductance is \( g_m = g_{m,v1} = 0.1 \mu S \); as a result, the values of capacitors are calculated by \( C_i = \tau_i g_m \), and are summarized in Table IV. The values of the resulting scaling factors are summarized in Table V.

In order to calculate the corresponding currents, we utilize expressions (12) and (13) along with the values of Table I. The resulting current values are summarized in Table VI. The current for the implementation of the corresponding transconductance \( g_{m,v1} = g_m = 0.1 \mu S \) is \( I_{bias} \), and is calculated using the expression \( I_{bias} = \frac{9}{8} n V_T g_m \). The current value for a transconductance of \( g_{mj} = G_j g_m \) can be calculated by \( I_{bias,j} = G_j I_{bias} \), where \( j = 0, 1, 2, 3 \). The values of the parameters in (8) and (9) depend directly on the coefficients of transfer function H(s) in (11). This means that the values, which are summarized in both Table V and Table VI can be modified in another case. The electronic capability of the bias current provides us with the opportunity to achieve different controller’s expression.

The obtained impedance responses along with the theoretically predicted ones are shown in Fig. 8 and Fig. 9, respectively. Both impedance and phase responses for the fractional-order capacitor emulator confirm the correct operation of the proposed architecture in Fig. 5. The Mean Absolute Error (MAE) is less than 3.8\( \mu \)Ω for the impedance and the maximum absolute error is less than 2° for phase.

The open-loop gain and phase responses of the controller-

\[ \text{Fig. 8. Impedance magnitude response of fractional-order capacitor emulator.} \]
TABLE VI
VALUES OF BIAS CURRENTS.

<table>
<thead>
<tr>
<th>Bias Current</th>
<th>Value nA</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_b )</td>
<td>20.00</td>
</tr>
<tr>
<td>( I_{bias} )</td>
<td>5.45</td>
</tr>
<tr>
<td>( I_{bias,\alpha} )</td>
<td>2.14</td>
</tr>
<tr>
<td>( I_{bias,\beta} )</td>
<td>52.42</td>
</tr>
<tr>
<td>( I_{bias,\gamma} )</td>
<td>2.92</td>
</tr>
</tbody>
</table>

plant are demonstrated in Fig. 10 and Fig. 11, respectively, along with the theoretically predicted ones, confirming the correct operation of the controller’s design. The maximum error between simulation and theoretical one is less than 0.12dB for gain and less than 0.55° for phase, respectively.

The time-domain behavior of the closed-loop controller-plant system, stimulated by a 500 mV step response, is depicted in Fig. 12. The results of the proposed architecture are in good agreement with the theoretical ones and confirm the accuracy and the performance of the system.

Fig. 9. Impedance phase response of fractional-order capacitor emulator.

Fig. 10. Frequency responses of the open-loop controller-plant system gain.

Fig. 11. Frequency responses of the open-loop controller-plant system phase.

The sensitivity behavior has been evaluated using the Monte-Carlo analysis tool for \( N = 100 \) runs. The corresponding histograms for gain and phase of the open-loop system are shown in Fig. 13 and Fig. 14, respectively. The mean value of the gain is \( G_{\text{mean}} = -15.2 \) dB, and the standard deviation is \( \sigma_G = 0.6 \) dB. The mean value of the phase is \( P_{\text{mean}} = -106.3^\circ \), and the standard deviation is \( \sigma_P = 2.3^\circ \) at \( f_0 = 10 \) Hz.

VI. CONCLUSION

The design of a tunable fractional-order instrumentation amplifier and its application is presented in this paper. The obtained simulation results confirm its proper operation, both in a closed- and an open-loop controller-plant system. Consistency improvement between theoretical and simulation results can be achieved through the utilization of a higher order RC-network approximation. It could be considered as a basic candidate for achieving high performance analog control systems.

Fig. 12. Time-domain behavior of the closed-loop controller-plant system stimulated by a 500 mV step response.
REFERENCES


