Integrators Using a Single Distributed RC Element

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Abstract: In this work we ask the fundamental question: *Is it possible to achieve single-pole behavior using a single grounded URC?* To answer this question affirmatively, we present two novel integrator topologies. They both use a *single* grounded uniformly distributed RC line instead of pure capacitors. They have important advantages compared to the topologies presented in the literature which require either pairs of exactly commensurate uniformly distributed RC lines or other distributed structures of complex geometry.

Introduction

Much work was done during the 60's and 70's on network synthesis using distributed RC elements. Researchers explored many different approaches to compose important classes of impedances and transfer functions using distributed elements. The developed techniques can be organized into four general classes. I) Exact synthesis of transfer functions rational on the $\Lambda = \tanh(a\sqrt{s})$ plane (Richard's transformation [1]), or the $P = \cosh(a\sqrt{s})$ plane (O'Shea's transformation [2]). II) Exact transfer function synthesis, rational on the s plane using non-uniform or non-grounded or multi-layer distributed structures [3]-[4]. III) Exact transfer function synthesis rational on the s plane using pairs of uniform grounded commensurate (with the same time constant) distributed RCs [5], [7]. IV) Approximate techniques leading to networks with transfer functions approximately rational on the s plane. The list of publications given at the end is only partial, an excellent reference for works on distributed linear networks techniques is [6].

Approaches in the first class are mathematically elegant but lead to a complex and impractical theory compared to network synthesis with lumped elements. Techniques in the second class lead to a large variety of implementations but in general they require types of distributed elements that may be hard or even impossible to manufacture. Approximate solutions in the fourth class provide good results only for low order transfer functions. The third class and particularly the elegant technique proposed in [5] exploits a property of pairs of commensurate grounded URCs to implement arbitrary rational transfer functions. More recently another exact synthesis technique on the s-plane was proposed in [7]. A large variety of basic blocks, integrators and differentiators is introduced there. All of them are composed of pairs of commensurate grounded URCs.

Both of the techniques in [5] and [7] require that the two URCs are exactly commensurate (have the same time constant). Significant errors are introduced when this property is not perfectly satisfied.

To solve this matching problem, two novel integrator topologies that require *only one* grounded URC are introduced in this paper. They are designed according to a new general approach. As it is shown by the two examples here and is discussed in great detail in [10], it is possible to achieve a rational transfer function (or other characteristic) with a single URC, only if it is operated inside a feedback loop. This is in contrast to the work in [7] where integrators are built as cascades of commensurate URCs. The application of feedback in the proposed topologies is shown to be equivalent to the separation of the common - differential modes of operation of the URC.

1. The Grounded Uniformly Distributed RC Line (URC)

In this Section we review some properties of the URC that will be used later for the validation of the two proposed integrators.

A grounded URC is a *symmetric two-port* linear element characterized by its resistance per unit length R_0 in Ω/m, its capacitance per unit length C_0 in F/m and its total length L. It is symbolically represented by the T network of Figure 1.

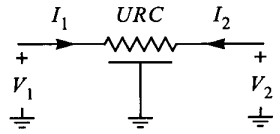

Figure 1: Grounded URC

The total resistance and the total capacitance of the URC are defined as $R = R_0 L$ and $C = C_0 L$ respectively. Finally, the *time constant* τ of the URC is defined as,

$$\tau = R_0 C_0 L^2 = RC \tag{1}$$

and is a measure of the propagation delay from one of its ports to the other. For frequencies much smaller than $1/\tau$ the URC tends to behave like a lumped R,C element. Two URCs with time constants τ_1, τ_2 are called *commensurate* if $\tau_1 = \tau_2$. Pairs of commensurate URCs have been used extensively in earlier studies.

The URC element accepts all two-port descriptions [6]. Here the impedance matrix is preferred,

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_0 & Z_m \\ Z_m & Z_0 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2}$$

The driving impedance Z_0 and the transimpedance Z_m of the URC are given by the expressions:

$$Z_0(s) = \frac{\sqrt{\tau s}\cdot \coth(\sqrt{\tau s})}{Cs}$$
$$Z_m(s) = \frac{\sqrt{\tau s}\cdot \operatorname{csch}(\sqrt{\tau s})}{Cs} \quad (3)$$

Although Z_0 and Z_m are both *irrational* functions of s, they satisfy the important relation:

$$Z_0^2 - Z_m^2 = \frac{R}{Cs} \quad (4)$$

Finally, since the URC is a symmetric two-port, it is equivalent to the T network of Figure 2. The difference $Z_0 - Z_m$ is an *irrational* function of s as well.

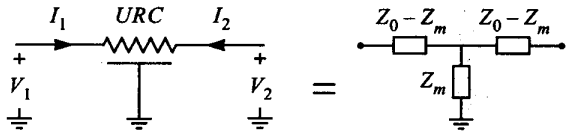

Figure 2: Equivalent T-element

2. GROUNDED-URC INTEGRATOR I

The first integrator topology is shown in Figure 3. The input is formed by the currents I_X and the output is the voltage difference $V_Y = V_1 - V_2$. It has an "internal" *feedback loop* consisting of the two voltage controlled current sources.

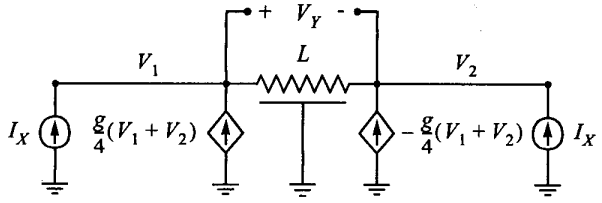

Figure 3: Proposed integrator I

As it will be shown in the rest of this section, the transfer function of the network is given by the expression:

$$\frac{V_Y}{I_X} = \frac{gR}{C}\cdot\frac{1}{s} \quad (5)$$

Since g is a transconductance, the products gR is dimensionless and (5) represents a current-in, voltage-out integrator of transcapacitance gR/C.

We now proceed with a gradual derivation of the above result, in parallel with a discussion of the principles involved; these principles have more general value, but are illustrated here using the specific situation at hand.

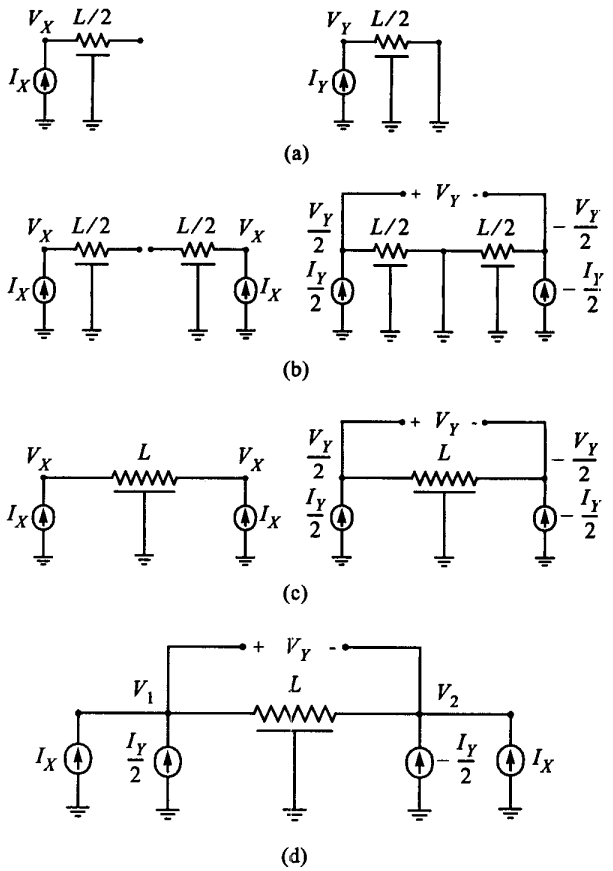

Figure 4: Combination of the *cm* and *dm* operations of the URC

2.1 Obtaining Both Open-Circuit and Short-Circuit URC Port Impedances Simultaneously from a Single URC.

Consider two URCs, each of length $L/2$ and current-driven at port 1. Port 2 is open-circuited in one URC and short-circuited in the other, as shown in Figure 4(a). Consider now the circuit in Figure 4(b), in which each URC of Figure 4(a) has been doubled up. The two URCs on the left are driven symmetrically, whereas the two URCs on the right are driven antisymmetrically as shown. It is clear that the responses V_X and V_Y are the same as the corresponding ones in Figure 4(a). We notice that, in the circuit on the left in Figure 4(b), the two floating nodes in the middle can be connected without changing any voltage or current; no current will flow through this connection due to symmetry. We also notice that, in the circuit on the right, by superposition, the middle connection to ground carries no current and can be broken. In both cases, then, we obtain two URCs of length $L/2$ each, connected end-to-end. This results in the situation shown in Figure 4(c), where each URC has length L. The responses V_X and V_Y in this figure can be obtained by direct use of the equivalent T-element in Figure 2 or equations (2):

$$V_X = (Z_0 + Z_m)I_X \quad (6)$$
$$V_Y = (Z_0 - Z_m)I_Y \quad (7)$$

Consider now the circuit in Figure 4(d). The responses V_1 and V_2 in this circuit can be obtained by superposing the responses of the circuits in Figure 4(c):

$$V_1 = V_X + V_Y/2 \tag{8}$$

$$V_2 = V_X - V_Y/2 \tag{9}$$

Thus, the *cm* (common-mode) value $(V_1 + V_2)/2$ of V_1 and V_2 is V_X, whereas the *dm* (differential-mode) value $V_1 - V_2$ is V_Y. We conclude that *the port impedances of the open-circuited and short-circuited URCs of Figure 4(a) can both be obtained on a single URC of twice the length, as the cm-to-cm and dm-to-dm responses, respectively.*

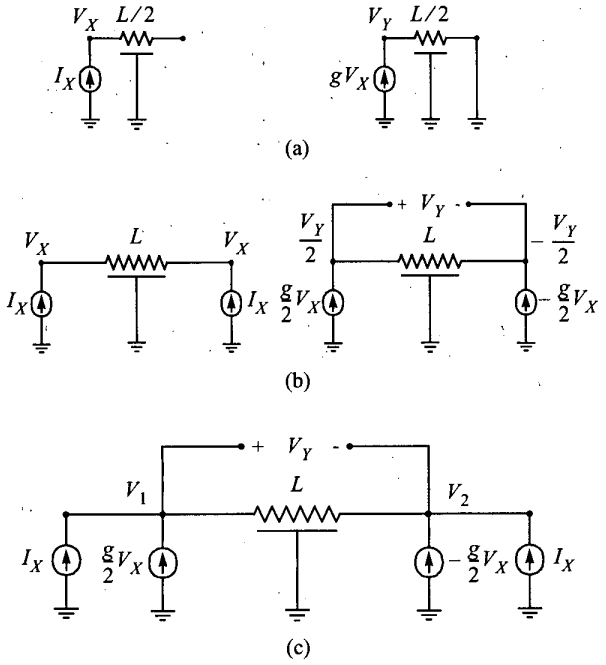

Figure 5: Composition of integrator I

2.2 Emulating Cascade Behavior by Re-Use of a Single Element

Consider now the cascade circuit in Figure 5(a); this circuit has been proposed in ref. [7], where it is shown that the behavior from I_X to V_Y is that of an ideal integrator. This figure is the same as Figure 4(a), with:

$$I_Y = gV_X \tag{10}$$

The circuit corresponding to Figure 4(c) is shown in Figure 5(b). Equation (6) still applies, and so does (7) with I_Y as in (10). The transfer function V_Y/I_X of this cascade can be obtained from these equations as:

$$\frac{V_Y}{I_X} = g(Z_0^2 - Z_m^2) \tag{11}$$

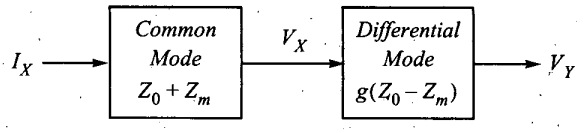

Figure 6: Integrator I as a cascade

As it was done above, the two circuits in Figure 5(b) can be combined into a single one, as shown in Figure 5(c). (Notice that in the current sources $\pm gV_X/2$, V_X is meant to be the voltage so labelled in Figure 5(b); thus, as far as the circuit in Figure 5(c) is concerned, these current sources can be viewed as independent current sources and there is no ambiguity in applying superposition.) Equations (8) and (9) still apply, with V_X and V_Y the voltages in the circuits of Figure 5(b). The *cm* and *dm* values of V_1 and V_2 are:

$$\frac{V_1 + V_2}{2} = V_X \tag{12}$$

$$V_1 - V_2 = V_Y \tag{13}$$

Thus, in the two middle current sources in Figure 5(c), V_X can be replaced by (12), i.e. their current can be produced by voltages in the same circuit, as shown in Figure 3. This is the proposed circuit; this circuit is still characterized by the above equations, and its transfer function is given by (11). Combining expressions (11) and (4) we get:

$$\frac{V_Y}{I_X} = \frac{gR}{Cs} \tag{14}$$

which is the transfer function of an ideal integrator.

We conclude that *the response of the cascade of the two URCs in Figure 5(a) can be obtained as the response of the single-URC circuit in Figure 3; thus, in a sense, the cascade behavior is emulated here by using a single URC element twice: once with cm excitation, and once with dm excitation. This element re-use is such that the two modes are oblivious to each other and do not interact. This principle is shown in Figure 6.*

2.3 Effects of Non idealities on Integrator Performance

Two are the major sources of phase error in Integrator I. First, the lumped parasitic elements at the ports of the URC. These are mostly due to the finite input and output impedances of the transconductors. They can be modeled as grounded parallel R-Cs connected to each port of the URC as shown in Figure 7.

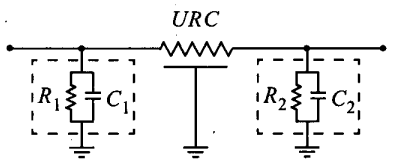

Figure 7: Lumped parasitic elements introduced by non ideal transconductors

Second, the variation of the transconductances from their nominal values. Other sources of error like the additional dynamics of the transconductances and low non-uniformity of the URC seem to be of secondary importance. All these phase error sources are common in all techniques using distributed elements. The advantage here is that there in no need for commensurate URCs. As it was demonstrated in [7], construction requiring pairs of commensurate URCs is extremely sensitive to mismatches.

HSPICE was used to compute the total phase error of Integrator I. The URC was implemented as a MOSFET in the triode region with R implemented by its channel, C implemented by the channel capacitance, and operated with small signals to keep nonlinearities low. The sizes of the transistor were $W/L = 100/3$ which corresponded to a total resistance of $R = 33\ \mathrm{K}\Omega$ and total capacitance of $C = 3\ \mathrm{pF}$. For the parasitics, $R_1 = 1\ \mathrm{M}\Omega$, $R_2 = 1\ \mathrm{M}\Omega$, $C_1 = 6\ \mathrm{fF}$ and $C_1 = 6\ \mathrm{fF}$ were used. The gain g was $160\ \mu\mathrm{A/V}$. All the parasitics and transconductances (including the strengths of the input and output current sources) were assumed independent Gaussian random variables with variance of 5% and 0.5% of their nominal values respectively. Simulations have shown an expected phase variation of about ±2.3 degrees over the 2 decades of best performance. An extensive theoretical phase error analysis is available in [10].

3. Grounded-URC Integrator II

In the second integrator topology, the input is formed by currents I_X that flow antisymmetrically into the two ports of the URC. The feedback loop is realized by the two "internal" voltage dependent current sources that drive the URC symmetrically.

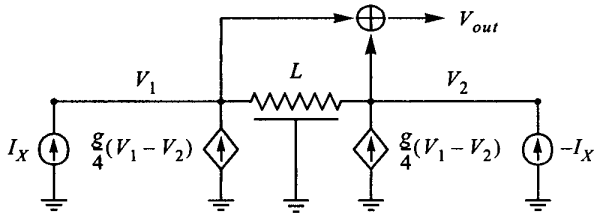

Figure 8: Proposed integrator II

The transfer function of the network is the same with that of integrator I given by equation (14). A decomposition of Integrator II into modes of operation is summarized in Figure 9. Here, the differential mode comes first and the common mode follows. The behavior of Integrator II with respect to phase errors due to parasitic elements and transconductance variation is similar to that of integrator I [10].

The main difference between the two integrators appears in their steady state behavior with zero input I_X. Integrator I requires that the voltage controlled current sources provide current to the URC in order to maintain the output voltage V_Y. On the contrary, when integrator II is in steady state with $I_X = 0$, it is $V_1 - V_2 = 0$ and so no current flows into the URC.

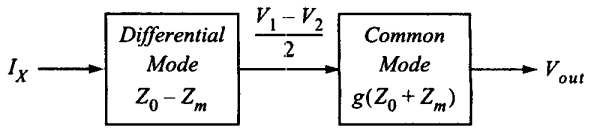

Figure 9: Integrator II as a cascade

4. Conclusions

Two novel integrator topologies using a single grounded URC have been proposed. What makes a single URC sufficient for achieving rational transfer function (integration) is the use of internal feedback that exploits the common and differential modes of operation of the device. The topologies have advantages in comparison to previously proposed architectures that require exactly matched URCs (commensurate) or other more complicated distributed structures. Compared to integrators with ideal capacitors, the two topologies may have an area advantage since the MOS capacitance density is 20-30 times higher than that of the ideal metal to metal (lumped) thin-oxide capacitors commonly available in digital VLSI processes. However, further work will be needed to address the effect of nonlinearities and to find ways to reduce the latter.

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