

Low Power Bus Coding Techniques Considering Inter-wire Capacitances

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1. ABSTRACT

The power dissipation associated with driving data busses can be significant, especially considering the increasing component of inter-wire capacitance. Previous work on bus encoding has focused on minimizing transitions to reduce power dissipation. In this paper, it is shown that transition reduction is not necessarily the best approach for reducing power when the effects of inter-wire capacitance are considered. An electrical model for data busses designed with submicron technologies is presented and a family of coding techniques is proposed that can reduce the average power consumption of the bus by 40%.

2. INTRODUCTION

An important component of the power consumption in digital processors involves the transmission of data through high capacitance busses. Several techniques have been proposed to reduce the power dissipation in these busses through the use of coding techniques, low-swing signaling, and charge recycling [1] [2] [3]. The use of reduced swing communication is attractive, but also suffers from reduced signal to noise ratio, especially as the power supply voltages are scaled [4][5][6][7]. An excellent reference that compares various low-swing techniques is presented in [1].

The coding of data has been explored for reducing power dissipation through the reduction of transitions. The basic idea is to add redundancy to encode the data on the bus. One effective approach proposed is the bus-invert technique in which the data bus is conditionally inverted to reduce the overall transitions [8]. If more than 50% of the bits change, the whole bus is inverted. Therefore, in addition to the data, an extra bit must be transmitted to indicate if the bus is inverted. In [9], temporal data correlations are exploited to reduce switching activity. Fundamental bounds on transition reduction are developed.

3. BUS AND DRIVER MODEL

The previous work on data bus coding use a simple electrical model in which lines are simply replaced by lumped grounded capacitors. Although this model is convenient for closed form mathematical analysis of the power consumption, it is not appropriate for submicron technologies. This is because the smaller scales make the distributive nature of the lines non negligible and even more because lines are placed geometrically closer to each other, so the inter-wire capacitances C_I become important with respect to the substrate capacitances C_L (see Figure 1).

In Figure 1, the lines are shown along with their dominant parasitic elements and their voltages V_1, V_2, \dots, V_n . The C_L is the parasitic capacitance to substrate or other near by elements with constant potentials and the C_I is the parasitic capacitance between

adjacent lines. The values of all C_L 's and C_I 's are assumed not to vary from node to node. For this model not only the transitions of the voltages V_1, V_2, \dots, V_n are responsible for the power consumption but also the relative transitions of the voltages of adjacent lines. This implies that the transition activity by itself is no longer the appropriate "measure" of power consumption. This complicates the exact calculation of the power consumption (making the standard assumption that the data sequences are white noise of 0's and 1's). In future work, we will extend this model to include the distributed nature of the wire.

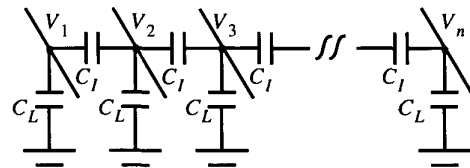


Figure 1: Simple model for the data bus.

In order to calculate the energy consumption caused by a transition using the above model, we need a model for the drivers of the lines too. We adopt the following simple one.

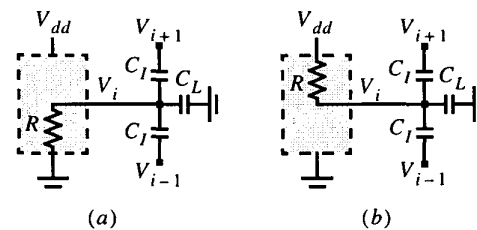


Figure 2: Equivalent circuits for the line drivers.

Figure 2a corresponds to the output of the line driver when it applies a low signal to the line. The resistor R is the *on* resistance of the NMOS. Similarly for the Figure 2b, R is the *on* resistance of the PMOS. The two resistors are not assumed to be constant (similarly to the case described in [10] for a CMOS inverter driving a lumped capacitance).

4. DERIVATION OF THE ENERGY FUNCTION

Combining the model of the data bus with the one of the drivers, we have the circuit in Figure 3. The buffers are replaced by resistors that are either connected to power supply (V_{dd}) or GND.

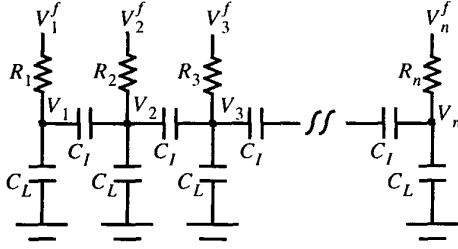


Figure 3: Drivers and lines combined.

The voltages $V_1^f, V_2^f, \dots, V_n^f$ take the values 0 or V_{dd} depending on the *logical* values of the lines we want to establish. Setting

$$\lambda = \frac{C_I}{C_L} \quad (1)$$

we have the following equations describing the operation of the circuit. For $k = 2, \dots, n-1$.

$$C_L \cdot \left[(1 + \lambda) \cdot \frac{dV_1}{dt} - \lambda \cdot \frac{dV_2}{dt} \right] = \frac{V_1^f - V_1}{R_1(t)} \quad (2)$$

$$C_L \cdot \left[-\lambda \cdot \frac{dV_{k-1}}{dt} + (1 + 2\lambda) \cdot \frac{dV_k}{dt} - \lambda \cdot \frac{dV_{k+1}}{dt} \right] = \frac{V_k^f - V_k}{R_k(t)} \quad (3)$$

$$C_L \cdot \left[-\lambda \cdot \frac{dV_{n-1}}{dt} + (1 + \lambda) \cdot \frac{dV_n}{dt} \right] = \frac{V_n^f - V_n}{R_n(t)} \quad (4)$$

Now let

$$V_1(0) = V_1^i, \dots, V_n(0) = V_n^i \quad (5)$$

be the initial values of the voltages V_1, V_2, \dots, V_n , and each of the $V_1^i, V_2^i, \dots, V_n^i$ is either 0 or V_{dd} . The final values of the voltages practically exist and are $V_1^f, V_2^f, \dots, V_n^f$. Here we do the reasonable assumption that the clock period is long enough for the voltages to settle in their new values, so,

$$V_1(\infty) = V_1^f, \dots, V_n(\infty) = V_n^f \quad (6)$$

The energy consumed (or deposited) by the driver k during the transition is:

$$E_k = \int_0^\infty V_k^f \cdot \left(\frac{V_k^f - V_k(t)}{R_k(t)} \right) dt = V_k^f \cdot \int_0^\infty \left(\frac{V_k^f - V_k(t)}{R_k(t)} \right) dt \quad (7)$$

Integrating Equations 2, 3, 4 from 0 to infinity and using Equations 5,6,7 we get,

$$E_1 = C_L \cdot [(1 + \lambda) \cdot (V_1^f - V_1^i) - \lambda \cdot (V_2^f - V_2^i)] \cdot V_1^f \quad (8)$$

$$E_k = C_L \cdot [-\lambda \cdot (V_{k-1}^f - V_{k-1}^i) + (1 + 2\lambda) \cdot (V_k^f - V_k^i) - \dots \dots -\lambda \cdot (V_{k+1}^f - V_{k+1}^i)] \cdot V_k^f \quad (9)$$

$$E_n = C_L \cdot [-\lambda \cdot (V_{n-1}^f - V_{n-1}^i) + (1 + \lambda) \cdot (V_n^f - V_n^i)] \cdot V_n^f \quad (10)$$

Hence the total energy consumed during the transition is given by the sum,

$$E = \sum_{r=1}^n E_r = \sum_{r=1}^n E_r^L + \lambda \sum_{j=1}^{n-1} E_j^I \quad (11)$$

where,

$$E_r^L = C_L \cdot V_r^f \cdot (V_r^f - V_r^i) \quad (12)$$

and

$$E_j^I = C_L \cdot [(V_{j+1}^f - V_j^f) \cdot (V_{j+1}^f - V_{j+1}^i + V_j^i - V_j^f)] \quad (13)$$

$$= C_L \cdot [(V_{j+1}^f - V_j^f)^2 + (V_{j+1}^f - V_j^f) \cdot (V_j^i - V_{j+1}^i)]$$

It should be mentioned that if we normalize the energy function by setting $C_L = 1$ and $V_{dd} = 1$, then the multiplications of the form $V_x^y \cdot V_z^w$ for any x, y, z, w , are reduced to logical AND operations. The calculation of the energy E is then completed by counting *ones* and doing five additions and one multiplication (assuming λ is a convenient rational number could save a lot of complexity in the multiplication).

5. BUS CODING TECHNIQUES

For a data bus with m -lines one way of coding for low power is first to expand it by adding a -more lines and then modify the driving circuit of the bus so that only the words of a subset Z of the (total) set $T = \{0, 1\}^{m+a}$ are transmitted. The subset Z must contain at least 2^m words whose average energy cost of use is less than that of the original bus.

It is a principle of coding theory that the larger the data set you want to compress the higher the efficiency of the compression is. The same is true for coding techniques that achieve power reduction in data busses. Suppose that we could afford a large latency in the data transmission. Then we could store a long sequence of data, process it and then transmit it through the data bus. This in general would allow for very efficient power saving algorithms. Unfortunately a large latency is not usually acceptable. Therefore we propose a family of coding schemes with minimal latency. Let

$$D(k) = (d_1(k), d_2(k), \dots, d_m(k)) \quad (14)$$

be the data vector that must be encoded and transmitted at time k and let

$$L(k) = (l_1(k), l_2(k), \dots, l_n(k)) \quad (15)$$

be the vector containing the logical values of the bus lines at time k . We set $n = m + a$ and decompose the vector $L(k)$ into two parts. The *data* part,

$$L^D(k) = (l_1(k), l_2(k), \dots, l_m(k)) \quad (16)$$

and the *code* part,

$$L^C(k) = (l_{m+1}(k), l_{m+2}(k), \dots, l_n(k)). \quad (17)$$

$$100\left(1 - \frac{E_c}{E_0}\right)\% \quad (21)$$

Where E_c is the total energy consumed when the coding was used and E_0 is the total energy consumed without coding. The energies were calculated using Equations 11,12,13. In this initial research, the power consumption of the encoder and decoder circuits were ignored. This approximation remains valid for very high capacitance data busses and for small values of the parameter a , where the complexity of the circuits is low. The results presented here however, provide a bound on the energy savings.

7. CONCLUSIONS

In this paper a new coding technique for low power has been presented. It is based on an model for data bus that explicitly considers the inter-wire capacitance. It was observed that the power dissipation is no longer minimized by simply minimizing the transition activity. Depending on the technology parameters (i.e., the relative size of inter-wire capacitance to the substrate capacitance), our proposed coding technique could save up to 40% of the power consumed by the drivers of the lines.

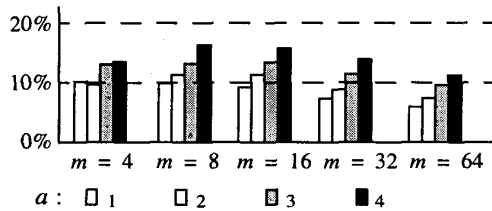


Figure 5: Energy savings with $\lambda = 0$.

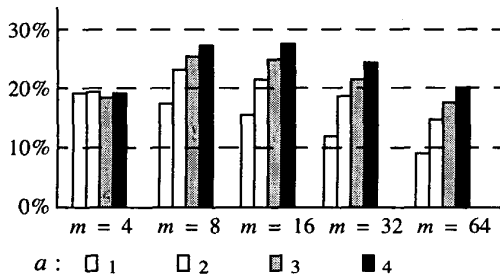


Figure 6: Energy savings with $\lambda = 1$.

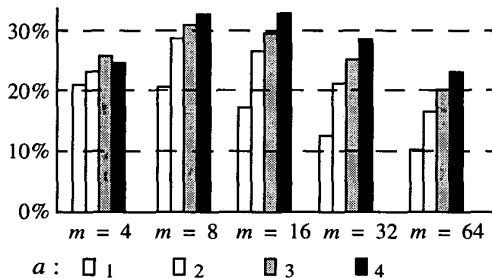


Figure 7: Energy savings with $\lambda = 2$.

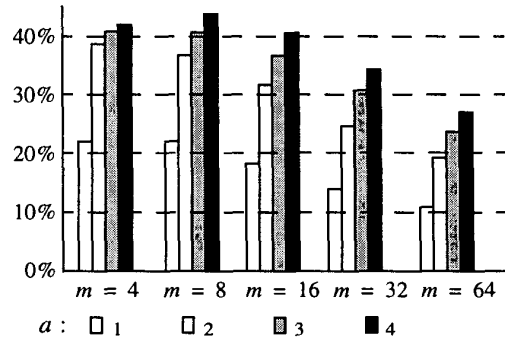


Figure 8: Energy savings with $\lambda = \infty$.

8. ACKNOWLEDGEMENTS

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