Analog and RF Circuit Constrained Optimization Using Multi-Objective Evolutionary Algorithms

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***Abstract*—This paper presents a simulation-based optimization method for automatic sizing in analog and RF IC blocks. It introduces a combination of a state-of-the-art Multi Objective evolutionary algorithm (EA) with a new constraint handling approach to effectively explore the high-dimensional constrained design space, typical in every analog and RF IC block design. An additional modification in the core of the EA is also proposed for handling efficiently mixed continuous-integer parameter search spaces. The methodology is illustrated in a Nested-Current-Mirror amplifier and a Wideband Low Noise Amplifier achieving better results than typical constraint handling approaches.**

***Index Terms*—sizing, optimization, analog, evolutionary algorithms**

I. Introduction

Over the past decades and with the continuing transistor miniaturization, the demand for mixed-signal systems-on-a-chip (SoCs) with increased functionalities and reduced cost for applications such as automotive, portable devices and communications has increased exponentially. However, transistor scaling entails problems for the design of such systems, as short channel effects and variations become main issues. Unlike digital Integrated Circuits (ICs) that have established synthesis flows and automated tools to assist the development of complex systems, analog and RF IC design flow automation has not yet reached maturity. Therefore robust automation methods are needed to increase design cycle efficiency.

The main approaches to analog design automation include optimization methods coupled with a circuit simulator and equation based approaches, that seek to optimize closed form representations of circuit-block representations. Although the equation based approach may provide easier optimization tasks, the existence of higher order effects that arise with smaller channel dimensions and the designer's intervention may deteriorate the design procedure. On the other hand, simulation-based approaches face the challenge of spending excessive computational resources for the exploration of the vast design space of analog circuits. Extensive research has attempted to address this problem, with many optimization strategies being proposed and the EAs being state-of-the-art [1], [2] in this direction. Though algorithms in the literature provide ways to handle constrained optimization, which is the essence of circuit sizing, they have been mainly aimed for continuous parameter spaces. However, in analog and RF design, integer ratios appear often, for instance when sizing current mirrors.

This work proposes a new approach to sizing analog and RF building blocks with simulation-based optimization. We aim to address the mixed parameter space of circuits and provide a framework that produces competitive results when constraints are applied, using EAs as the optimiation core. To address the constraint handling part, we note that the main approach, which is motivated by the feasibility rule [3], does not make use of the infeasible space fitness function information. The incorporation of infeasible fitness function information in EAs is recently gaining attention [4]. Here we employ a corresponding scheme using the Non dominated sorting genetic algorithm (NSGA-II) [5]. Our approach can handle integer as well as continuous search spaces, exploit infeasible fitness function information and optimize for multiple objectives.

We argue that our approach can aid the designers to discover the capabilities of a particular design and reason about the competing trade-offs, while exploring the fitness landscape efficiently. To examine its performance, we use it to size two state-of-the-art topologies, a Nested-Current-Mirror amplifier [6] and a wideband low noise amplifier [7]. The remainder of this paper is organized as follows. In section II, the proposed approach is presented. Section III presents experimental results and Section IV concludes the paper.

II. Proposed Approach

Analog and RF schematic sizing is cast to a constrained optimization problem:

$$\begin{aligned} &\text{minimize} \quad f(\vec{x}), \quad \vec{x} = [x_1, x_2, \ldots, x_D]\,, \\ &\text{subject to: } g_j(\vec{x}) \leq 0, \quad j = 1, \ldots, l \\ &\qquad\qquad L_i \leq x_i \leq U_i, \quad i = 1, \ldots, D, \end{aligned}$$

where vector $\vec{x}$ contains the design variables, L_i and U_i are the lower and upper bounds of the i-th variable, $S = \prod_{i=1}^{D}[L_i, U_i]$ is the variable space, f is the objective (fitness) function and g_j is the j-th constraint. In our case, the fitness function contains performance metrics of the circuit to be sized. For a given parameter vector $\vec{x}$, its degree of constraint violation is defined as

$$G(\vec{x}) = \sum_{j} max[0, g_j(\vec{x})].$$

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In the context of simulation-based sizing using EAs, parametrized testbenches are simulated in iterations using a commercial simulator and software platforms, that automate the procedure of data processing and simulation automation. For the remainder of this section, we assume that the reader is familiar with the concepts of EAs and of NSGA-II particularly.

A. Handling Integer Parameters

The trivial approach to treating mixed parameter spaces using EAs is handling discrete parameters as continuous ones. Following mutation, the parameters that need to be discrete are transformed back to the nearest integer value. Though simple, this approach is flawed; in the case that a particular discrete variable is restricted to small ranges at a particular stage of the optimization, it remains unchanged for the remainder of the procedure and therefore hinders exploration [4]. To address this problem, we adopted a quantization scheme: vector $\vec{x}$ is divided into two parts,

$$\vec{x_c} = [x_{c0}, x_{c1}, \dots],$$

$$\vec{x_i} = [x_{i0}, x_{i1}, \dots],$$

where x_{cj} and x_{ij} are the j-th continuous and integer parameters respectively. For the vector containing continuous variables, the bounded polynomial mutation is applied as in [5], while for the integer variables, a Poisson distribution $P(\lambda)$ is assumed. New values for x_{ij} are sampled from $P(\lambda)$, where λ is equal to x_{ij}. This mutation operator boosts exploration and alleviates the problem of stagnation.

B. Constraint Handling

When constraints are present, the goal of the optimizer is twofold; to drive the search to the parameter space region where the constraints are satisfied (feasible region), and then perform an elitist approach to find the optimal solutions. A straightforward approach is the inclusion of penalty terms in the fitness function. Each penalty term is a weighted version of the degree of violation for each constraint. The determination of the weights, however, is left to the designer and may lead to biasing towards some constraint satisfaction on top of others.

A preference based scheme (feasibility rule) provides unbiased operation and has gained recently attention [1]. It compares pairs of candidate solutions as follows:

1) Feasible candidate solutions are preferred than infeasible ones,
2) Amongst feasible solutions, the ones with better fitness function are preferred and,
3) Amongst infeasible solutions, the ones with the least degree of constraint violation are preferred.

This scheme is incorporated on the EA's selection process and drives the population to feasible regions. However, by favouring constraint satisfaction more than fitness function minimization, this approach leads to convergence to feasible, but not optimum parameter regions [4]. This problem is exacerbated in situations where the feasibility regions are disjoint, or the optimum solutions lie close to the feasibility boundary.

Since trade-offs are the essence of circuit sizing, optimum solution may lie close to the infeasible spaces in analog design spaces. Therefore, driven by [8], we introduce a mechanism to the NSGA-II algorithm that executes in parallel with the feasibility rule and makes use of infeasible fitness functions.

At each iteration (generation), the offspring are sorted according to their fitnesses using the non-dominated ranking algorithm. Those candidate vectors that do not survive to the next generation and are on the first pareto level, are stored in an archive. Then, the individuals in the archive and the surviving population are sorted by their degree of constraint violation. The next step is to select k vectors with the minimum (maximum) constraint violation in the archive (population), a total of $2k$ vectors. These are sorted once more using the non-dominating procedure, accounting only for their fitness functions. The k best individuals are placed on the population and the rest are discarded. As a rule of thumb, we choose k to be equal to $1/20$ of the total population.

An example is illustrated in Fig.1, where a 2D Rastrigin function is limited to be feasible only in the regions inside the red curves, i.e.

$$\text{minimize } f(\vec{x}) = \sum_{i=1}^{2} x_i^2 - 10cos(2\pi x_i) + 10,$$

$$\text{subject to: } 3(x_1+7)^2 + x_2^2 \leq 0.3$$
$$(x_1+8)^2 + (x_2-3)^2 \leq 2.$$

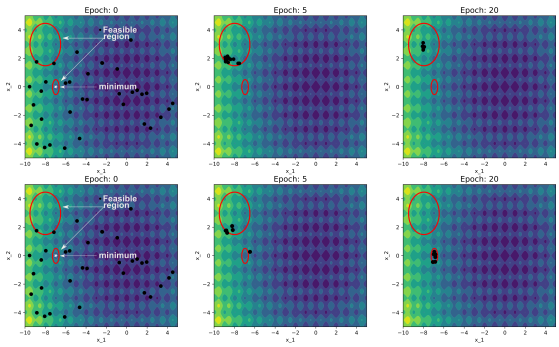

Fig. 1. Top row: Optimization run for a multimodal constrained function, using the feasibility rule. Bottom row: optimization run using the constrained handling method proposed. Initial candidate vectors are identical.

A single-objective Genetic Algorithm (GA) is used to find the minimum of this constrained function. The one using the feasibility rule concentrates its search in the large feasible region, whereas the GA incorporating the constraint-handling method described above, for single-objective this time, searches through both feasible regions.

III. Example Applications

For our experiments, an in-house tool was used to interface the commercial simulator Spectre. Simulations run in batch mode and in parallel, on a machine with an 8-core Intel Xeon processor.

TABLE I
NCM SPECIFICATIONS

Performance	Desicription	Specification
PM	Phase Margin	$\geq 90^o$
GM	Gain Margin	$\geq$ 60dB
A_0	DC Gain	$\geq$ 72dB
N_{10k}	Noise @ 10kHz	$\leq 100nV/\sqrt{Hz}$
SR_{avg}	Slew Rate (average rise and fall)	maximize
Pdc	Total power dissipation	minimize
Design Variable	**Description**	**Constraint**
W_i	MOS Width	$[1-30]$um
L_i	MOS Gate Length	$[0.2-1]$um
K_i	Mirror Parameters	$[1-5]$
V_b	Biasing Voltage	$[0.7-1.1]$V

A. Nested-Current-Mirror amplifier

Here we demonstrate our sizing strategy on the single stage Nested-Current-Mirror amplifier (NCM) [6], shown in Fig. 2. This topology aims to address display applications, where large capacitive loads need to be handled. The ratios of the current mirrors employed in this topology are key parameters for sizing. These are integer numbers and are addressed accordingly with our proposed approach.

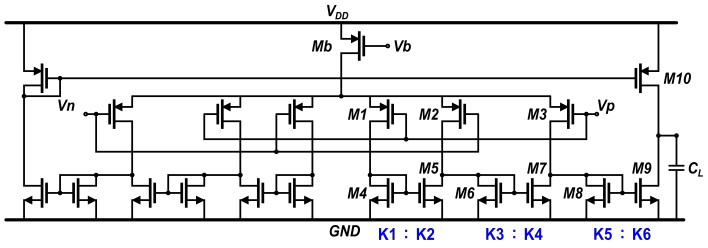

Fig. 2. Nested Current Mirror amplifier proposed in [6]. Half-circuit instance names are shown, since the circuit is symmetric.

For this experiment, we seek to determine the mirror ratios (K1-K6), the unit transistors dimensions and the voltage V_b. Three types of unit transistors are considered, one for nmos devices, one for pmos devices and one for Mb [1]. A TSMC 90nm process is used to design the amplifier.

For comparison, we follow the original implementation of the topology with 15nF load capacitor, V_{DD} = 1.2V and set the design constraints equal to the ones stated in [6]. For trade-off exploration, we optimize for high slew rate and low power consumption. The design constraints and specifications are given in Table I.

Fig. 3 shows the pareto fronts resulting from two NSGA-II optimization runs, one using the feasibility rule and the other using the new constraint handling method. Both experiments use the same set of hyperparameters, with population size and maximum generations set to 200 and 300 respectively, and the mixed-integer mutation scheme proposed. The plot suggests that we are able to size the circuit with better slew rate and power trade-off compared to the original implementation. Also, the proposed constraint handling is able to provide slightly better and denser pareto fronts. The patches in the pareto front of the feasibility rule can be explained as follows: Traversing an infeasible part of the design space to reach non-dominated solutions is easier for the proposed algorithm.

[1]The transistors sizes are defined by parameters K1-K6 and the unit transistors, i.e. M2 width is (K2+K3) times the unit pmos width.

TABLE II
NCM DESIGN VARIABLES

Var	Size	Var	Size	Var	Size	Var	Size
$W_{pmos,nmos}$	1u	$K2$	2	$K5$	1	W_{bias}	6.1u
$L_{pmos,nmos}$	1u	$K3$	1	$K6$	5	L_{bias}	1u
$K1$	2	$K4$	5	V_b	0.98V		

The performance of the two methods is assessed quantitatively using the Hypervolume indicator (HV) [9]. This indicator provides a measure of the region which is dominated by each pareto front and bounded by a reference point, therefore higher HV values are better. Using the same reference point for both pareto fronts, the HV value for the proposed method is $28.5 \cdot 10^4$ whereas for the feasibility rule $18.34 \cdot 10^4$.

The optimization took approximately 20 minutes. Table II provides the sizes for an example solution marked on the pareto front, with 1.2uW power dissipation and the same slew rate as the original implementation ($250\ V/s$).

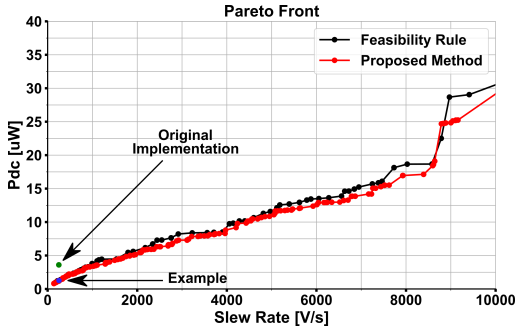

Fig. 3. Pareto fronts for the NSGA-II algorithm with the proposed constraint handling method, and the typical NSGA-II with feasibility rule.

B. Inductorless Wideband LNA

An inductorless, wideband LNA, shown in Fig. 4 [7], is sized in this example. This topology adopts active shunt feedback to achieve wideband operation.

We use the same TSMC 90nm process, with 1.2V supply voltage for both the main and the feedback amplifier. The capacitive load is 50fF and the buffer is considered lossless. In the same manner as in [7], transistor lengths are set to the lowest acceptable value by the process, i.e. 100nm. The design specifications are set equal to the ones shown in the original implementation, with the exception of higher bandwidth, and they are shown in Table III.

The optimization goal is to determine the trade-off between power consumption and Noise Figure. The population count is set to 150 and the maximum generations to 200. The resulting pareto fronts using the NSGA-II with feasibility rule and with the proposed constraint handling method are shown in Fig. 5.

The plot suggests that the proposed method finds wider pareto fronts than the feasibility rule. The HV value for

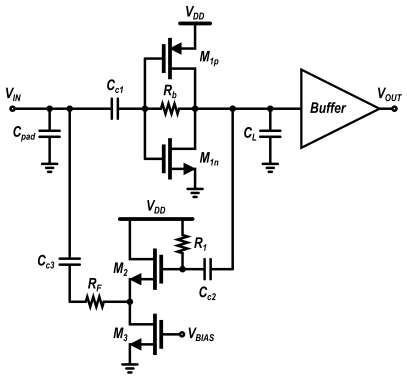

Fig. 4. Inductorless, wideband low noise amplifier proposed in [7].

TABLE III
WIDEBAND LNA SPECIFICATIONS

Performance	Desicription	Specification
S_{11}	Input Matching (entire bandwidth)	≤ -10dB
IIP3	Third-order intercept point @ 2GHz	$\geq$ 8dBm
A_v	Voltage Gain	$\geq$ 18dB
BW	$-$3dB Bandwidth	$\geq$ 3GHz
NF	Noise Figure @ 2GHz	minimize
Pdc	Total power dissipation	minimize
Design Variable	**Description**	**Constraint**
W_i	MOS Width	$[1-100]$um
R_F	Feedback Resistor	$[1-10K]\Omega$
R_b	Self-Biasing Resistor	$[1-20]K\Omega$
R_1	Biasing Resistor	$[1-20]K\Omega$
C_{ci}	Coupling capacitors	$[0.5-10]$pF
V_{BIAS}	M_3 biasing	$[0.3-0.8]$V

the feasibility rule is 26.28 and for the proposed method 100.62, indicating that the proposed method provides more uniform and widespread solutions. Both experiments took approximately 25 minutes.

Repeating the above experiment 5 times, we calculate the figure-of-merit (FOM) for wideband LNAs [7]. The mean FOM for the pareto front of the proposed methodology is 41.2dB, while for the one resulting from feasibility rule and NSGA-II is 39.6dB. We note that the achieved FOM is increased with comparison to the original implementation. The sizes of an example design marked on the pareto front are shown in Table IV.

IV. CONCLUSION

A simulation-based optimization strategy for sizing in nominal conditions of analog and RF building blocks was proposed. In order to improve the efficiency of EAs when sizing analog circuits, we presented a scheme to handle mixed-integer parameter spaces and a new constraint handling method. The proposed approach was demonstrated on an inductorless wideband Low Noise Amplifier and a Nested-Current-Mirror Amplifier. It was shown that mixed-integer optimization provided competitive results and the proposed constraint handling method was able to provide wider pareto fronts and therefore better exploration of the competing trade-offs.

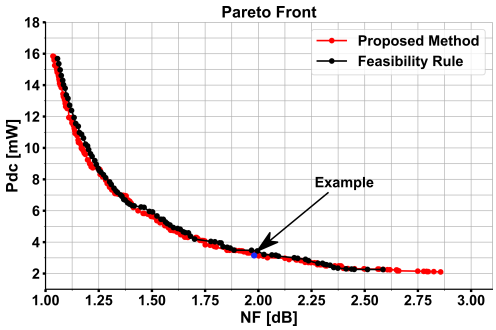

Fig. 5. Pareto fronts for the wideband LNA experiment.

TABLE IV
WIDEBAND LNA DESIGN VARIABLES

Var	Size	Var	Size	Var	Size	Var	Size
W_{1p}	12×1.05u	W_3	3×1.2u	R_F	340 Ω	C_{c3}	900fF
W_{1n}	90×1u	R_1	15.6KΩ	C_{c1}	10pF	V_{BIAS}	0.55V
W_2	10×1.05u	R_b	9KΩ	C_{c2}	5pF		

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