An Analog, Low-Power Threshold Classifier tested on a Bank Note Authentication Dataset

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***Abstract*—Bank note authentication devices are used widely in many large scale stores and companies. Their main focus is to accurately detect all the forged bank notes regardless of a few false alarms on genuine ones. In this work, a low power ($210nW$), area efficient ($0.057mm^2$), analog threshold classifier is proposed to operate as a bank note authentication circuit. The architecture consists of bump and Winner-Take-All circuits. A real-world bank note authentication dataset is used to confirm the proper operation of the proposed classifier, via post-layout simulations in a TSMC 90nm CMOS process, using the Cadence IC Suite. The achieved recall (91.0%) indicates that the classifier is capable of detecting forged bank notes successfully.**

***Index Terms*—Analog VLSI implementation, Area-Efficiency, Bank Note Authentication, Low-Power design, Threshold Classifier**

I. Introduction

Internet of things (IoT) devices capture and create various forms of sensor data such as images and videos. All these devices can be used in a variety of applications which contain information on all aspects of human production and life [1]. Using machine learning (ML) in live applications such as real-time image recognition requires flexible systems and a lot of model training. A rising research topic in IoT domain is Computer Vision, in which information is extracted from images and videos [2]. Machines are able to use computer vision technologies in combination with sensors or actuators and a high accurate software to achieve image recognition. In practice, one or more concepts in an image are recognised by a trained neural network.

Various ML algorithms, offering different accuracy and complexity, have been proposed to tackle the challenges of image classification [2]. Since most image recognition techniques are constrained in terms of processing power, latency and resources, new computing paradigms are necessary. A promising solution is edge computing which pushes processing capabilities closer to the sensor [3]. This solution is critical in applications in which real-time measurements are necessary such as autonomous vehicles, surgical devices, obstacle detection etc [4]. However, this solution reduce the data transfering (minimizing the energy needed for data transferring), but it can consume a high amount of energy.

All these related applications are in many cases implemented by battery and area depended devices [5]. Combining edge [3] and analog computing [6] is an alternative solution since the information processing is based on physical laws with area efficient circuits. This combined with sub-threshold techniques results in more power efficient systems [7]. Given the need for area and power efficient devices and motivated by their increased computation requirements, we propose an analog integrated, low-power, area efficient threshold classifier for general purpose banknote authetication applications. The classifier is designed in TSMC 90nm CMOS process and tested in a real-world banknote authetication dataset [8], compared with a software based implementation.

The remainder of this paper is organized as follows. The mathematcial background regarding the proposed analog integrated threshold classifier are explained in Section II. In Section III, the main building blocks and the proposed architecture are presented. A real-world banknote authetication dataset is used to confirm the proper operation of the proposed classifier in Section IV. A comparison between hardware and software implementation and sensitivity tests are also provided. Some concluding remarks are given in Section V.

II. Threshold Classifier

A threshold classifier is a simplified version of a Support Vector Machine [9]. In practice, it utilizes a multivariate nonlinear transformation ($f()$) to render two, previously intertwined, classes as linearly or almost linearly separable. Then, by tuning a threshold value (I_{th}), it manages to distinguish them as shown in:

$$y = \begin{cases} 1 & \text{if } f(X) \geq I_{th} \\ 2 & \text{if } f(X) < I_{th} \end{cases}, \tag{1}$$

where y is the prediction of the classifier and $\boldsymbol{X}$ is a given input vector. This simple architecture is preferable in hardware implementations since it minimizes chip area in the cost classification accuracy.

In our implementation, $f()$ is chosen to be a sum of multivariate Gaussian function, given by:

$$f(X) = \sum_{k=1}^{K} \frac{1}{\sqrt{2\pi\sigma_k}} e^{\frac{(X-M_k)^2}{\Sigma_k^2}}. \tag{2}$$

Here, K is the number of the selected Guassian functions, M_k and Σ_k are the mean value and covariance matrices of the k-th Gaussian, respectively. The Gaussian function is preferred over other alternatives due to its ease of implementation.

III. Proposed Architecture

The topology of the analog threshold classifier along with its basic building blocks is presented in this Section. In particular, the multivariate Gaussian functions are implemented using a multivariate Bump circuit [10]. The comparison with the threshold value is accomplished using a Winner-Take-All circuit [11]. The entire classifier operates with the supply voltage set to $V_{DD} = -V_{SS} = 0.3V$ and all transistors are biased in the sub-threshold region.

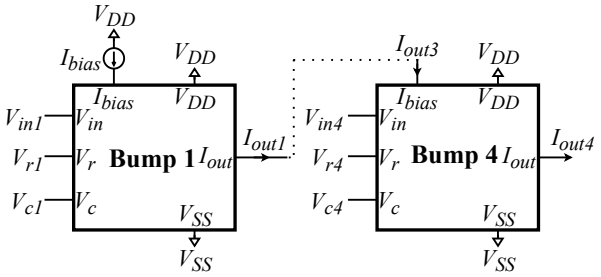

Fig. 1: A multivariate (4-D) Bump circuit composed of 4 univariate Bump circuits connected sequentially. The output of each Bump circuit is used as a bias current for the next one. The output of the last Bump circuit corresponds to the produced Gaussian curve.

Multivariate Bump circuits produce a multivariate Gaussian function in which the mean value matrix is electronically tuned. In some architectures a diagonal covariance matrix can also be altered, affecting the width of the Gaussian function. In this work, the topology implementing a 4-D Gaussian function is presented in Fig. 1. It is composed of 4 identical univariate Bump circuits, connected in a cascaded form [10]. Each Bump circuit, shown in Fig. 2, is fully electronically tuned and therefore the multivariate one is also fully tuned. This allows for full control over the non-linear transformation function in eq. 2. The transistors' dimensions for one Bump circuit are summarized in I.

TABLE I: MOS Transistors' Dimensions (Fig. 2).

NMOS	W/L (µm/µm)	PMOS	W/L (µm/µm)
M_{n1},M_{n4}	1.6/0.4	M_{p1},M_{p2}	1.6/1.6
M_{n2},M_{n3}	0.8/0.4	M_{p3}-M_{p6}	0.4/1.6
M_{n5}-M_{n8}	0.4/1.6	-	-
M_{n9},M_{n10}	1.6/1.6	-	-

The utilized WTA circuit indicates the index of its largest input, hence performing the argmax operator. In the case of a 2-input WTA circuit, shown in Fig. 3, its operation is similar to a comparator. Specifically, by biasing its second input with a constant (threshold) current, the WTA circuit is equivalent to a current-mode comparator. This block is crucial to a threshold classifier, since it is responsible for extracting the classifier's prediction. All transistors' dimensions are set as $W/L = 0.4\mu m/1.6\mu m$.

The proposed threshold classifier, presented in Fig. 4, uses a sum of $k = 2$ Gaussian functions for the non-linear transformation. This is implemented using 2 multivariate Bump

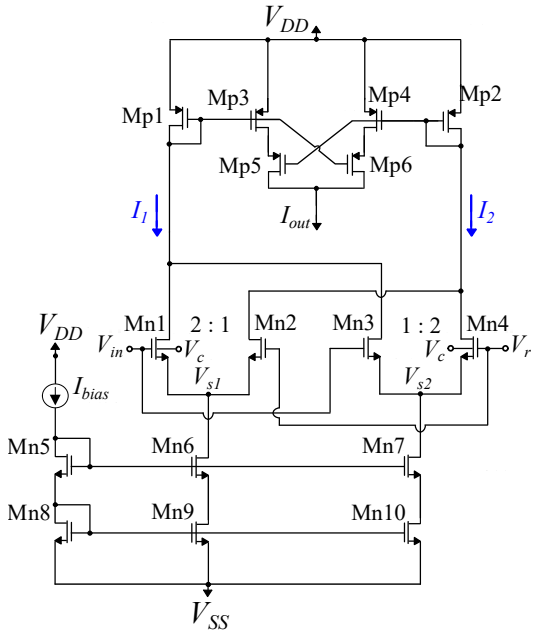

Fig. 2: A differential difference pair Bump circuit. The voltage parameters V_r and V_c and the bias current I_{bias} control the mean value, the variance and the height of the produced Gaussian curve (I_{out}), respectively.

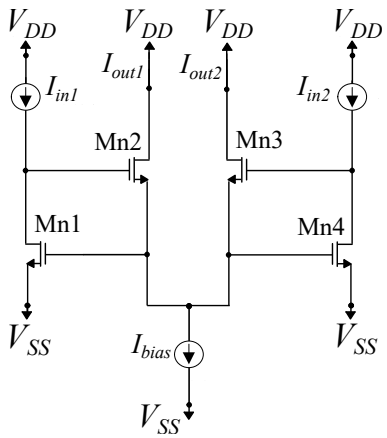

Fig. 3: A WTA circuit with 2 inputs and 2 outputs. Its operation is similar to a current-mode comparator.

circuits and then simply adding their output currents. This summation is then compared to the threshold current $I_{threshold}$ and the classifier's prediction is in fact the WTA's first output current (I_1). This current is in a binary format; a logical 1 (a high current value) indicates the first class as the winning one and a logical 0 (a low current value) the second one. This design is easily scalable for any number of Gaussians and/or dimensions.

IV. Bank Note Authentication Dataset

To test the threshold classifier, a real-world bank note authentication dataset was used [8]. The data include genuine and forged bank notes from the University of Applied Sciences,

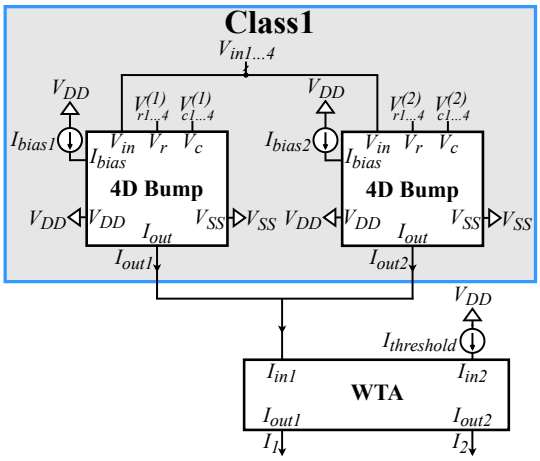

Fig. 4: The proposed threshold classifier. It is comprised of 2 multivariate Bump circuits, performing the non-linear transformation, and 1 WTA circuit acting as a current-mode comparator. The $I_{threshold}$ controls the decision boundary of the classifier.

Ostwestfalen-Lippe. They are recorded using a simple camera and 4 image related features are extracted and used to train a software-based model, which is identical to the analog one. This model's parameters are then imported to the analog circuit for its validation. On the following, two tests, validating the classifier's accuracy and the circuit's stability, are presented. Both of them are conducted on the layout presented in Fig.5.

First, the hardware implementation is compared to the aforementioned software one. Since identifying all the forged banknotes is of vital importance, the comparison is also based on the classifiers recall, given by:

$$\text{recall} = \frac{\text{Identified FBN}}{\text{Identified FBN} + \text{Unidentified FBN}}, \quad (3)$$

where, FBN stands for Forged Bank Notes [12]. To account for the experiment's randomness, the results from 20 different training-test iterations are presented in Figs. 6 and 7. The circuit's sensitivity is confirmed via a Monte Carlo analysis on its layout. In particular, Fig. 8 corresponds to the Monte Carlo Histogram for $N = 200$ points. The results for both tests are also summarized in Table II.

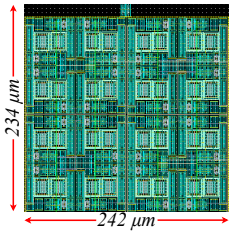

Fig. 5: The layout of the implemented classifier

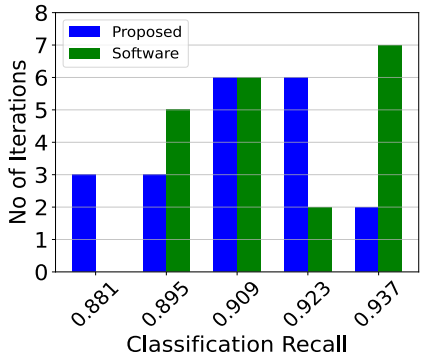

Fig. 6: Comparison between hardware (post-layout simulation) and software implementations over 20 iterations for the proposed classifier, regarding the classification recall.

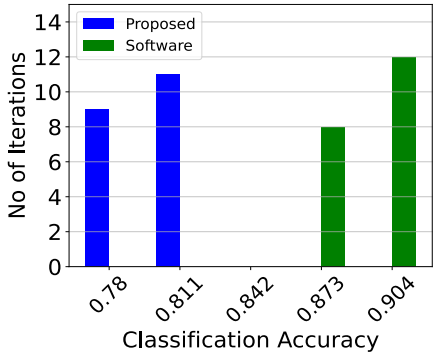

Fig. 7: Comparison between hardware (post-layout simulation) and software implementations over 20 iterations for the proposed classifier, regarding the classification accuracy.

TABLE II: Performance Results for the 2 conducted tests.

Method	Best	Worst	Mean	Std.
Software (recall)	0.944	0.893	0.919	0.017
Proposed (recall)	0.940	0.874	0.910	0.017
Software (accuracy)	0.920	0.864	0.894	0.013
Proposed (accuracy)	0.823	0.765	0.795	0.015
Monte Carlo (recall)	1.000	0.820	0.922	0.027

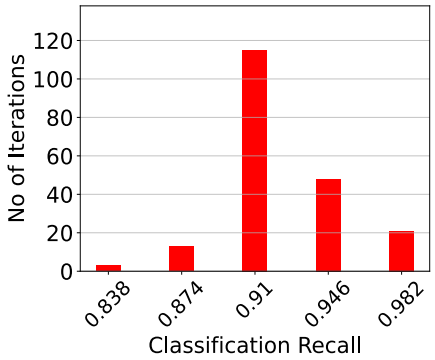

Fig. 8: Post-layout Monte Carlo sensitivity analysis histogram for $N = 200$ points, regarding the classifier's recall score.

V. Analog Classifiers Summary and Discussion

In Table III, a performance summary that includes both model and circuit related parameters is presented. Using Bump circuits as their main building block, a Gaussian Mixture Model (GMM)-based classifier [13], Support Vector Machines

TABLE III: Analog ML Algorithm Summary.
* No. of dimensions designed on the layout.

	Technology	Classifier	No. of dimensions	Power Consumption	Energy per classification	Area
This work	$90nm$	Threshold	4	$210nW$	$\frac{2.5\ \text{pJ}}{\text{classification}}$	$0.057mm^2$
[13]	$90nm$	GMM	*16	$12.0\mu W$	$\frac{96\ \text{pJ}}{\text{classification}}$	$0.451mm^2$
[14]	$0.5\mu m$	SVM	N/A	$5.9mW$	$\frac{460\ \text{pJ}}{\text{sample}}$	$9.000mm^2$
[15]	$180nm$	SVM	2	$220.0\mu W$	$\frac{252\ \text{pJ}}{\text{vector}}$	$0.060mm^2$
[16]	$0.5\mu m$	SVM	14	$840.0nW$	$\frac{21\ \text{nJ}}{\text{classification}}$	$9.000mm^2$
[17]	$90nm$	Bayesian	5	$365nW$	$\frac{2.15\ \text{pJ}}{\text{classification}}$	$0.030mm^2$
[18]	$90nm$	GRBFN	7	$112 \sim 520nW$	$\frac{0.66\sim3.1\ \text{pJ}}{\text{classification}}$	$0.050mm^2$
[19]	$180nm$	K-means	2	$1.53\mu W$	N/A	$0.951mm^2$
[20]	$180nm$	LSTM	16X16	$460.3mW$	N/A	$9.990mm^2$

(SVM) [14]–[16], a Bayesian classifier [17], a Gaussian Radial Basis Function Network (GRBFN) [18], a K-means-based classifier [19] and a Long Short-Term Memory network (LSTM) [20] have been proposed in literature. The main criteria for selecting a specific model/network is the trade-off between accuracy and system complexity or resources. In this work, we focus on the power and area efficiency, while maintaining a reasonable accuracy. To this end, we proposed a low-power ($210\ nW$), area efficient ($0.057mm^2$), analog threshold classifier.

VI. Conclusion

An analog integrated, low power, area efficient threshold classifier was proposed in this work. Its main building blocks are bump circuits along with a current-mode comparator (WTA circuit). A real-world bank note authentication dataset was used to validate the classifier's performance. All post-layout simulation results are conducted in a TSMC 90nm CMOS process and are compared with a software-based implementation. Its sufficient recall allows for its operation as either a stand alone device or a wake up circuitry, when a need for higher security is required.

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