A Precise, Power-Efficient, Analog-Hardware Edge Detector for Biomedical Imaging

Vassilis Alimisis, Argyro Kamperi, Georgios Gennis and Paul P. Sotiriadis

Department of Electrical and Computer Engineering
National Technical University of Athens, Greece
E-mail: alimisisv@gmail.com, argykaberi@gmail.com, giorgosyennis@gmail.com, pps@ieee.org

2024 IEEE International Symposium on Biomedical Imaging (ISBI) | 979-8-3503-1333-8/24/$31.00 ©2024 IEEE | DOI: 10.1109/ISBI56570.2024.10635210

***Abstract*—Edge detection stands as a pivotal tool across a spectrum of Biomedical imaging applications. One prominent use case involves discerning spatial boundaries within an image, facilitating subsequent tumor or broken bone separation and identification. While edge detection typically demands significant computational resources, the inherently parallelizable nature of this implementation offers distinct advantages over other power-hungry approaches. In this study, an analog-hardware approximation of the Robert's Cross operator is introduced, based on Gaussian function circuits to achieve notable gains in area/power efficiency and high accuracy. The implemented design is tested using three biomedical images, yielding a high Structural Similarity Index Metric of ~ 0.8 while requiring an area of $1912\mu m^2$ per pixel. The proposed architecture was implemented and simulated in a TSMC 90nm CMOS process, utilizing the Cadence IC Suite.**

***Index Terms*—Analog integrated circuits, Biomedical imaging, Bump circuit, Edge detector, Low-power design**

I. Introduction

Biomedical imaging is a transformative field that lies at the intersection of medicine, engineering and technology, fundamentally reshaping our comprehension and diagnosis of intricate physiological processes within the human body [1]. Employing a diverse range of cutting-edge techniques including X-ray, computed tomography (CT) scans, Magnetic Resonance Imaging (MRI) and ultrasound, biomedical imaging empowers us to peer into the detailed structures and functions of living organisms with unprecedented clarity [2]. This invaluable tool not only facilitates early disease detection and precise localization but also guides surgical interventions and monitors treatment responses [2]. Through harnessing the potential of advanced imaging modalities, researchers and healthcare professionals are forging a path towards more effective therapies and improved patient outcomes [3]. The integration of biology and technology in biomedical imaging holds the promise of a future where diagnoses are more precise, treatments are highly personalized and lives are positively influenced on a global scale.

The combination of Computer Vision (CV) and biomedical imaging can extract meaningful information from images and videos [4]. This enables greater precision in medicine. By leveraging the computational ability of computer vision algorithms, we empower machines to discern, analyze and interpret intricate visual data derived from the human body [4]. From early disease diagnosis to surgical planning and treatment evaluation, this combined approach helps patient care [5]. The only difficulty is that achieving real-time automatic extraction, analysis and processing of the vast amounts of data, even for relatively straightforward computer vision tasks, necessitates an unprecedented level of performance [6]. At present, technologies such as Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs) and Graphic Processing Units (GPUs) have significantly advanced in meeting this surge in computational requirements [7]. An alternative solution to the previous power harvesting architectures is analog computing, which offers advantages in terms of power efficiency and speed [8]. This makes it well-suited for meeting the real-time processing requirements in medical imaging. In pursuit of this goal, this work introduces a precise, power-efficient and compact analog integrated image edge detector.

In the existing literature, with the exception of [9], [10] (our previous works), there are only a limited number of works related to analog integrated-based image edge detection. Notably, the approach detailed in [11] stands out for its good power management and compact area allocation per pixel. Alternatively, other designs emphasizing system efficiency opt for the implementation of either current-based [12] or voltage-mode [13]–[15] convolution filters. Conversely, [16] and [17] concentrate on the integration of a more precise algorithm, specifically the Sobel operator for edge detection [18], albeit at the expense of increased area and power consumption. Finally, an unconventional approach is outlined in [19], where an edge detector utilizing erosion and dilation operators is introduced. This diverse array of methodologies demonstrates the multidimensionality of analog-based image edge detection techniques.

The rest of this work is ordered in the following manner. The related background of this work is analysed in Section II. The implemented architecture is proposed in Section III. The simulation results are provided and the metrics are compared to related works in Section IV. Finally, Section V concludes this work.

II. Background

The Regional Convolutional Operator (RCO) identifies areas in the diagonal direction that exhibit high spatial frequency,

mirroring the perceptual tendencies observed in human vision [20]. For an image with a resolution of $N \times M$, the light intensity of a pixel at coordinates (i, j) in grayscale is represented by $x_{i,j}$. It's worth noting that for every $i < N$ and $j < M$, the RCO provides an approximation of the image's gradient, denoted as $z_{i,j}$, as illustrated below:

$$z_{i,j} = \sqrt{(\sqrt{x_{i,j}} - \sqrt{x_{i+1,j+1}})^2 + (\sqrt{x_{i+1,j}} - \sqrt{x_{i,j+1}})^2}. \tag{1}$$

The computations involved in these processes necessitate intricate analog hardware circuitry. Therefore, [9] introduces a hardware-optimized adaptation of the RCO, tailored to harness the advantages of Bump circuits, a specialized type of Gaussian function generation circuit [21]. This modification proves instrumental in the deployment of an analog integrated image edge detector. In this revised algorithm, equation (1) encapsulates the transformed form of the RCO's formula, streamlining its application in practical hardware configurations:

$$\hat{z}_{i,j} = 2\pi \cdot \sigma^2 \cdot \mathcal{N}(y_{i,j} \| y_{i+1,j+1}, \sigma^2) \cdot \mathcal{N}(y_{i+1,j} \| y_{i,j+1}, \sigma^2), \tag{2}$$

where $\mathcal{N}(x \| \mu, \sigma^2)$ describes the univariate Gaussian function which is expressed by:

$$\mathcal{N}(x \| \mu, \sigma^2) = \frac{1}{\sqrt{(2\pi) \cdot \sigma^2}} \; e^{-\frac{1}{2} \cdot \frac{(x-\mu)^2}{\sigma^2}}. \tag{3}$$

In this context, μ represents the mean value while σ signifies the variance of the Gaussian function. Also, a straightforward threshold circuit distinguishing between edges and non-edges can be employed to generate a binary output. In this work, however, it is not necessary since edges and non-edges are separated easily. In comparison with the previous works [9], [10], the implemented one is more precise and it can implement a fully tunable and accurate Gaussian curve which is necessary for biomedical imaging.

III. Proposed Design

In this study we adopt the framework proposed in [9], enhancing it with a precise, power-efficient voltage-mode Bump circuit [22]. Furthermore, the design is simplified by removing the previously employed threshold circuit (edges and non-edges are recognized). It's worth emphasizing that all transistors function within the sub-threshold domain with power supply rails set to $V_{DD} = -V_{SS} = 0.3V$.

A. Edge Detector Circuitry

In this work, a differential difference voltage-mode Bump circuit is utilized [22] depicted in Fig. 1. This configuration consists of a differential difference pair (two differential pairs) and a symmetric current correlator, biased by a current mirror I_{bias}. The differential pairs operation yield two drain currents denoted as I_1 and I_2, related to the two neuron currents in previous studies [9], [21]. These sigmoidal currents drive the correlator's output, resulting in a response akin to a Gaussian curve. The bias current, denoted as I_{bias}, tunes the amplitude of this curve. Notably, in this setup, adjustments to the variance

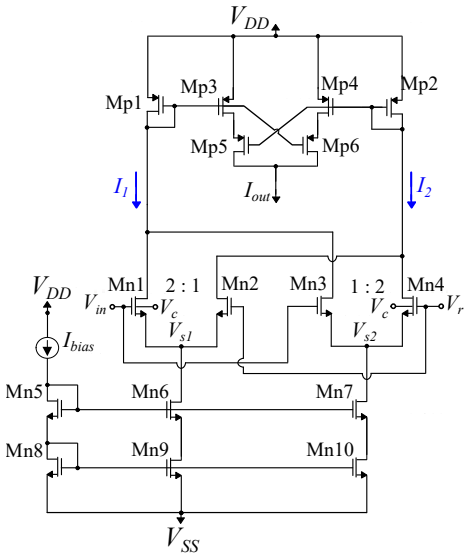

Fig. 1: A Gaussian Function circuit has been successfully integrated, wherein the voltage V_{in} serves as the system's input. The parameters V_r and V_c along with the bias current I_{bias} are utilized to fine-tune the mean value, variance and amplitude of the Bell-shaped function. This configuration enables precise control over the characteristics of the function, enhancing its adaptability to diverse input scenarios.

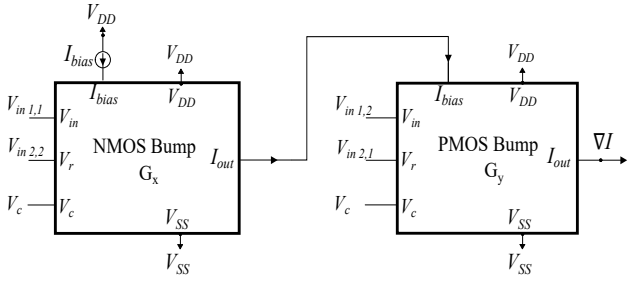

Fig. 2: The analog hardware implementation of a Robert Cross Operator. It consists of two cascaded Bump circuit.

of the Gaussian curve can be made by tuning the voltage parameter V_c. However, for the RCO, fine-tuning the variance of the Gaussian function provides a higher quality output for biomedical images.

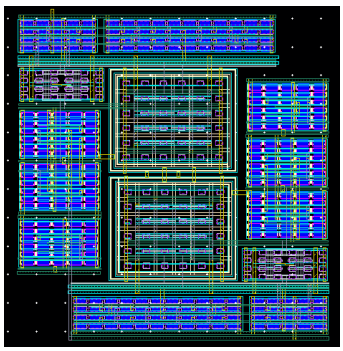

Fig. 3: The implementation of the RCO cell's Layout.

In equation (2) the RCO's outcome is determined by the multiplication of two Gaussian functions. The choice of Bump circuits proves pivotal as they demonstrate remarkable efficiency in carrying out this multiplication task without the need for supplementary components (e.g. analog multipliers). By biasing the second Bump circuit with the output current of the first, the resulting output current precisely represents the product of their individual Gaussian curves [23]. It is important to note that, in this setup, only the first Bump circuit is subjected to a designated external bias current (I_{bias}). In contrast to [9], this study takes a different approach to minimize the circuit's footprint. Specifically, the second Bump circuit undergoes a redesign, opting for a PMOS-based configuration, a depiction of which is presented in Fig. 2. Furthermore, manipulating the bulk voltage of bulk-controlled transistors like M_{n1} and M_{n4} enables to effectively regulate the circuit's output, allowing for the detection of more or fewer edges depending on the specific application at hand. Finally, the dimensions of all transistors are detailed in Table I.

TABLE I: MOS Transistors' Dimensions (Fig. 1).

Block	**W/L** ($\mu m/\mu m$)	**Current Correlator**	**W/L** ($\mu m/\mu m$)
M_{n1},M_{n4}	1.6/0.4	M_{p1},M_{p2}	1.6/1.6
M_{n2},M_{n3}	0.8/0.4	M_{p3}-M_{p6}	0.4/1.6
M_{n5}-M_{n8}	0.4/1.6	-	-
M_{n9},M_{n10}	1.6/1.6	-	-

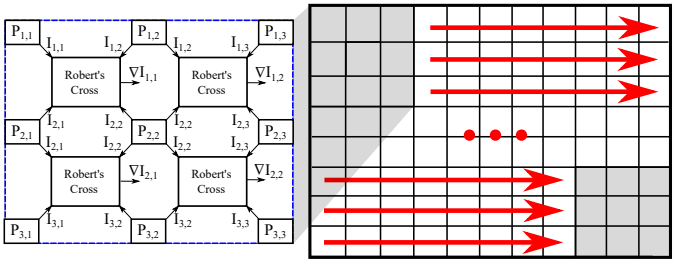

Fig. 4: The proposed system-level architecture entails the deployment of a multi-cell analog edge detector that systematically scans the entirety of the image. This approach allows for comprehensive and detailed edge detection across the entire visual field.

B. High-Level Implementation

In the related study [9], various system-level architectures were introduced, each offering distinct trade-offs between computation speed, chip area and power consumption. While some architectures achieved high frame-per-second (FPS) values, a crucial goal for an edge detector in hardware, they proved impractical in terms of ASIC area. In this endeavour we have managed to substantially reduce the size of the RCO's cell, as evidenced by the layout depicted in Fig. 3, eliminating the need for the threshold circuit. To mitigate for manufacturing precision and fabrication mismatch effects, the common-centroid technique is implemented in the layout design, necessitating the use of additional dummy transistors. In a high-level design the dummies can be minimized or altered with active ones. Moreover, they can potentially accommodate the integration of photodiodes and/or multiple cells in close proximity, leading to an even more substantial reduction in the overall chip area. Consequently, architectures resembling the one exemplified in Fig. 4 can incorporate numerous RCO cells before approaching an impractical size.

IV. Simulation Results and Comparison Study

In this section we conduct a comparative analysis involving analog integrated implementations, for example the current work and our previous related study [9]. Both analog architectures and their corresponding simulation results are executed within a TSMC 90nm CMOS process, utilizing the Cadence IC suite. To ensure a comprehensive evaluation across diverse biomedical images, our comparison is based on three distinct image scenarios: XRAY hand, foot and scalp [24]. The binary images for all cases are depicted in Fig. 5. Similar to our prior research we employ three key metrics to underscore the advantages of this implementation: the layout area per pixel (LAP), the Structural Similarity Index Metric (SSIM) and the power consumption per pixel (PCP). For a detailed summary of these results refer to Table II. The LAP and PCP metrics, which remain independent of the chosen image, are presented in Table III. However, it's worth noting that the visual assessment of the images generated by the analog circuits is also crucial.

TABLE II: Analog Edge Detectors: Performance Overview

Work	**Image**	**Resolution**	**Total Power Consumption**	**SSIM**
[9]	Hand	697×416	$9.7\mu W$	0.73
This work	Hand	697×416	$9.1\mu W$	0.77
[9]	Foot	458×515	$5.6\mu W$	0.81
This work	Foot	458×515	$5.1\mu W$	0.83
[9]	Scalp	520×515	$5.9\mu W$	0.76
This work	Scalp	520×515	$5.4\mu W$	0.82

Concluding the assessment, a Monte-Carlo analysis is performed involving $N = 200$ points to evaluate the circuit's resilience to Process, Voltage and Temperature (PVT) fluctuations. The focus of this examination lies on the threshold boundary of the circuit translated as the voltage disparity between two diagonal pixels. Results indicate a mean distance of $\mu = 2$mV accompanied by a standard deviation of $\sigma = 0.7$mV under PVT variations. Notably, this study demonstrates considerably higher sensitivity to PVT variations compared to our earlier work [9].

Given the primary objective of this study to optimize LAP and PCP metrics while providing high-quality results, a comprehensive comparison is presented in Table III, in contrast to our approach with other analog edge detection methods from existing literature. It's worth noting that assessing the image quality produced by these methods may not be entirely equitable. Notably, the proposed methodology demonstrates high performance in terms of PCP and achieves the highest attainable FPS in scenarios where a fully parallel architecture

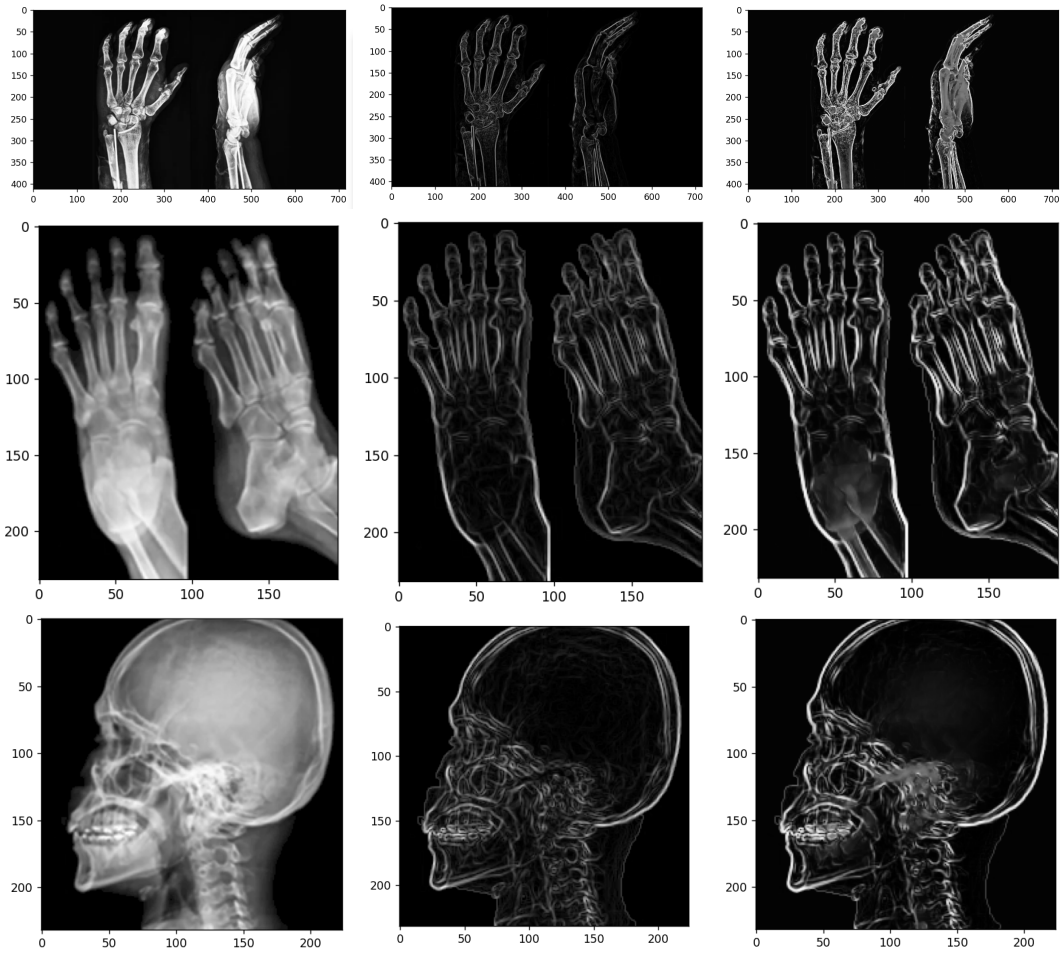

Fig. 5: Images provided by: Left: the prototype image. Center: the software-based edge detector. Right: the analog hardware edge detector proposed in this work.

TABLE III: Analog Edge Detectors: Performance Overview

	Technology	**Supply Voltage**	**PCP**	**FPS**	**LAP**
This work	90nm	0.6V	23nW	$130K$	$1912\mu m^2$
[9]	90nm	0.6V	33nW	$100K$	$2392\mu m^2$
[10]	90nm	0.6V	14nW	$100K$	$956\mu m^2$
[11]	180nm	1.8V	0.9μW	1300	$225\mu m^2$
[12]	600nm	1.8V	3.6μW	50	$100\mu m^2$
[13]	350nm	3.3V	5.8μW	N/A	$1125\mu m^2$
[14]	250nm	N/A	1.2μW	N/A	$633\mu m^2$
[16]	150nm	1.8V	790μW	75	$140\mu m^2$
[17]	350nm	3.3V	26.8μW	2000	$1125\mu m^2$
[19]	500nm	1.8V	368μW	N/A	$8600\mu m^2$

is employed. Nevertheless, it's important to acknowledge that despite the reduction in chip area achieved in this work, there are still other approaches in the literature that manage to achieve an even more compact footprint. The primary accomplishment lies in the attainment of high-quality results while maintaining comparable levels of PCP and LAP.

V. Conclusion

This work introduces an analog edge detector capable of achieving a small per-pixel area that enables highly parallel architectures, making it adept at processing even high-definition images. In a fully parallel setup the proposed edge detector demonstrates the capacity to process images at impressive rates of up to 130 thousand frames per second while consuming a mere 23nW per pixel. This substantial advancement can be primarily attributed to the utilization of a voltage-mode and differential difference Bump circuit. To comprehensively evaluate the proposed architecture, three medium-resolution images representing biomedical imaging applications were employed. Through simulation in a TSMC 90nm CMOS process the resulting edge images affirm the high quality of the output. In conclusion, the presented architecture stands as a prime contender for serving as a pre-processing block in various biomedical imaging systems necessitating robust edge detection capabilities.

REFERENCES

[1] A. Webb, *Introduction to biomedical imaging*. John Wiley & Sons, 2022.

[2] R. Y. Kwong and E. K. Yucel, "Computed tomography scan and magnetic resonance imaging," *Circulation*, vol. 108, no. 15, pp. e104–e106, 2003.

[3] S. E. Dilsizian and E. L. Siegel, "Artificial intelligence in medicine and cardiac imaging: harnessing big data and advanced computing to provide personalized medical diagnosis and treatment," *Current cardiology reports*, vol. 16, pp. 1–8, 2014.

[4] A. Esteva, K. Chou, S. Yeung, N. Naik, A. Madani, A. Mottaghi, Y. Liu, E. Topol, J. Dean, and R. Socher, "Deep learning-enabled medical computer vision," *NPJ digital medicine*, vol. 4, no. 1, p. 5, 2021.

[5] J. Olveres, G. González, F. Torres, J. C. Moreno-Tagle, E. Carbajal-Degante, A. Valencia-Rodríguez, N. Méndez-Sánchez, and B. Escalante-Ramírez, "What is new in computer vision and artificial intelligence in medical image analysis applications," *Quantitative imaging in medicine and surgery*, vol. 11, no. 8, p. 3830, 2021.

[6] M. Bertozzi, A. Broggi, and A. Fascioli, "Vision-based intelligent vehicles: State of the art and perspectives," *Robotics and Autonomous systems*, vol. 32, no. 1, pp. 1–16, 2000.

[7] D. Moolchandani, A. Kumar, and S. R. Sarangi, "Accelerating cnn inference on asics: A survey," *Journal of Systems Architecture*, vol. 113, p. 101887, 2021.

[8] W. Haensch, T. Gokmen, and R. Puri, "The next generation of deep learning hardware: Analog computing," *Proceedings of the IEEE*, vol. 107, no. 1, pp. 108–122, 2018.

[9] G. Gennis, V. Alimisis, C. Dimas, and P. P. Sotiriadis, "A general purpose, low power, analog integrated image edge detector, based on a current-mode gaussian function circuit," *Analog Integrated Circuits and Signal Processing*, pp. 1–12, 2022.

[10] G. Gennis, A. Kamperi, V. Alimisis, C. Dimas, and P. P. Sotiriadis, "An area-efficient, analog integrated image edge detector based on the robert's cross operator," in *2023 12th International Conference on Modern Circuits and Systems Technologies (MOCAST)*. IEEE, 2023, pp. 1–4.

[11] M. Nam and K. Cho, "Implementation of real-time image edge detector based on a bump circuit and active pixels in a cmos image sensor," *Integration*, vol. 60, pp. 56–62, 2018.

[12] R. Njuguna and V. Gruev, "Low power programmable current mode computational imaging sensor," *IEEE Sensors Journal*, vol. 12, no. 4, pp. 727–736, 2011.

[13] N. Massari, M. Gottardi, L. Gonzo, D. Stoppa, and A. Simoni, "A cmos image sensor with programmable pixel-level analog processing," *IEEE Transactions on Neural Networks*, vol. 16, no. 6, pp. 1673–1684, 2005.

[14] J.-H. Kim, J.-S. Kong, S.-H. Suh, M. Lee, J.-K. Shin, H. B. Park, and C. A. Choi, "A low power analog cmos vision chip for edge detection using electronic switches," *ETRI journal*, vol. 27, no. 5, pp. 539–544, 2005.

[15] L. Dron, "The multiscale veto model: A two-stage analog network for edge detection and image reconstruction," *International Journal of Computer Vision*, vol. 11, no. 1, pp. 45–61, 1993.

[16] C. Soell, L. Shi, J. Roeber, M. Reichenbach, R. Weigel, and A. Hagelauer, "Low-power analog smart camera sensor for edge detection," in *2016 IEEE international conference on image processing (ICIP)*. IEEE, 2016, pp. 4408–4412.

[17] J. Dubois, D. Ginhac, M. Paindavoine, and B. Heyrman, "A 10 000 fps cmos sensor with massively parallel image processing," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 706–717, 2008.

[18] O. R. Vincent, O. Folorunso *et al.*, "A descriptive algorithm for sobel image edge detection," in *Proceedings of informing science & IT education conference (InSITE)*, vol. 40, 2009, pp. 97–107.

[19] L. A. S. Gaspariano and A. D. Sánchez, "Analog cmos morphological edge detector for gray-scale images."

[20] L. Roberts, "Machine perception of 3-d solids, optical and electro-optical information processing," 1965.

[21] V. Alimisis, M. Gourdouparis, G. Gennis, C. Dimas, and P. P. Sotiriadis, "Analog gaussian function circuit: Architectures, operating principles and applications," *Electronics*, vol. 10, no. 20, p. 2530, 2021.

[22] V. Alimisis, G. Gennis, K. Touloupas, C. Dimas, M. Gourdouparis, and P. P. Sotiriadis, "Gaussian mixture model classifier analog integrated low-power implementation with applications in fault management detection," *Microelectronics Journal*, vol. 126, p. 105510, 2022.

[23] V. Alimisis, M. Gourdouparis, C. Dimas, and P. P. Sotiriadis, "A 0.6 v, 3.3 nw, adjustable gaussian circuit for tunable kernel functions," in *2021 34th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI)*. IEEE, 2021, pp. 1–6.

[24] [Online]. Available: https://www.ucsfhealth.org/medical-tests/x-ray—skeleton