A Multistage Nested-Loops Stabilized Operational Amplifier

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***Abstract*—In this paper, a nested $g_m - C$ loops operational amplifier has been implemented, using cascade gain stages, Miller compensation capacitors and feedforward amplifying paths. Special care is given to thoroughly analyze the mathematical background of this compensation technique. The implemented circuit is designed and post-layout simulated in TSMC 90 nm CMOS technology node using the Cadence IC Suite. According to the simulation results the implemented architecture improves the stability performance of the circuit, achieving 89.45° phase margin along with $101.3\ dB$ DC gain.**

***Index Terms*—Analog VLSI, Low Power design, Operational Amplifier, Nested Loops**

I. Introduction

Integrated Circuits (ICs) have revolutionized modern electronics by packing an array of electronic components onto a single chip. One of the main building blocks in IC design is the operational amplifier (op-amp). These versatile devices play a critical role in various applications, spreading from analog signal processing and computing to voltage regulation and amplification. Op-amps are integral to countless electronic systems, ranging from audio amplifiers and data acquisition circuits to power management units in portable devices [1], [2]. Their main advantage is the ability to provide high gain, high input impedance, low output impedance and versatile signal processing capabilities, making them indispensable in IC design [3].

Ensuring the stability and robustness of op-amps in ICs is of great importance. Stability issues can lead to unintended oscillations and instability in the system, which can compromise the overall performance or even provoke total malfunction. Moreover, robustness is essential to ensure that the circuit operates reliably across different operating conditions, such as variations in temperature, voltage and manufacturing process. Traditionally, op-amps are compensated using a single feedback loop, i.e. Miller compensation. However, the Miller effect has a serious drawback because a right-halfplane zero appears and if it lies at a low / medium frequency seriously affects the op-amp. This approach may have limitations in achieving the desired high-performance operation and robustness [4]. This enables the exploration of more advanced compensation techniques, such as nested $g_m - C$ loops, i.e. the nested transconductance-capacitance compensation (NGCC) topology. By employing multiple nested loops, it becomes possible to achieve enhanced performance and robustness, allowing for precise control of the op-amp's response and mitigating stability challenges often encountered with single-loop designs [5]. In this work, a nested $g_m - C$ loops compensated op-amp, is modelled, designed and simulated demonstrating the potential of this compensation technique in order to address critical limitations and improve the overall performance and robustness of ICs. The implementation of the op-amp is done in the TSMC 90nm CMOS process utilizing the Cadence IC suite for design and simulation flow.

The rest of this work is organized in the following manner. Section II provides the implemented amplifier's architecture model and transistor-level design. In Section III the op-amp's model described in Section II is mathematically analyzed regarding the frequency response, transfer function and stability behavior of the multiple-loops compensation. The simulation results of the realized op-amp are depicted in Section IV. A comparison study and discussion about the op-amp's overall performance is provided in Section V. Finally, Section VI presents some concluding remarks.

II. Amplifier's Architecture

In order to minimize the effects arising from the right-halfplane zeros, the architecture illustrated in Fig. 1 was implemented and is presented in this Section.

This topology consists of 4 cascade gain stages, denoted with their transconductance gains g_{m1}-g_{m4} and equivalent output resistances R_1-R_4. The last stage in the chain has negative gain in contrast to the first 3 stages. Additionally, the op-amp's compensation is accomplished using 3 feedback loops which consist of the capacitors C_{m1}, C_{m2} and C_{m3}, connected to take advantage of the Miller effect in order to avoid very large values for them. Due to these capacitors 3 right-halfplane zeros are added to the dynamics of the system, jeopardizing its stability if any of them lie at low/medium frequencies. A possible approach to account for the effects of these capacitors on the op-amp is to "push" the added zeros to very high frequencies. Intending to do so, feedforward compensation technique is utilized. Specifically, feedforward

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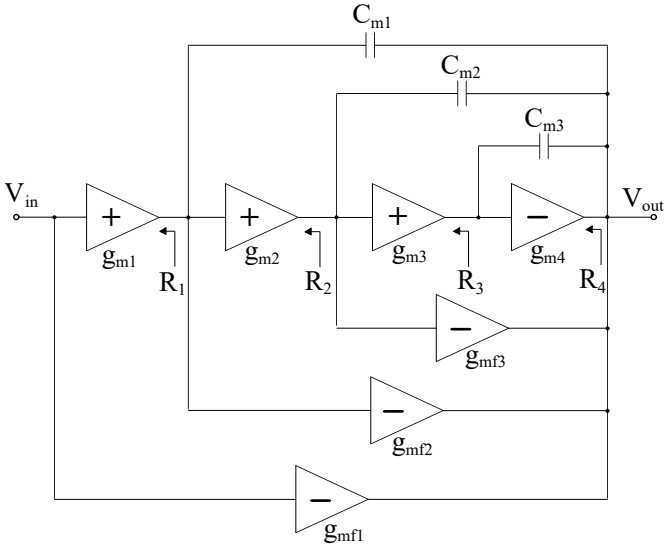

Fig. 1: Architecture of the implemented op-amp, leveraging the nested $g_m - C$ loops to achieve increased performance regarding stability issues [6].

gain stages denoted by their transconductance g_{mf1}-g_{mf3} are added for each corresponding zero, as shown in the model of Fig. 1. As explained thoroughly in the mathematical analysis of Section III, the transconductance gain (g_{mfi}) of each feedforward stage must be equal to the corresponding transconductance of each op-amp stage (g_{mi}). This way, the corresponding zero is placed at very high frequencies where it has practically no influence on the stability, minimizing the impact on the op-amp.

TABLE I: MOS Transistors' Dimensions (Fig. 2).

NMOS	**W/L (μm/μm)**	**PMOS**	**W/L (μm/μm)**
M_{n1}-M_{n4}	4/1	M_{p1},M_{p2}	16/1
M_{n5}	3.94/1	M_{p3}	20/1
M_{n6}-M_{n10}	4/1	M_{p4}	16/1
M_{n11}	3.76/1	M_{p5}	4/1
M_{n12}	2/1	M_{p6},M_{p7}	4/12
-	-	M_{p8},M_{p9}	8/1
-	-	M_{p10}	60/1

The circuit implementation of the architecture described previously is illustrated in Fig. 2. The transistors M_{p1}, M_{p2} along with the current mirror formed by the transistors M_{n1}, M_{n2} compose the first stage of the op-amp (g_{m1}), realizing a single-ended differential pair. The corresponding feedforward path is designated by the transistor M_{n5} accompanied with the current mirrors M_{n1}-M_{n3} and M_{n4}-M_{n5}. The M_{n5} is connected in common source (CS) topology and has to be biased, via transistor M_{p4} and sized appropriately so that $g_{m1} = g_{mf1}$. The CS connected transistor M_{n6} along with the current mirror M_{p6}-M_{p7} compose the second stage of the op-amp. The mirror M_{p6}-M_{p7} inverts the phase of the signal thus making the voltage gain positive. As for the corresponding feedforward stage, the transistor M_{n11} is used which must be equally sized with the transistor M_{n6} so that the currents through them are equal. The fact that $V_{gs,M_{n11}} = V_{gs,M_{n6}}$ assures that $g_{m2} = g_{mf2}$. For the third stage, the same design approach has been applied. For the final gain stage a CMOS inverter was designed where the CS transistor M_{p10} provides the negative gain g_{m4}. The transistors' sizes are summarized in Table I.

III. Loop Stability Analysis

In this Section, the mathematics behind the nested $g_m - C$ loops compensation technique are presented. The analytical computation of the transfer function of the circuit is necessary in order to analyze its stability. For this reason, a high-frequency small signal analysis is conducted to extract the transfer function. Applying the Kirchhoff voltage and current laws leads to the following system of equations in the Laplace frequency domain

$$(1 + sC_{m1}R_1)\, v_1 - g_{m1}R_1 v_{in} - sC_{m1}R_1 v_{out} = 0 \quad (1)$$

$$(1 + sC_{m2}R_2)\, v_2 - g_{m2}R_2 v_1 - sC_{m2}R_2 v_{out} = 0 \quad (2)$$

$$(1 + sC_{m3}R_3)\, v_3 - g_{m3}R_3 v_2 - sC_{m3}R_3 v_{out} = 0 \quad (3)$$

$$\begin{aligned}[1 + s\,(C_{m1} + C_{m2} + C_{m3})\, R_4]\, v_{out} + g_{mf1}R_4 v_{in} + \\ (g_{mf2}R_4 - sC_{m1}R_4)\, v_1 + (g_{mf3}R_4 - sC_{m2}R_4)\, v_2 + \\ (g_{mf4}R_4 - sC_{m4}R_4)\, v_3 = 0 \end{aligned} \quad (4)$$

where v_i is the ac voltage on the i-node, g_{mi} is the transconductance gain of each stage, R_i is the output resistance of each stage and g_{mfi} is the transconductance gain of each feedforward stage.

The solution of the above system results in the transfer function of the circuit

$$G(s) \triangleq \frac{v_{out}}{v_{in}} \equiv \frac{N(s)}{D(s)}$$

The nominator of the transfer function is :

$$\begin{aligned} N(s) = s^3\,[C_{m1}C_{m2}C_{m3}R_1R_2R_3R_4(g_{m1} - g_{mf1})] + \\ s^2\{C_{m1}R_1R_4(C_{m2}R_2 + C_{m3}R_3)(g_{m1} - g_{mf1}) + \\ C_{m2}C_{m3}R_1R_3\,[R_2R_4g_{m1}(g_{m2} - g_{mf2}) + R_4g_{mf1}]\} + \\ s\{C_{m1}R_1R_4(g_{m1} - g_{mf1}) + \\ C_{m2}R_2R_4\,[g_{m1}R_1(g_{m2} - g_{mf2}) + g_{mf1}] \\ + C_{m3}R_3R_4\,[R_1R_2g_{m1}g_{m2}(g_{m3} - g_{mf3}) + g_{mf1}(1 + R_1g_{mf2})]\} \\ + R_1R_2g_{m1}g_{m2}(R_3R_4g_{m3}g_{m4} + R_4g_{mf3}) \\ + g_{m1}g_{mf2}R_1R_4 + g_{mf1}R_4 \end{aligned} \quad (5)$$

In order to place the zeros of the system to very high frequency, the transconductance of each gain stage g_{mi} has to be equal to the transconductance g_{mfi} of the corresponding feedforward path. This way, the impact of these zeros on the stability of the system is minimized and if we ignore very small terms, the nominator of the transfer function is simplified as follows:

$$\begin{aligned} N(s) = s^2R_4g_{mf1} + s[C_{m2}R_2R_4g_{mf1} \\ + C_{m3}R_3R_4(g_{mf1} + R_1g_{mf1}g_{mf2})] + A_o \end{aligned} \quad (6)$$

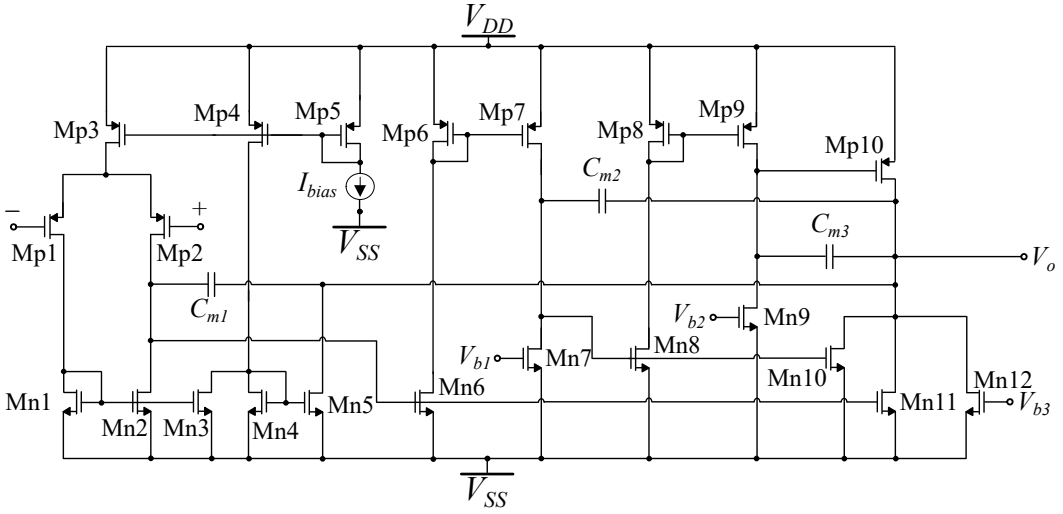

Fig. 2: Transistor level design of the implemented op-amp.

where $A_o = g_{m1}g_{m2}g_{m3}g_{m4}R_1R_2R_3R_4$.

Applying the same process to the denominator the result is:

$$D(s) = s^3(C_{m1}C_{m2}C_{m3}R_1R_2R_3R_4g_{m4}) + s^2(C_{m1}C_{m2}R_1R_2R_3R_4g_{m3}g_{m4}) + s(C_{m1}R_1R_2R_3R_4g_{m2}g_{m3}g_{m4}) + 1 \quad (7)$$

Because of the computational complexity that emerges when trying to compute the poles and place them to desirable positions, the Open-Circuit Time Constants (OCTC) method is applied. OCTC gives an estimation (usually pessimistic) for the position of the poles of a circuit. However, the accuracy provided by OCTC is sufficient when designing the circuit and it is a useful method when dealing with complicated transfer functions [4]. Therefore the dominant pole is derived as

$$\omega_{p1} = \frac{1}{(R_1 + R_4 + g_{m2}g_{m3}g_{m4}R_1R_2R_3R_4)C_{m1}} \cong \frac{1}{g_{m2}g_{m3}g_{m4}R_1R_2R_3R_4C_{m1}} \quad (8)$$

In similar manner, the non-dominant poles' frequencies are calculated

$$\omega_{p2} \cong \frac{1}{gm3g_{m4}R_3R_4R_2Cm2} \quad (9)$$

$$\omega_{p3} \cong \frac{1}{g_{m3}g_{m4}R_3R_4C_{m_3}} \quad (10)$$

In op-amp design, a single pole behavior is usually desirable in order to achieve both high gain and descent stability performance. Furthermore, the calculation of the unity gain bandwidth (UGBW) of the opamp, i.e. the frequency that its gain is 0dB, is a necessity. In a single-pole transfer function the calculation of the UGBW is quite simple and it can be derived as follows

$$\omega_t = \frac{\omega_{p_1}}{A_o} = \frac{g_{m1}}{C_{m1}} \quad (11)$$

From the last result, it is directly concluded that in order to increase the bandwidth of the amplifier, the circuit must be biased in such a way that it has a large g_{m1}. Moreover, it should be verified that the system is stable and ensure that it has a descent phase margin. The phase margin is given as follows

$$\phi_{pm} = 90^\circ - tan^{-1}\left(\frac{\omega_t}{\omega_{p2}}\right) - tan^{-1}\left(\frac{\omega_t}{\omega_{p3}}\right) - tan^{-1}\left(\frac{\omega_t}{\omega_{z1}}\right) - tan^{-1}\left(\frac{\omega_t}{\omega_{z2}}\right) \quad (12)$$

where ω_{z1} and ω_{z2} are the frequencies of the right-halfplane zeros which are much larger than ω_t, as mentioned above.

IV. Simulation Results

TABLE II: Performance Results

Parameter	Value
Power Supply	0.9 V
DC Gain	101.3 dB
Phase Margin	89.45°
Gain Margin	29.87 dB
Unity Gain Bandwidth (UGBW)	1.95 MHz
Power Consumption	28.11 μW
Load conditions	20 pF // 20kΩ
Area	0.04 mm^2

The simulation was conducted on the layout of the implemented op-amp, as shown in Fig. 3. For simulation purposes it was connected in an ideal negative feedback loop with $V_{CM} = 570$ mV as common-mode input voltage. The ideal feedback was formed using an ideal voltage buffer for the output of the op-amp V_{out} in series with a very large-value inductor and a very large-value capacitor to V_{SS}. The simulations were conducted with a 20 pF capacitor in parallel with a 20 kΩ resistor as load. In addition, the bias current was set to $I_{bias} = 1\mu$A in order to achieve the minimum possible power consumption with all transistors operating in saturation

TABLE III: Operational Amplifiers' performance comparison

	Process	Supply	Load conditions	DC gain	Phase margin	Gain margin	UGBW	Power Consumption	Estimated area
This work	$90nm$	0.9 V	$20k\Omega//20pF$	101.3 dB	89.45°	29.87 dB	1.95 MHz	28.11 μW	0.04 mm^2
[5]	$0.8\mu m$	2 V	$25k\Omega//100pF$	>100 dB	48°	NA	2.6 MHz	676 μW	0.14 mm^2
[6]	$2\mu m$	2 V	$10k\Omega//20pF$	100 dB	60°	NA	610 kHz	0.68 mW	0.22 mm^2
[7]	$0.6\mu m$	3 V	$20k\Omega//1pF$	96.76 dB	83.66°	10.53 dB	59.51 MHz	4.41 mW	NA
[8]	$0.6\mu m$	3 V	$40pF$	102 dB	76°	18 dB	47 MHz	6.9 mW	NA
[9]	$0.8\mu m$	2 V	$25k\Omega//120pF$	>100 dB	65°	NA	4.5 MHz	0.4 mW	0.06 mm^2
[10]	$0.35\mu m$	1.5 V	$150pF$	110 dB	$>57^\circ$	NA	4.4 MHz	30 μW	<0.02 mm^2

region. In Table II the simulation performance of the op-amp is summarized.

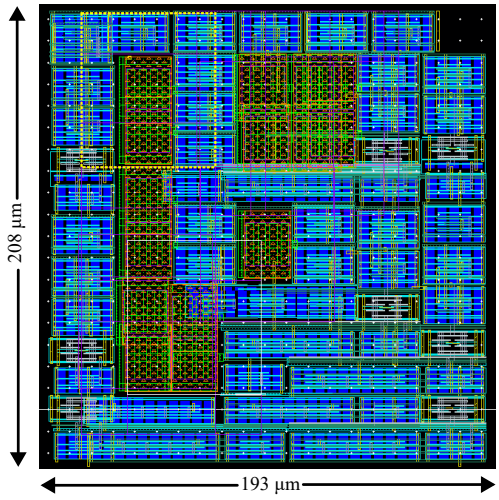

Fig. 3: The layout of the implemented amplifier.

Under the earlier mentioned conditions, the op-amp can provide a quite high DC voltage gain of around 100 dB; a reasonable value since four cascaded stages are used. The main advantage of this circuit is the stability performance. Even though the op-amp consists of four cascaded stages and three right-halfplane zeros appear due to the Miller effect of the three compensation capacitors, the circuit achieves a Phase Margin (PM) higher than 89° establishing a very robust design. Additionally, unity gain bandwidth is quite decent and lies at approximately 2 MHz, while Gain Margin (GM) is always more than 29 dB. Last but not least, the total value of the three compensation capacitors is no more than 6 pF which saves valuable chip area highlighting the importance of Miller effect.

V. Comparison and Discussion

In this Section, the realized op-amp is compared to other amplifiers that utilize various, both conventional and advanced, compensation techniques. The performance results of these designs are described in Table III.

The proposed architecture outperforms the other operational amplifiers in terms of phase margin, gain margin and power consumption making it a significantly more energy-efficient but at the same time very robust choice. Moreover, it achieves a high small-signal DC gain in comparison with the other implementations in Table III, except of [10] which has higher gain sacrificing phase margin. Regarding the Unity Gain Bandwidth (UGBW), the proposed design has a descent value taking into account the value of the capacitive load used along with the low bias currents in the amplifier.

VI. Conclusion

In this work, a nested $g_m - C$ loops operational amplifier has been implemented, using cascade gain stages, along with Miller-capacitors and feedforward paths compensation. Special care is given to analyze the dynamics of this compensation technique regarding the system frequency response. The circuit is designed and post-layout simulated in TSMC 90 nm CMOS process using the Cadence IC Suite. According to the simulation results the implemented architecture improves the stability performance of the circuit, achieving 89.45° phase margin along with 101.3 dB small signal DC gain.

References

[1] W. Jung, *Op Amp applications handbook*. Newnes, 2005.

[2] B. Carter, T. R. Brown *et al.*, *Handbook of operational amplifier applications*. Texas Instruments Dallas, TX, 2001, vol. 9.

[3] P. R. Gray and R. G. Meyer, "Mos operational amplifier design-a tutorial overview," *Ieee journal of solid-state circuits*, vol. 17, no. 6, pp. 969–982, 1982.

[4] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and design of analog integrated circuits*. John Wiley & Sons, 2009.

[5] K. N. Leung and P. K. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE transactions on circuits and systems I: fundamental theory and applications*, vol. 48, no. 9, pp. 1041–1056, 2001.

[6] F. You, S. H. Embabi, and E. Sanchez-Sinencio, "Multistage amplifier topologies with nested g/sub m/-c compensation," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, 1997.

[7] N. Baxevanakis, I. Georgakopoulos, and P. P. Sotiriadis, "Rail-to-rail operational amplifier with stabilized frequency response and constant-gm input stage," in *2017 Panhellenic Conference on Electronics and Telecommunications (PACET)*. IEEE, 2017, pp. 1–4.

[8] H.-T. Ng, R. M. Ziazadeh, and D. J. Allstot, "A multistage amplifier technique with embedded frequency compensation," *IEEE Journal of Solid-state circuits*, vol. 34, no. 3, pp. 339–347, 1999.

[9] H. Lee and P. K. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 511–520, 2003.

[10] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance adapting compensation for low-power multistage amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 445–451, 2010.